AJIT CORE BUS and AJIT FIFO BUS Explained

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The primary interfaces between the AJIT processor and the external world are:

- AJIT CORE BUS interface (ACB): A 64-bit data, 36-bit address system memory interface.
- AJIT FIFO BUS interface (AFB): A 32-bit data, 36-bit peripheral/memory interface.

Both these bus interfaces involve a request and a response interface. The bus master sends a request word to the slave, which responds to the request with a response word. The exchange of data between the master and slave is regulated using a simple two-wire protocol.

1 AJIT core bus interface

This consists of a request FIFO and a response FIFO. The requester (AJIT processor) writes a request word into the request FIFO. The 110-bit request word has the following format:

```
--------------------------------
bit-field          meaning
--------------------------------
[109]              lock
```

[108]	read/write_bar
[107:100]	byte mask
[99:64]	address
[63:0]	write-data

The response FIFO consists of a 65-bit word with the following format:

bit-field	meaning
[64]	error
[63:0]	read-data

The request/response pair can be used with a pipelined memory.

2 AJIT FIFO bus interface

This also consists of a request FIFO and a response FIFO. The requester (AJIT processor) writes a request word into the request FIFO. The 74-bit request word has the following format:

bit-field	meaning
[73]	lock
[72]	read/write_bar
[71:68]	byte mask
[67:32]	address
[31:0]	write-data

The response FIFO consists of a 33-bit word with the following format:

bit-field	meaning
[32]	error
[31:0]	read-data

The request/response pair can be used with a pipelined memory.

3 ACB/AFB Protocol and Timing

Both the ACB and AFB schemes are similar in their timing. We illustrate the timing based on the setup described in Figure 1.

1. The master initiates a transaction by sending request data to the slave. Thus, the first transfer in a transaction is a request word (110 bits for ACB, 74 bits for AFB) which is transferred from the master to the slave.

2. After the slave has computed the response to the request, the slave sends response data to the master. Thus, the second transfer is response word (65 bits for ACB, 33 bits for AFB) which is sent to the master.

The protocol and protocol for each transfer is similar and is described below.

3.1 Timing of a single transfer

The protocol relies to two wires between the sender and receiver.

- The first wire goes from the sender to the receiver. On the sender side, this wire is interpreted as *sender has data to send*. This wire connects to the receiver's write_req port and the senders read_ack port.

- The second wire goes from the receiver to the sender. On the receiver side, this wire is interpreted as *receiver ready to receive*. This wire connects to the sender's read_req port and to the receiver's write_ack port.

Now the behaviour of the sender can be summarized as follows:

```
sender_has_data_to_send = 0
if (sender wants to send) {
   sender_data = DATA,
      sender_has_data_to_send = 1
   while(1) {
      if (receiver_ready_to_receive)
```

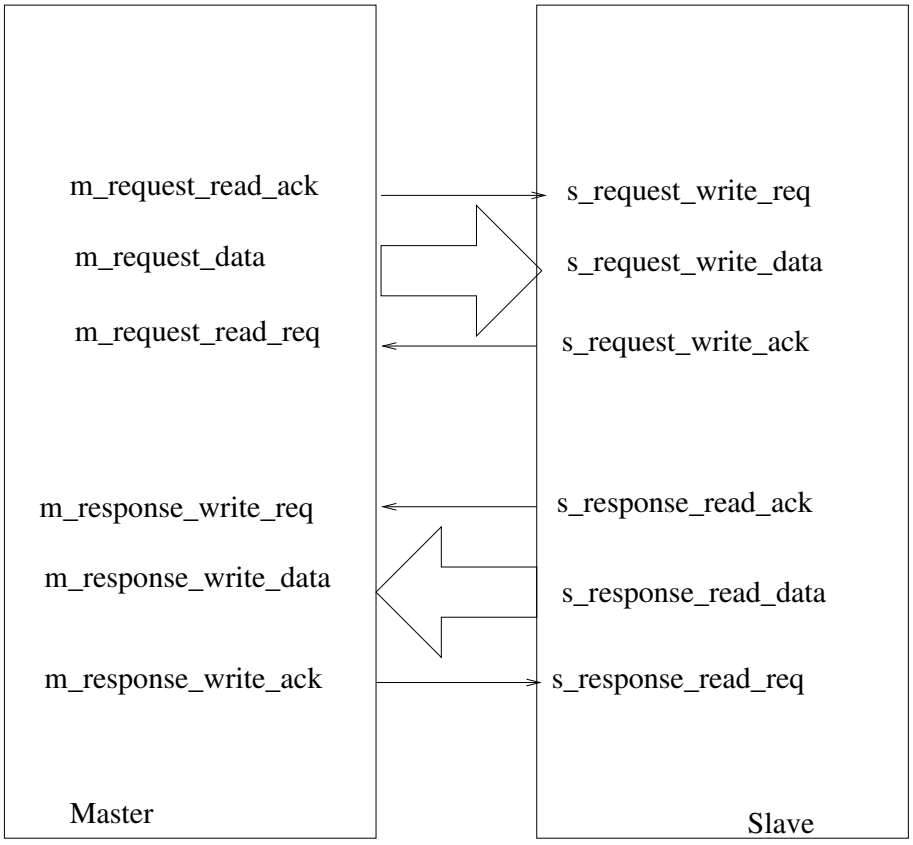

Figure 1: Visualization of setup for ACB/AFB master slave connections

```
         break; /* receiver has accepted */
   }
}
```

The behaviour of the receiver can be summarized as follows:

```
receiver_ready_to_receive = 0
if (receiver wants to receive) {
   receiver_ready_to_receive = 1
   while(1) {
      if (sender_has_data_to_send)
         REGISTER = sender_data
         break; /* receiver has accepted */
   }
}
```

This protocol is highly flexible and allows either the sender or receiver to block the transaction. For example, if the sender is faster than the receiver, the timing diagram will be as shown in Figure 2. If the receiver is faster than the sender, the timing diagram will be as shown in Figure 3. If both sender and receiver are full-rate, then the timing diagram will be as shown in Figure 4.

4 Summary

The ACB and AFB bus interfaces offer a simple, flexible mechanism to connect components in an AJIT system. Each bus interface consists of a request connection and a response connection. The data transfer on the request and response connection is managed using a simple two-wire protocol which can be used for full rate transfers as well as slow transfers.

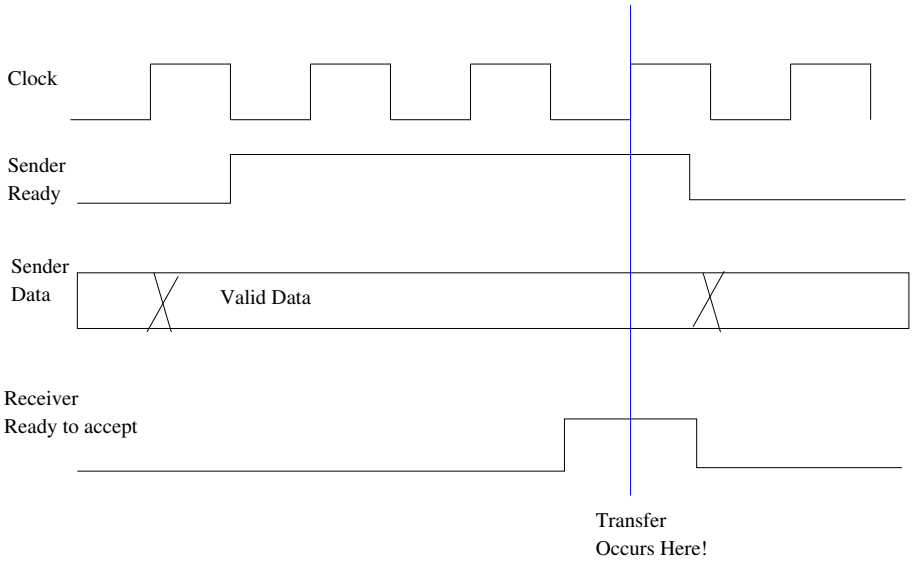

Figure 2: Timing Diagram for fast sender, slow receiver

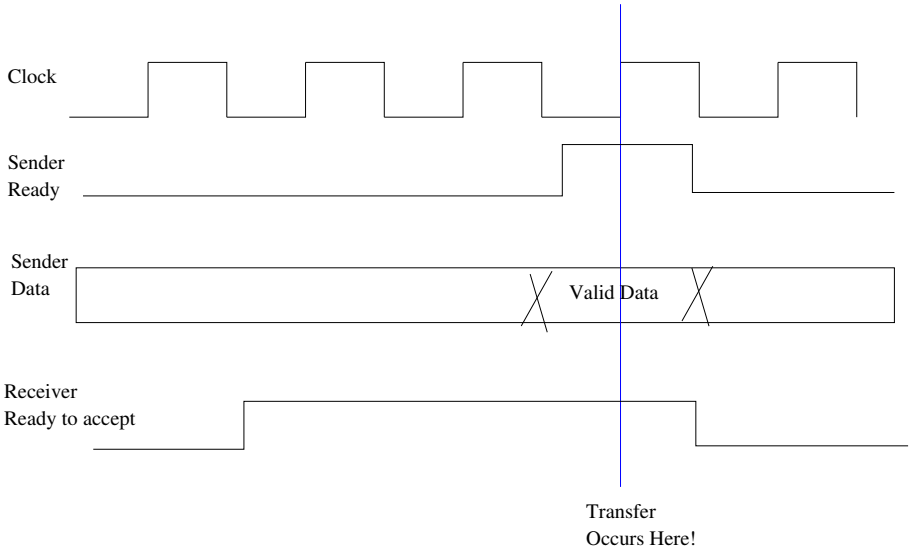

Figure 3: Timing Diagram for slow sender, fast receiver

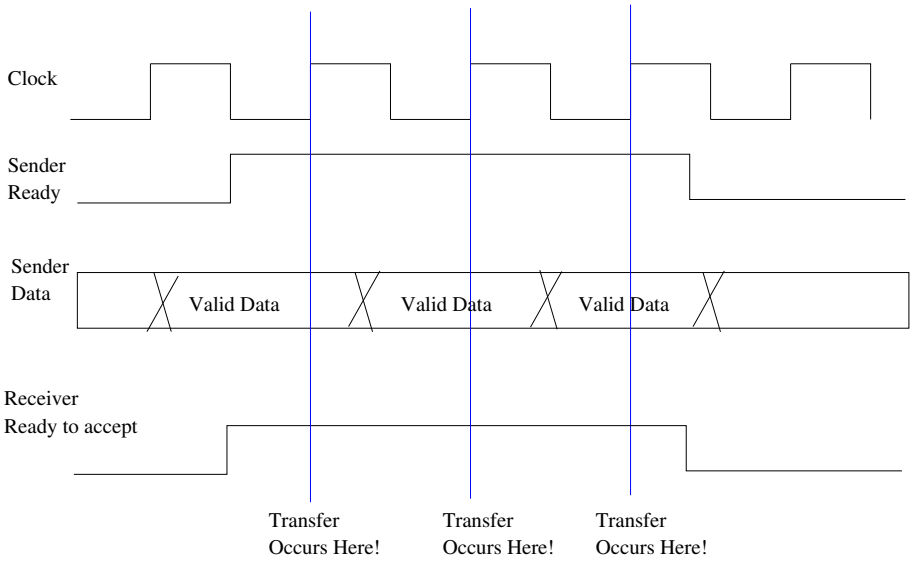

Figure 4: Timing Diagram for full-rate sender and receiver