March 12, 2020 # Memory Interleaving (Hamacher) Bubber Register ABR : Add ess DBR: Data K-bits m-bits ABR DBR ABR DBR ABR DBR ABR DB:R 000 111 MO MI m 2 m3 00 01 10 11

A Each Module has 8 locations,

Total there are 4 modeles i.e., 32 locations.

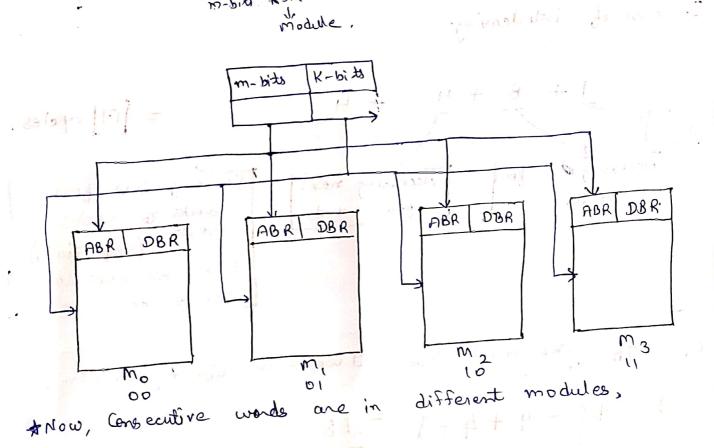
The generates 5 bit los address (let's say), then,

Modulei Addressin module

seper words exequentially. That's why we introduce memory—interlacing has been introduced. In memory—interlacing, all modules work indepently—or memory—interlacing, all modules work indepently—or independently or in parallel.

I'm memory-interlocing, lost two bits of address one used for identifying module.

Eg![1000]
m-bit Kbit
module.



Eg:- Cache-block size = 8 words, · One cycle is required to send main-memory address from CPU to main-memory. . B dock-cycle for accessing 1st word in a module. · 4 clock for accessing subsequent words from same for sending one - word to · One dock cycle Oache. Find the time orequired to send a black to cache Solution: without interleaving :-XF 1 + 8 138 cycle + CPU to main-memory Accessing 15+ For sending last Accessing never 7 words block to cache In case of interleaving: = 117 cy des, Accessing 10 1 St four Sending last four Accessing next blocks to fores words (sequentially) Since, all house some common data-line Eg: - It cache-block size = 9 words in above problem. → 1+8+4+4+1 = 18