① Arithmetic Logic Unit

Addition and Subtraction of Signed Numbers

x_i	$\overline{y_i}$	C_i	sum S_i	Carry-out C_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	
1	1	1	1	

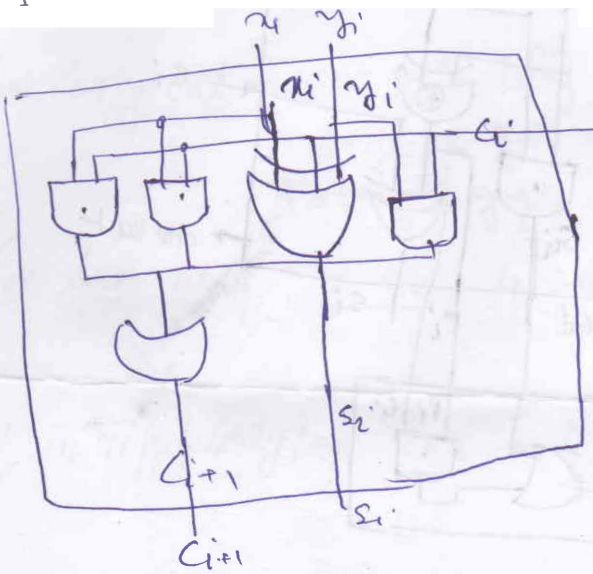
$S_i = \bar{x}_i y_i C_i + x_i y_i \bar{C}_i + x_i \bar{y}_i \bar{C}_i + x_i y_i C_i$

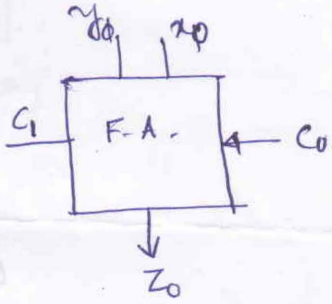
$= x_i \oplus y_i \oplus C_i$

$C_{i+1} = x_i y_i C_i + x_i y_i C_i + x_i \bar{y}_i \bar{C}_i + x_i y_i C_i$

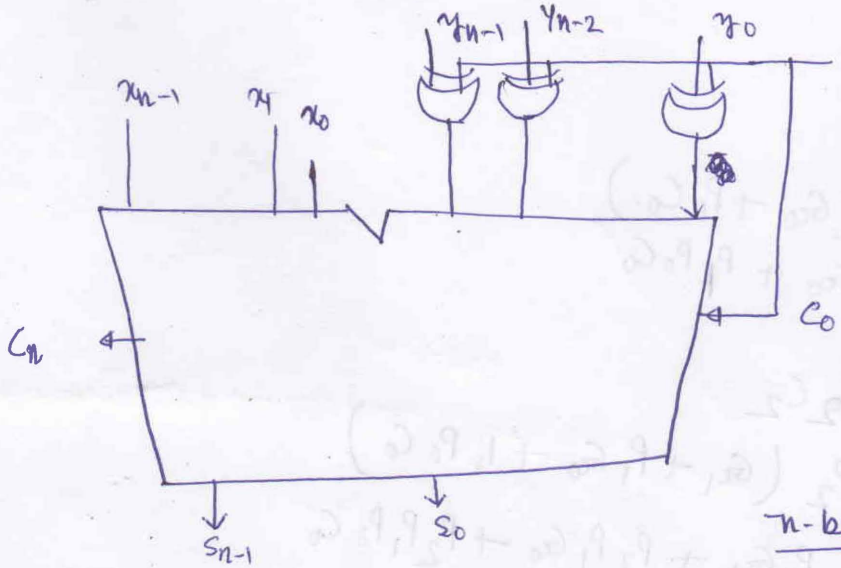
$= \bar{x}_i y_i C_i + x_i y_i C_i + x_i y_i$

$= y_i C_i + x_i C_i + x_i y_i$





n bit ripple-carry adder



X-Y
X+Y

Carryout

n-bit, delay : $C_n \rightarrow 2n$ gate delay

C_{n-1} $2(n-1)+1$

$= 2n-1$ gate delay.

Dt: 30/07/1982

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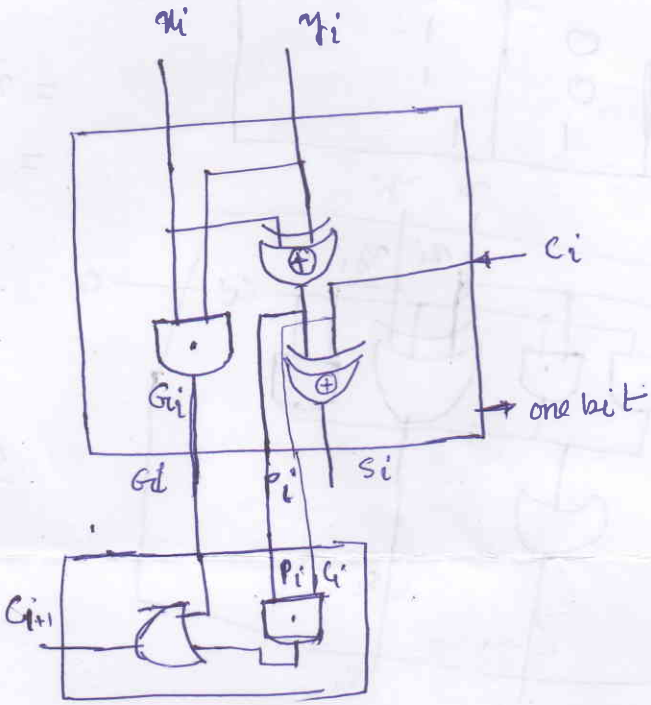
Design of Fast Adder

$$S_i = x_i \oplus y_i + c_i$$

$$C_{i+1} = x_i y_i + x_i c_i + y_i c_i$$
$$= x_i y_i + (x_i + y_i) c_i$$
$$= G_i + P_i c_i$$

Carry-out generated if $G_i = 1$, $x_i = 1$, $y_i = 1$, independent of c_i

Carry-out propagate if $P_i = 1$, $x_i = 1$ or $y_i = 1$



x_i	y_i	$x \oplus y$ / $x+y$
0	0	0
0	1	1
1	0	1
1	1	

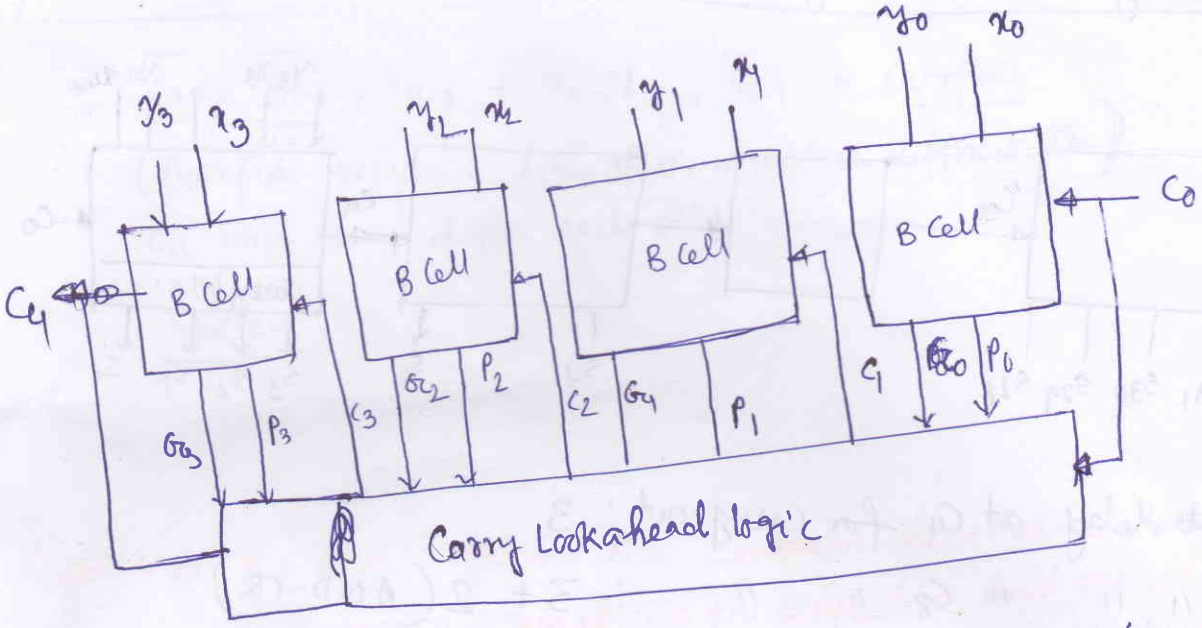
4-bit Adder.

$$C_1 = G_{i0} + P_0 C_0$$

$$C_2 = G_{i1} + P_1 C_1$$
$$= G_{i1} + P_1 (G_{i0} + P_0 C_0)$$
$$C_2 = G_{i1} + P_1 G_{i0} + P_1 P_0 C_0$$

$$C_3 = G_{i2} + P_2 C_2$$
$$= G_{i2} + P_2 (G_{i1} + P_1 G_{i0} + P_1 P_0 C_0)$$
$$= G_{i2} + P_2 G_{i1} + P_2 P_1 G_{i0} + P_2 P_1 P_0 C_0$$

$$C_4 = G_{i3} + P_3 C_3$$
$$= G_{i3} + P_3 (G_{i2} + P_2 G_{i1} + P_2 P_1 G_{i0} + P_2 P_1 P_0 C_0)$$
$$= G_{i3} + P_3 G_{i2} + P_3 P_2 G_{i1} + P_3 P_2 P_1 G_{i0} + P_3 P_2 P_1 P_0 C_0$$

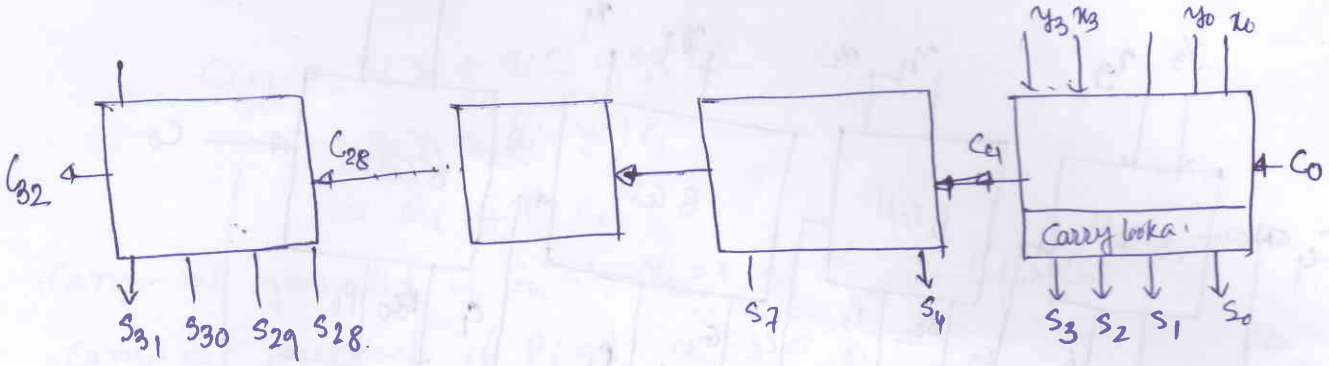


delay for Carry out - one gate delay for generating G_i / P_i
AND-OR gate for Carry out
Total 3 gate delay.

delay for Sum at C_4 : X-OR 4 gate delay.

gate delay in ripple carry: → $2 \times n$ → 8/8

Cascading the 4-bit Carry lookahead adder



Gate delay at C_4 for carry-out : 3

" " " C_8 " " : 3 + 2(AND-OR)

C_{12} " " : 3 + 2 × 2

C_{28} " " : 3 + 6 × 2 = 15

C_{32} " " : 15 + 2 = 17

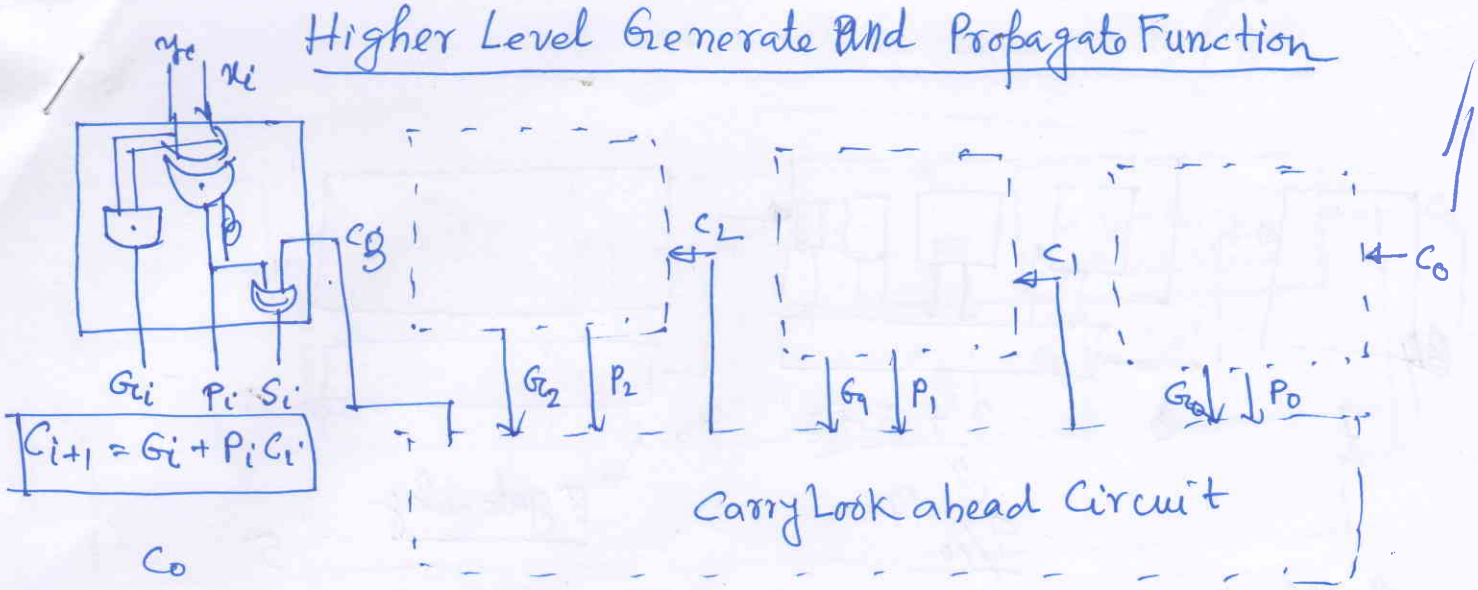
Sum S_{31} gate delay : 17 + 1 (X-OR)

S_{30} "

S_{29} "

S_{28} "

Higher Level Generate and Propagate Function



C_0

$C_1 = G_0 + P_0 C_0$

$C_2 = G_1 + P_1 G_0 + P_1 P_0 C_0$

$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$

$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$

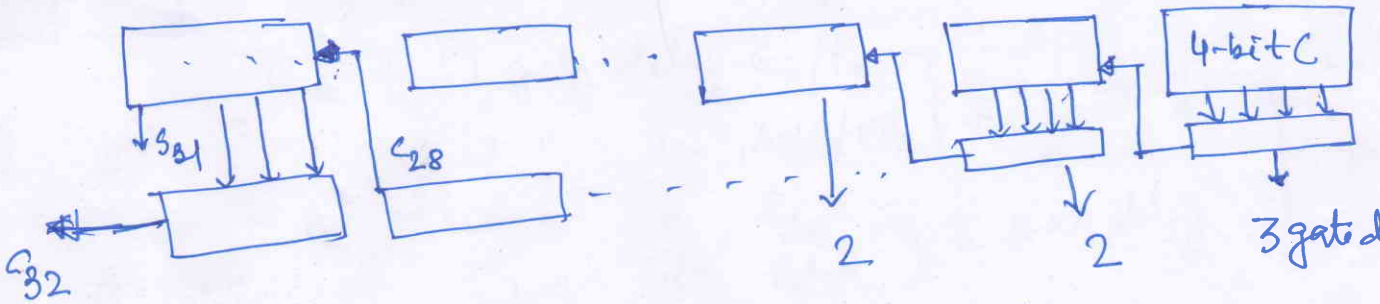
Gate-delay for C_4 → 1 (G_i/P_i) + 2 (AND-OR) = 3.

" " for S_3 → 3 + 1 (XOR) = 4.

Fan-in: # input of a logic gate

Fan-out: # input can be feed from an output of a logic gate.

How do you make 32-bit adder using 4-bit Carry look ahead adder?

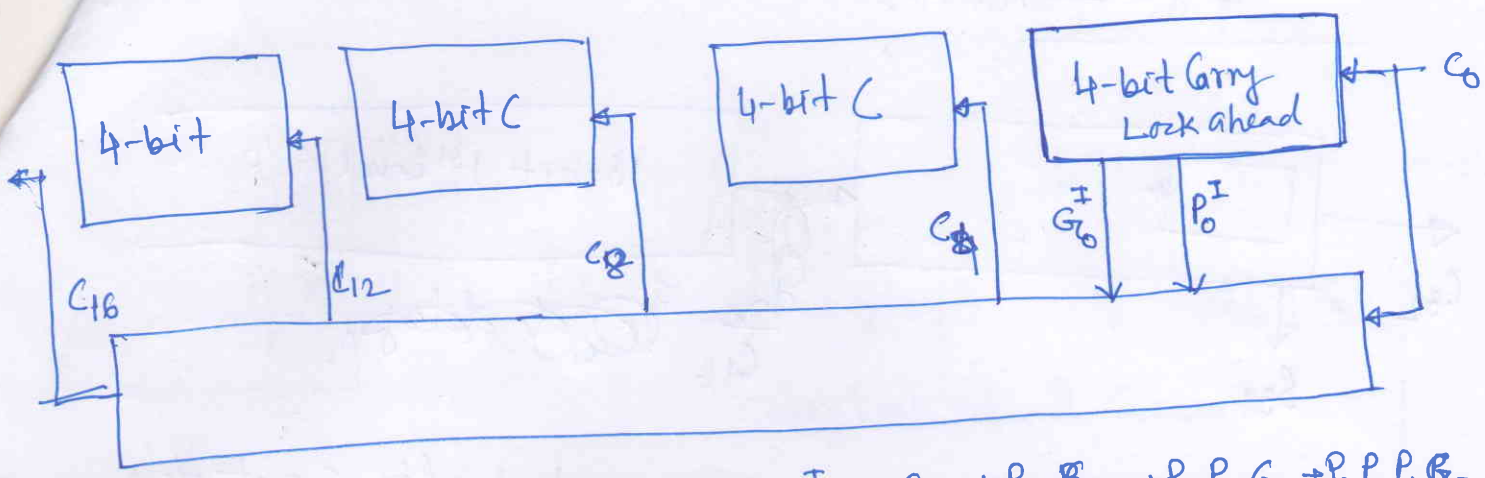


C_{28} will require 3 + 2 = 15 gate delay.

C_{28} " " 17 gate delay →

S_{31} " " 17 + 1 = 18 gate delay.

Higher Level Generate and Propagate



$$C_4 = G_{G0}^I + P_0^I C_0 \quad \Big\| \quad G_{G0}^I = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0$$
$$P_0^I = P_3 P_2 P_1 P_0$$

$$C_8 = G_{G1}^I + P_1^I C_4$$
$$= G_{G1}^I + P_1^I G_{G0}^I + P_1^I P_0^I C_0$$

$$C_{12} = G_{G2}^I + P_2^I C_8$$
$$= G_2^I + P_2^I G_1^I + P_2^I P_1^I G_0^I + P_2^I P_1^I P_0^I C_0$$

$$C_{16} = G_3^I + P_3^I G_2^I + P_3^I P_2^I G_1^I + P_3^I P_2^I P_1^I G_0^I + P_3^I P_1^I P_0^I C_0$$

Delay Analysis:

G_K^I : 1 gate delay G_i/P_i } 3-gate delay.
2 " " AND/OR }

P_K^I : 1 " " P_i } 2 gate delay.
1 " " AND }

G_K^I/P_K^I — 5 gate

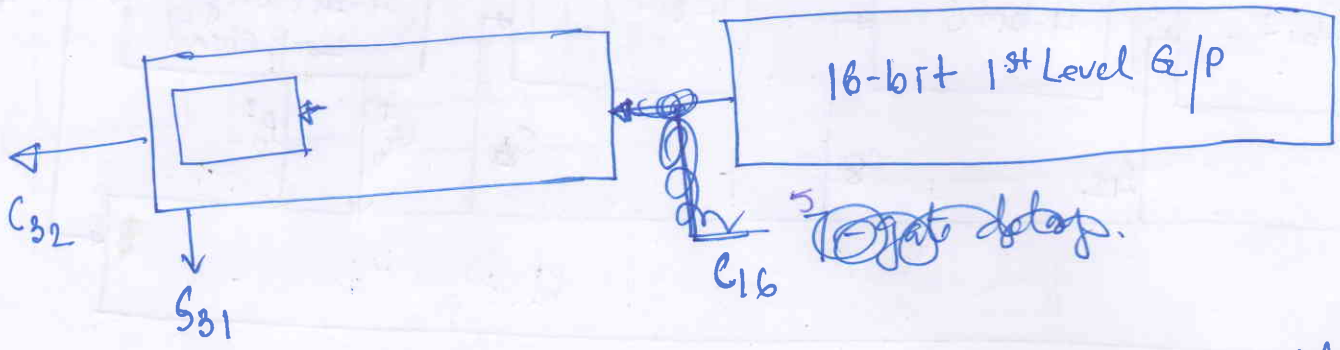
C_4, C_8, C_{12}, C_{16} → AND/OR, $P_0^I C_0$ / $P_1^I C_8$ /

Total 5 gate delay for $C_4, C_8, C_{12} C_{16}$.

S_{15} : C_{13}, C_{14}, C_{15} will require 2 gate delay after presently $C_{12} = 5+2 \rightarrow$ 7 gate.

S_{15} : one more gate delay : 7+1 = 8 gate.

32-bit adder using 2-16 bit higher level (first) Generate and Propagate function.



$C_{20}, C_{24}, C_{28}, C_{32}$ will be generated after 2 gate delay.
$= 7+2 = 9$ gate-delay.

C_{16} → need 5 gate delay ✓

$C_{20}/C_{24}/C_{28}/C_{32}$ needs $5+2 = 7$ gate delay. ✓

$C_{31} \rightarrow 7+2 \rightarrow 9$ gate delay ✓

$S_{31} \rightarrow 9+1 = 10$ gate delay. ✓

12-gate for Second Level Generate/Propagate.

7 gate delay for $C_{16}/C_{32}/C_{48}/C_{64}$ (3 → 1st level P/G, 2 → 2nd level P/G, 2 → AND/OR)

$C_{48} \rightarrow C_{52} \rightarrow C_{56} \rightarrow C_{60} \rightarrow C_{64}$

→ $7+2+2 \rightarrow C_{63}$ gate delay.

$11+1 \rightarrow S_{63}$ gate delay.