Analysis of Clocked Sequential Circuits

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- Analysis means what a given circuit will do under a certain operating conditions.
- The behavior of a sequential circuit can be determined from the inputs, outputs and the states of its flip flops.
- The out put and next state are both functions of inputs and present state.

- The **analysis** of sequential circuits starts from a circuit diagram and culminates in a state table or diagram.
- The **design** (synthesis) of a sequential circuit starts from a set of specifications and culminates in a logic diagram.

Analysis of Clocked Sequential Circuits

The behavior of a clocked sequential circuit can be described by

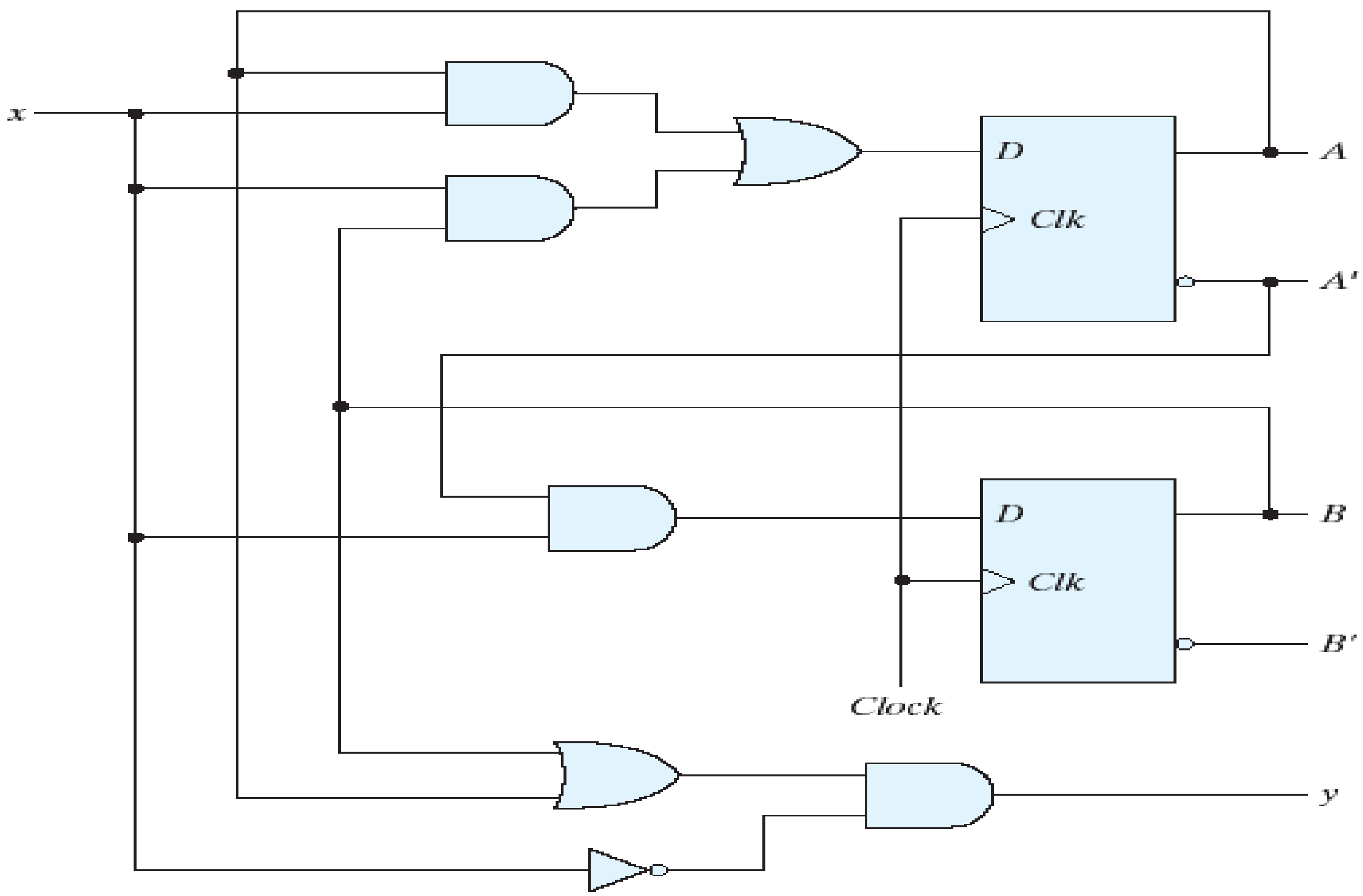
- **State Equation**
- **State Table**
- **State Diagram**
- **Flip flop Input Equations**

State equation

- Also called transition equation
- A state equation specifies the next state as a function of the present state and inputs.
- The behaviour of a clocked sequential circuit can be described algebrically by means of state equation.

- The LHS of the state equation denotes next state of the flip flop one clock pulse later
- The RHS of the state equation is a Boolean expression that specifies the present state and input conditions that makes the next state equal to 1.

An example of sequential circuit is analyzed through State equation



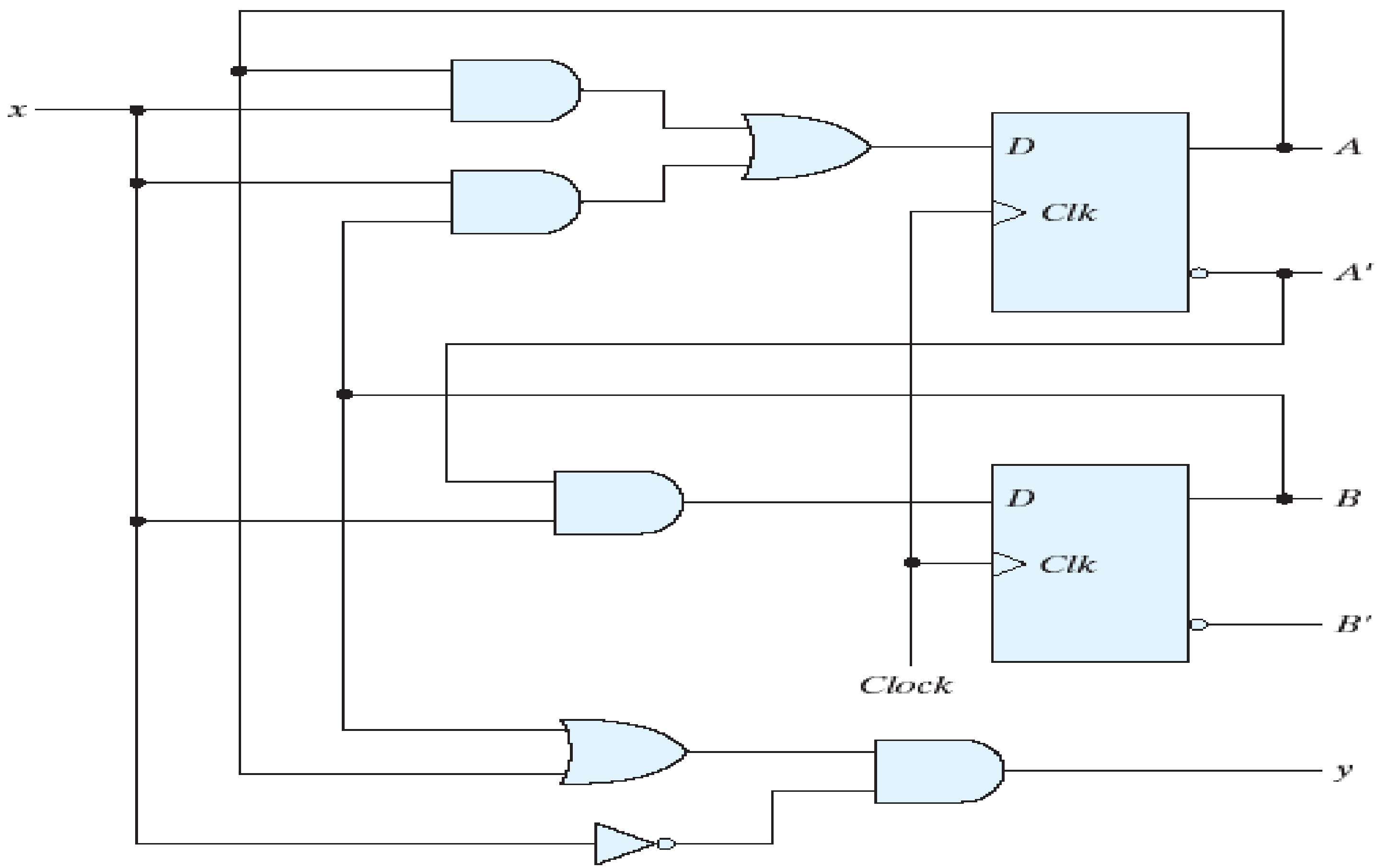
- The state equations can be written for the example as,

$$A(t+1) = A\,x + B\,x$$
$$B(t+1) = A'\,x,$$
$$y = (A + B)\,x'$$

State table

- Also called transition table.
- The time sequence of inputs, outputs and flip flop states can be combined in a state table.
- The state table consists of 4 sections: present state, input, next state, and output.

Analysis of Clocked Sequential Circuits through state table



State table

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

$A(t+1) = A\,x + B\,x$
$B(t+1) = A'\,x,$
$y = (A + B)\,x'$

Second Form of the State Table

Present State		Next State				Output	
		$x = 0$		$x = 1$		$x = 0$	$x = 1$
A	B	A	B	A	B	y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

$$A(t+1) = A\,x + B\,x$$

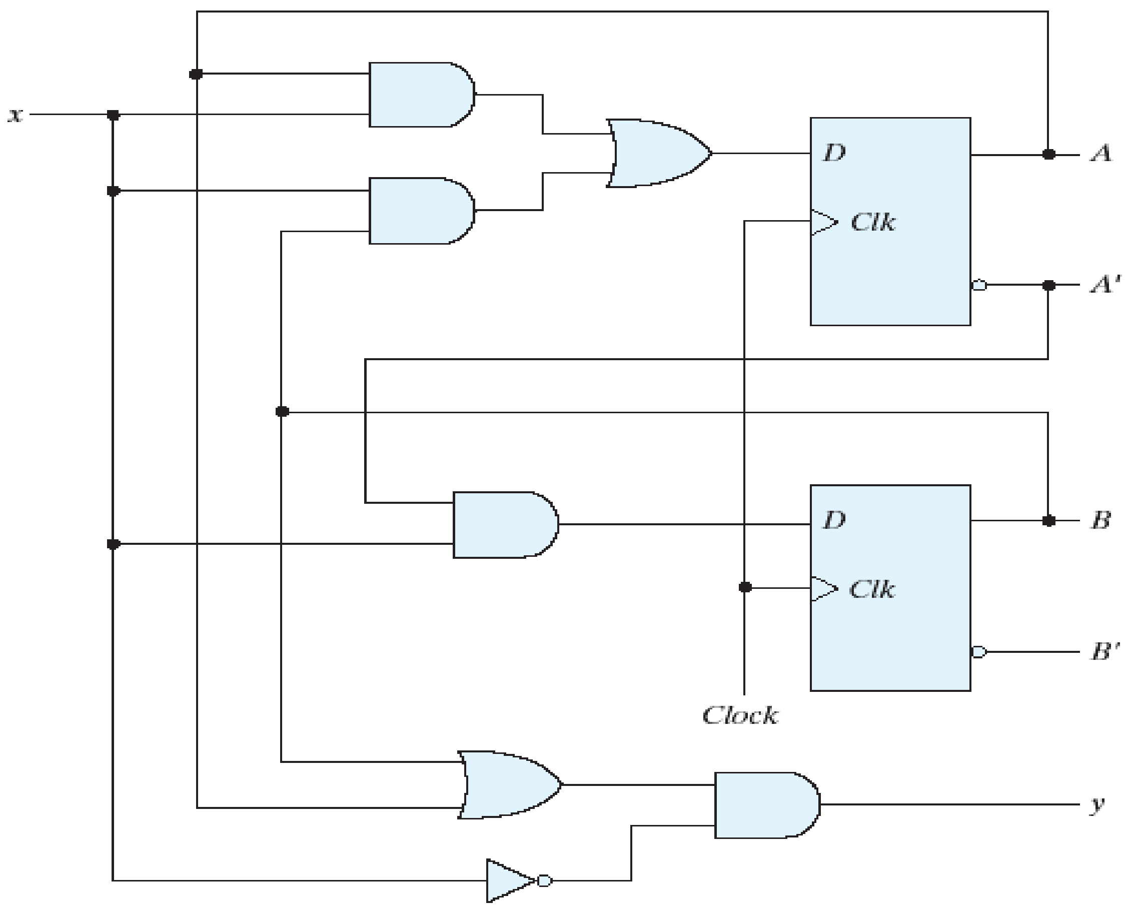
$$B(t+1) = A'\,x,$$

$$y = (A + B)\,x'$$

State Diagram

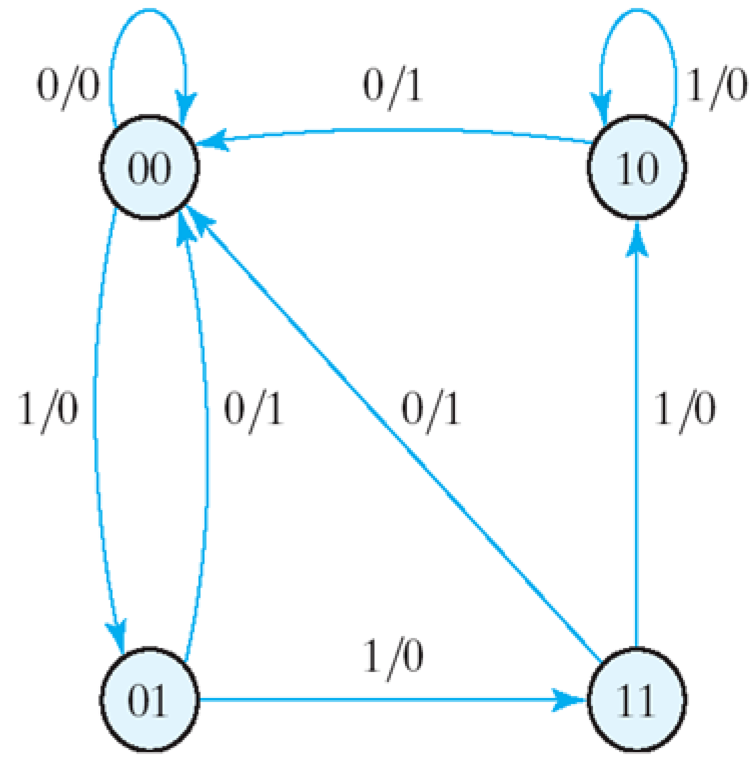
- The information available in a state table can be graphically represented by a state diagram.
- A state is represented by a circle and the transitions between states are represented by directed lines connecting the circles.

Analysis of Clocked Sequential Circuits



Analysis of Clocked Sequential Circuits through State Diagram

Present State		Next State				Output	
		$x = 0$		$x = 1$		$x = 0$	$x = 1$
A	B	A	B	A	B	y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

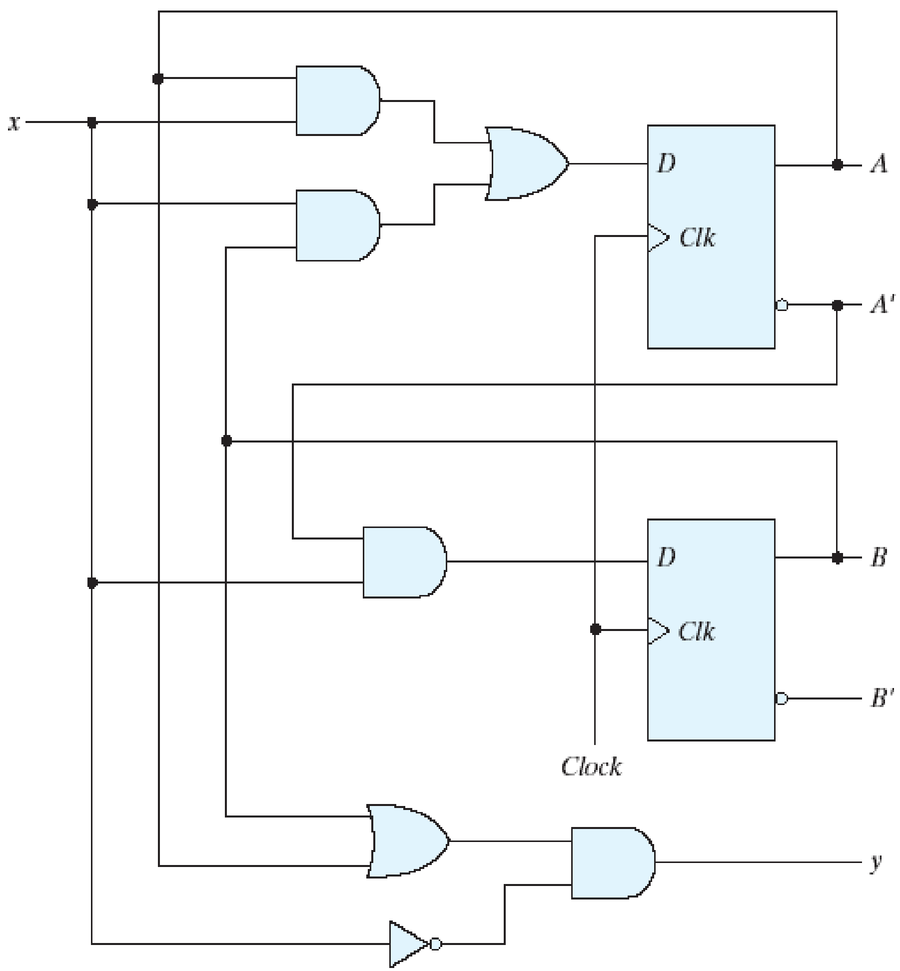


Flip-Flop input equations

- The logic diagram of a sequential circuit consists of **flip-flops** and **gates**.
- The interconnections among the gates form a combinational circuit and may be specified algebraically with **Boolean expressions**.
- The knowledge of the **type of flip-flops** and a list of the **Boolean expressions** of the combinational circuit provide the information needed to draw the logic diagram of the sequential circuit.

Flip-Flop input equations

- The part of the combinational circuit that generates external outputs is described algebraically by a set of Boolean functions called ***output equations***.
- The part of the circuit that generates the inputs of flip-flops is described algebraically by a set of Boolean functions called flip-flop ***input equations* (or *excitation equations*).**



Input equations:

$$D_A = A\,x + B\,x,$$

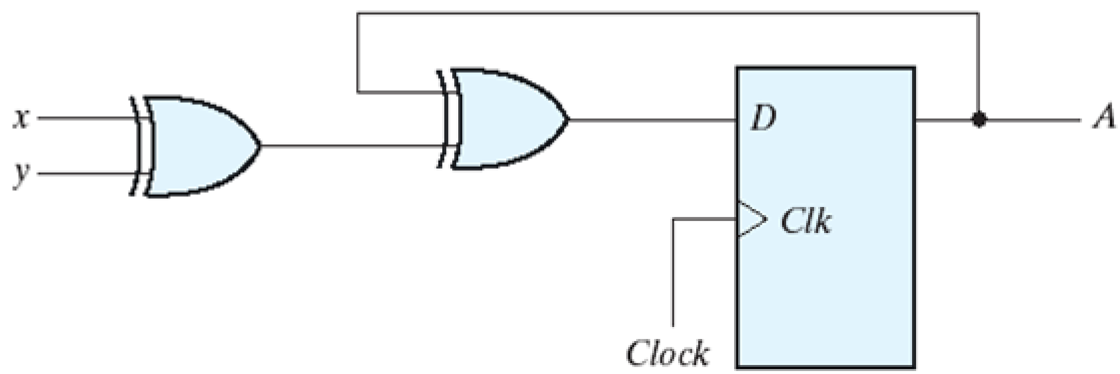
$$D_B = A'\,x.$$

Output equations:

$$y = (A + B)\,x'$$

These equations provide the necessary information for drawing the logic diagram of the sequential circuit.

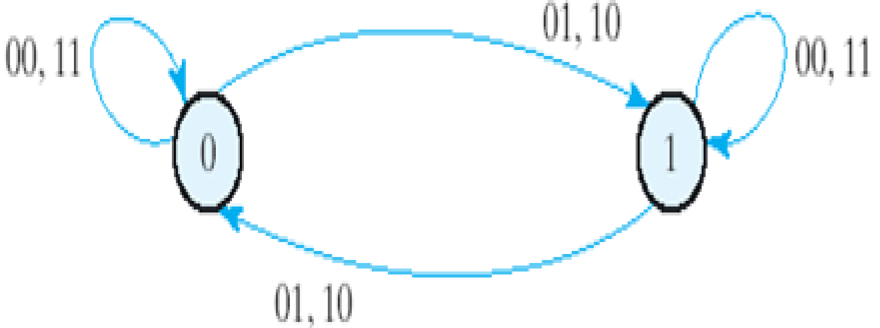
Analysis of Clocked Sequential Circuits with *D* Flip-Flops



(a) Circuit diagram

Present state	Inputs		Next state
A	*x*	*y*	*A*
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

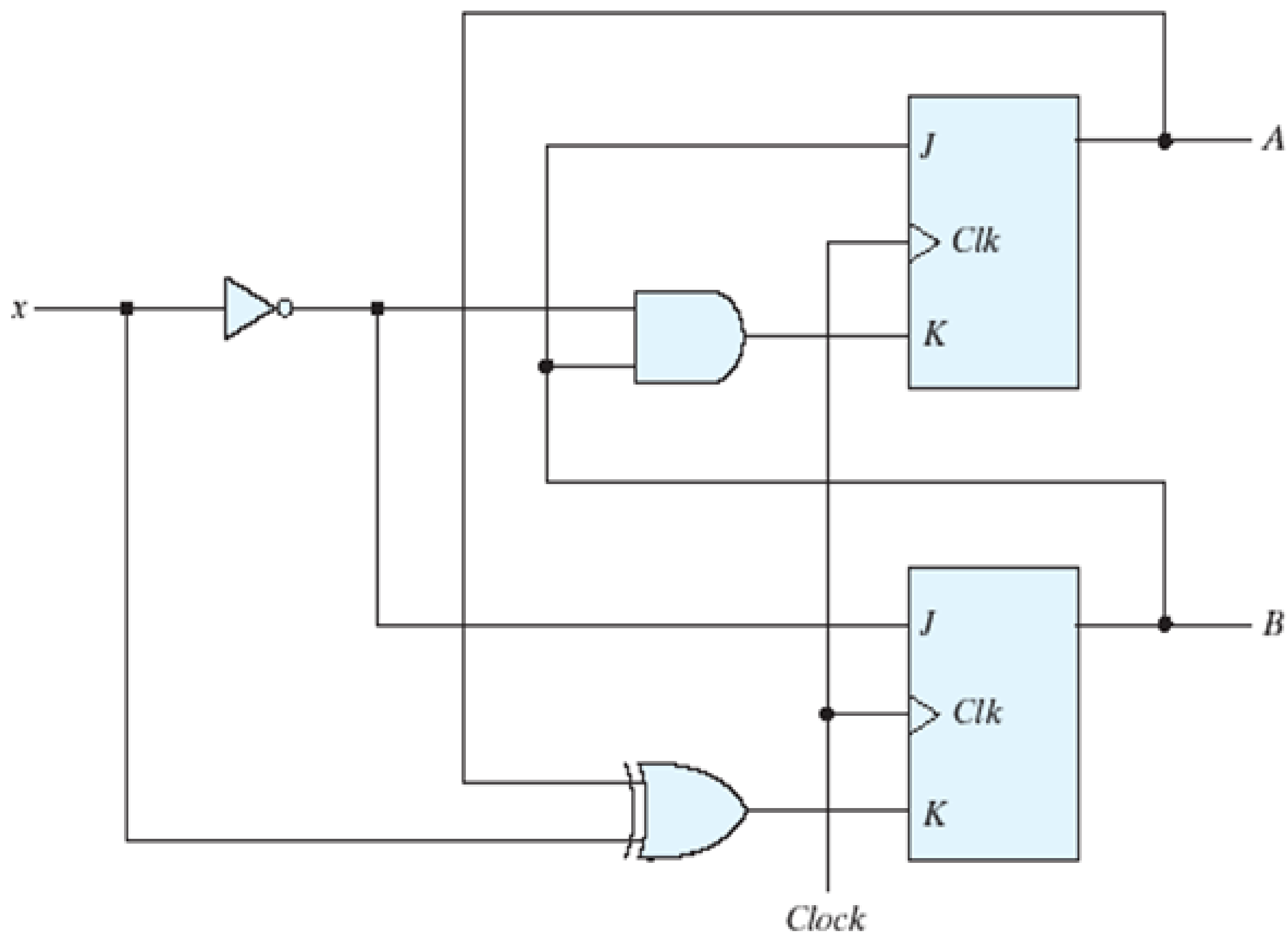
(b) State table



(c) State diagram

$$\boxed{\begin{array}{l} D_A = A \oplus x \oplus y, \\ A(t+1) = A \oplus x \oplus y \end{array}}$$

Analysis of Clocked Sequential Circuits with *JK* Flip-Flops



Input equations:

$J_A = B,$

$K_A = Bx',$

$J_B = x',$

$K_B = A \oplus x$

Analysis with *JK* Flip-Flops—State table

Present State		Input	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

Input equations:

$J_A = B,$

$K_A = Bx',$

$J_B = x',$

$K_B = A \oplus x$

Analysis with *JK* Flip-Flops—State equations

Input equations:

$J_A = B, K_A = Bx',$

$J_B = x', K_B = A \oplus x$

Characteristic equation: $Q(t+1) = J\,Q' + K'Q$

$$A(t+1) = J_A A' + K_A' A = BA' + (Bx')'A = BA' + B'A + xA$$

$$B(t+1) = J_B B' + K_B' B = x'B' + (A \oplus x)'B = x'B' + ABx + A'Bx'$$

Analysis with *JK* Flip-Flops—State diagram

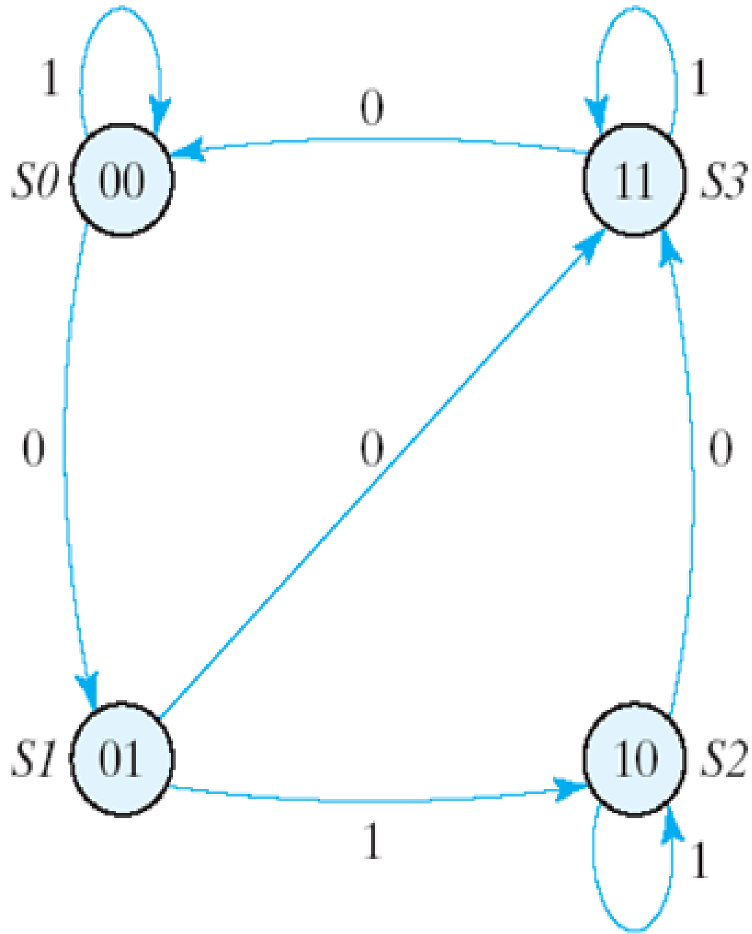
$A(t+1) = BA' + B'A + xA$
$B(t+1) = x'B' + ABx + A'Bx'$

$S0$: $A = 0, B = 0$

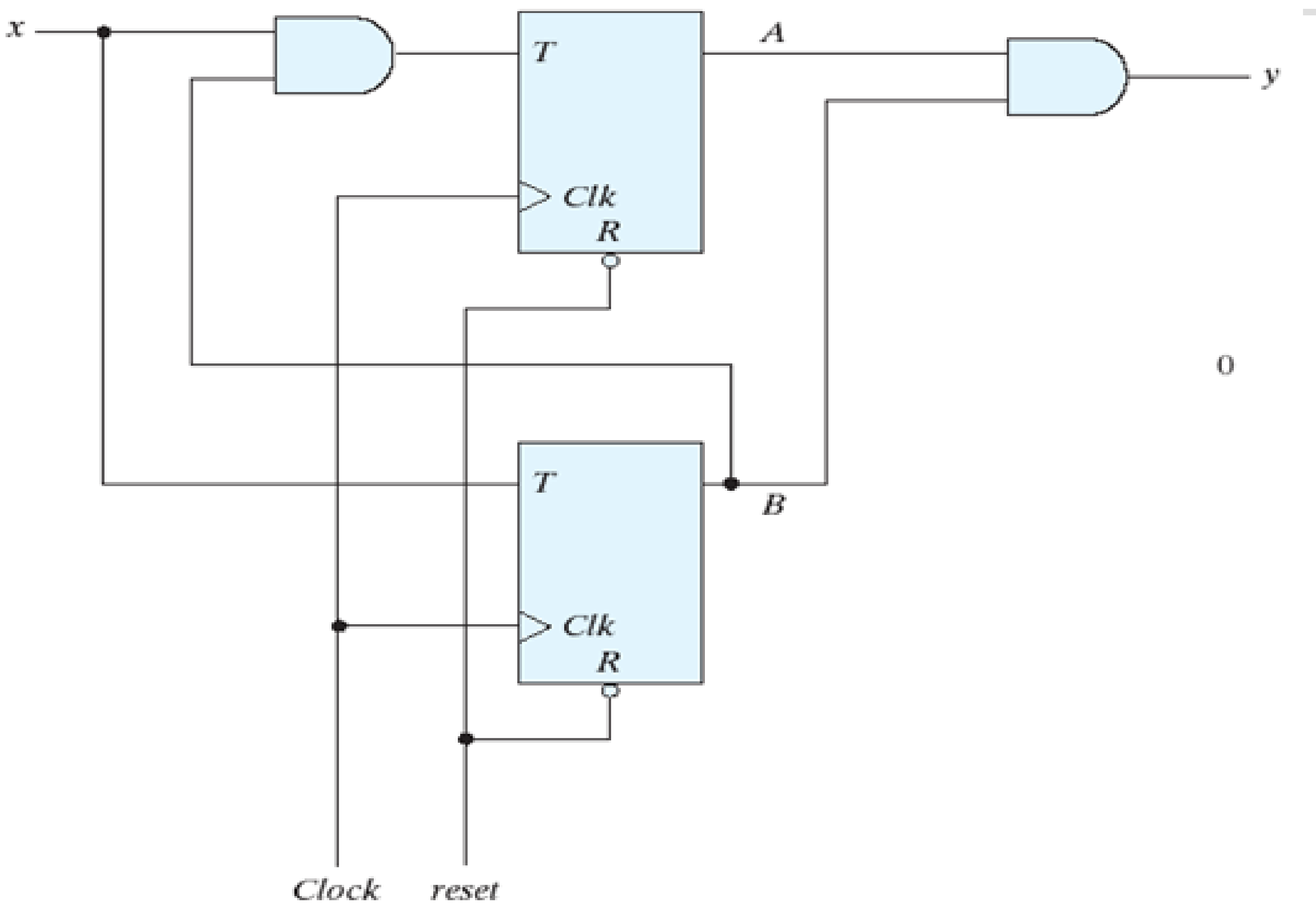
on $x = 1$, $A(t+1) = 0$,
$B(t+1) = 0$
$\Rightarrow S0 \rightarrow S0$

on $x = 0$, $A(t+1) = 0$,
$B(t+1) = 1$
$\Rightarrow S0 \rightarrow S1$

$S1$: $A = 0, B = 1$



Analysis of Clocked Sequential Circuits with *T* Flip-Flops



Input equations:

$$T_A = Bx,$$

$$T_B = x$$

Output equation:

$$y = AB$$

Analysis with *T* Flip-Flops – State table

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

Input equations:
$T_A = Bx,$
$T_B = x$
Output equation:
$y = AB$

Analysis with *T* Flip-Flops – State equations

Input equations: $T_A = Bx,\ T_B = x$

Output equation: $y = AB$

Characteristic equation: $Q(t+1) = T \oplus Q$

$$A(t+1) = (T_A \oplus A) = (Bx \oplus A)$$
$$= (Bx)'A + (Bx)A' = AB' + Ax' + A'Bx$$

$$B(t+1) = (T_B \oplus B) = (x \oplus B)$$

Analysis with *T* Flip-Flops – State diagram

.

$$A(t+1) = (Bx \oplus A)$$
$$B(t+1) = (x \oplus B)$$
$$y = AB$$

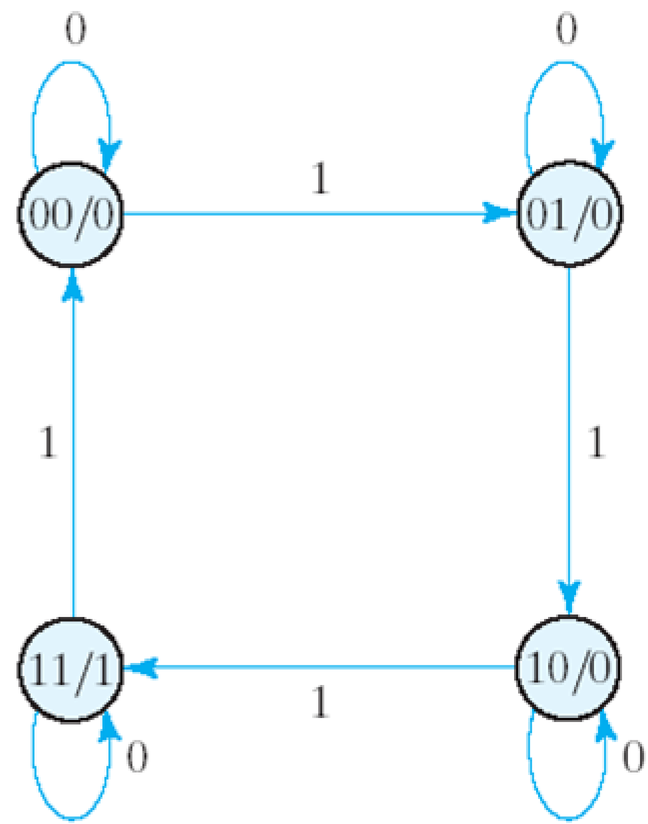
00/0: $A = 0,\ B = 0,\ y = 0$

on $x = 1$:

$$A(t+1) = 0,\ B(t+1) = 1,\ y = 0$$
$$\Rightarrow 00/0 \rightarrow 01/0$$

on $x = 0$:

$$A(t+1) = 0,\ B(t+1) = 0,\ y = 0$$
$$\Rightarrow 00/0 \rightarrow 00/0$$



State Reduction and Assignment

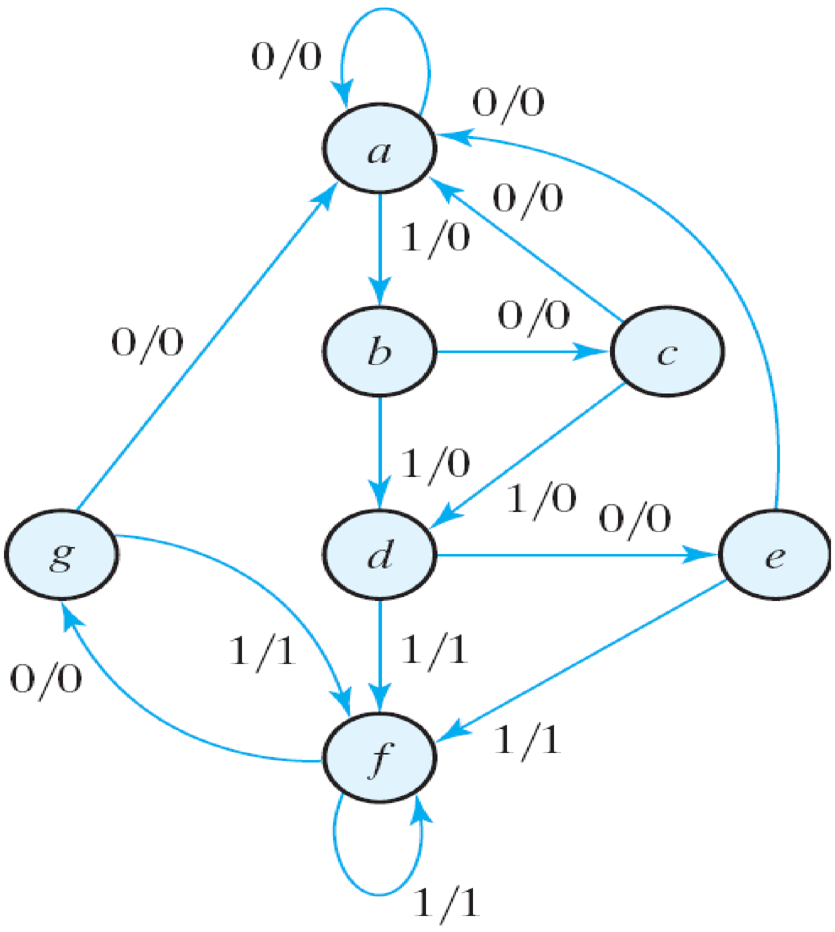
State Reduction and Assignment

- Two sequential circuits may exhibit the same input-output behavior, but have a different number of **internal states (flip-flops)** in their state diagram.
- Reducing the number of internal states may simplify a design. The reduction in the number of flip-flops in a sequential circuit is referred to as **state-reduction** problem

- If identical input sequences are applied to the two circuits and identical outputs occur for all input sequences, then the two circuits are said to be **equivalent** (as far as the input-out is concerned) and one may be replaced by the other.
- The **problem of state reduction** is to find ways of reducing the number of states in a sequential circuit without altering the input-output relationship.

- Two states are said to be **equivalent** if for each member of the set of inputs, they give exactly the same output and send the circuit either to the same state or to an equivalent state.
- When two states are equivalent one of them can be removed without altering the input-output relationship.

Example – state reduction



Example – state reduction

State Table

Present State	Next State $x = 0$	Next State $x = 1$	Output $x = 0$	Output $x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

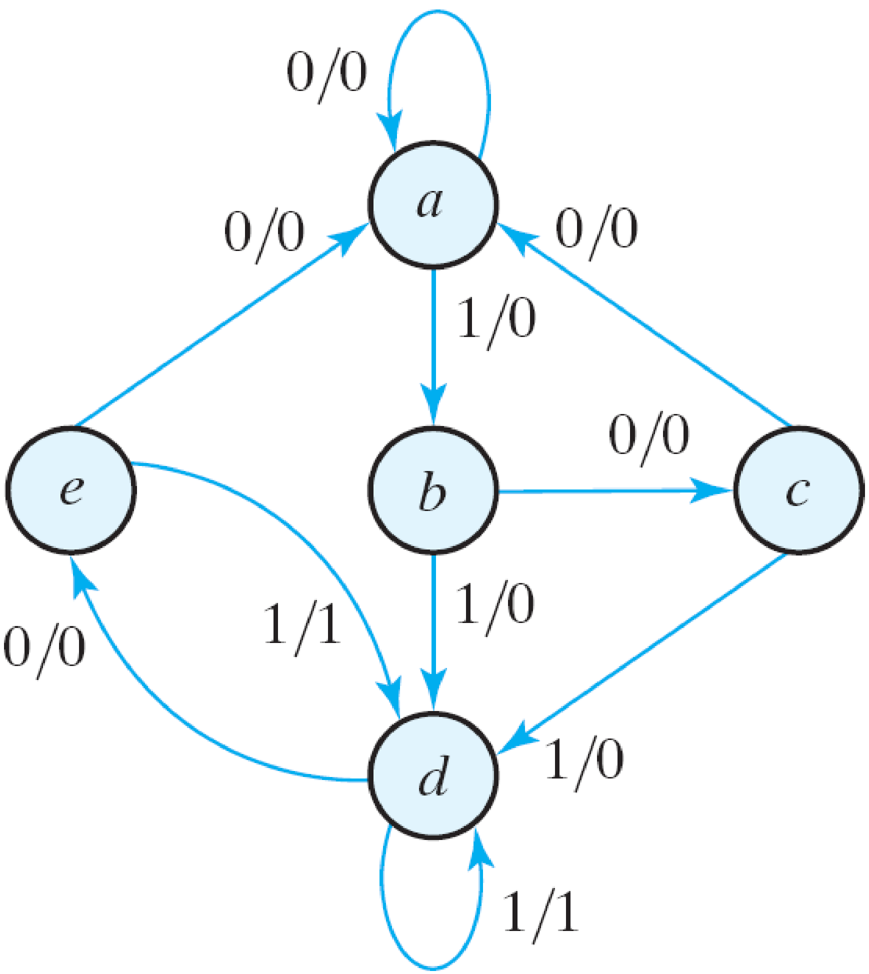
Reducing the State Table

	Next State		Output	
Present State	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

Reduced State Table

	Next State		Output	
Present State	**$x = 0$**	**$x = 1$**	**$x = 0$**	**$x = 1$**
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

- **Reduced state diagram**



State assignment

- In order to design a sequential circuit with physical components, it is necessary to assign unique coded binary values to the states.
- For a circuit with ***m* states**, the codes must contains ***n* bits**, where $m \leq 2^n$
- Unused states are treated as don't care conditions during the design.

Design procedure

Design procedure

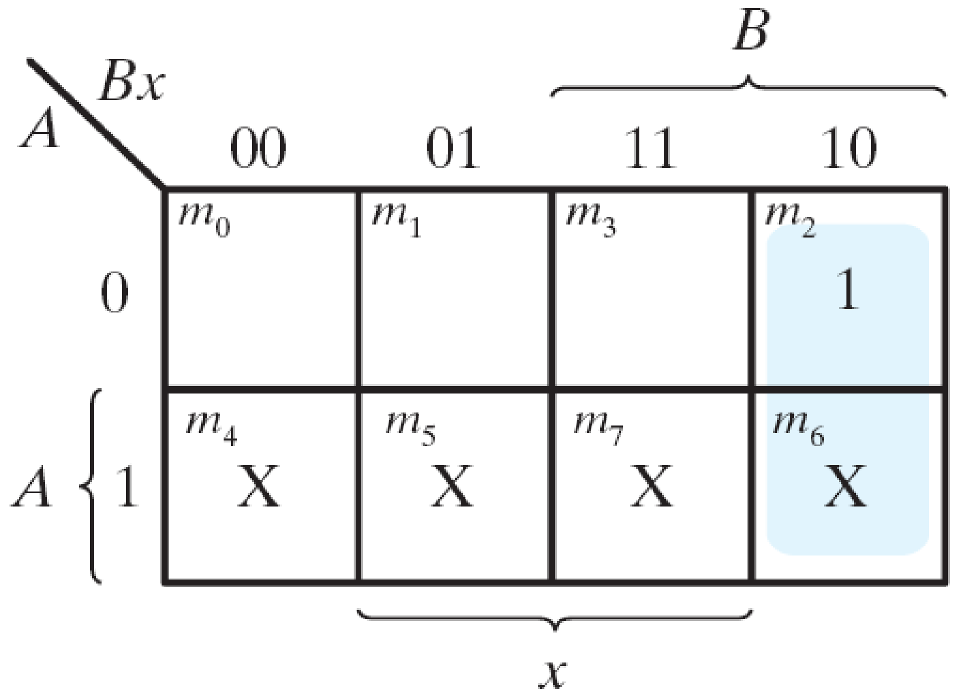
The procedure for designing **synchronous sequential circuits** can be summarized by a list of recommended steps:

1. From specification of the desired operation, **derive a state diagram for the circuit**.
2. Reduce the number of states if necessary.
3. Assign binary values to the states.
4. Obtain the **binary-coded state table** (transition table).
5. Choose the **type of flip-flops** to be used.
6. Derive the simplified **flip-flop input equations** and **output equations**.

7 Draw the **logic diagram**.

Synthesis using *JK* flip-flops

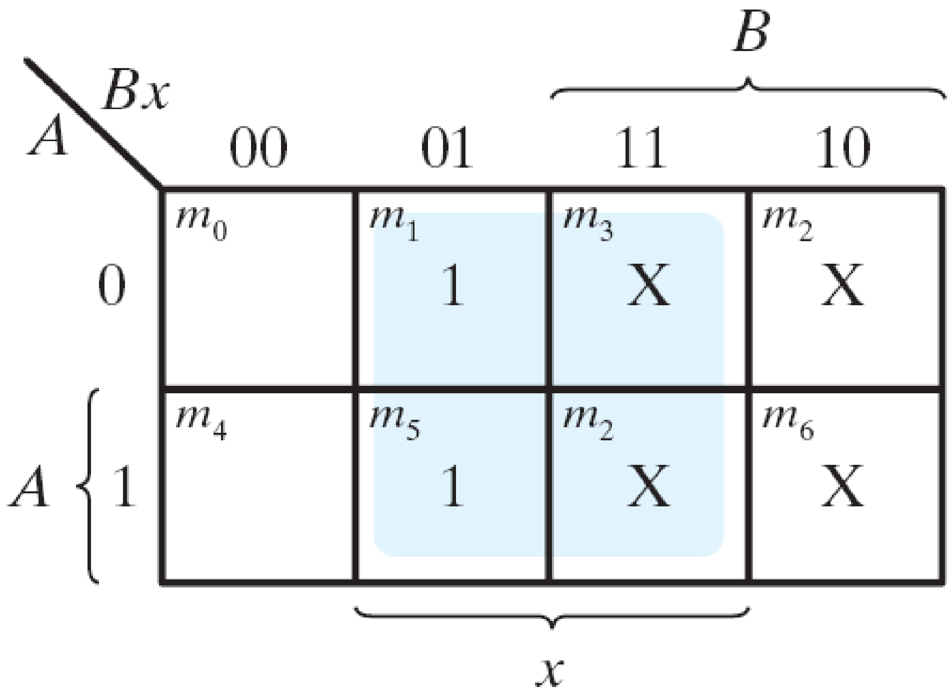
Present State		Input	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1



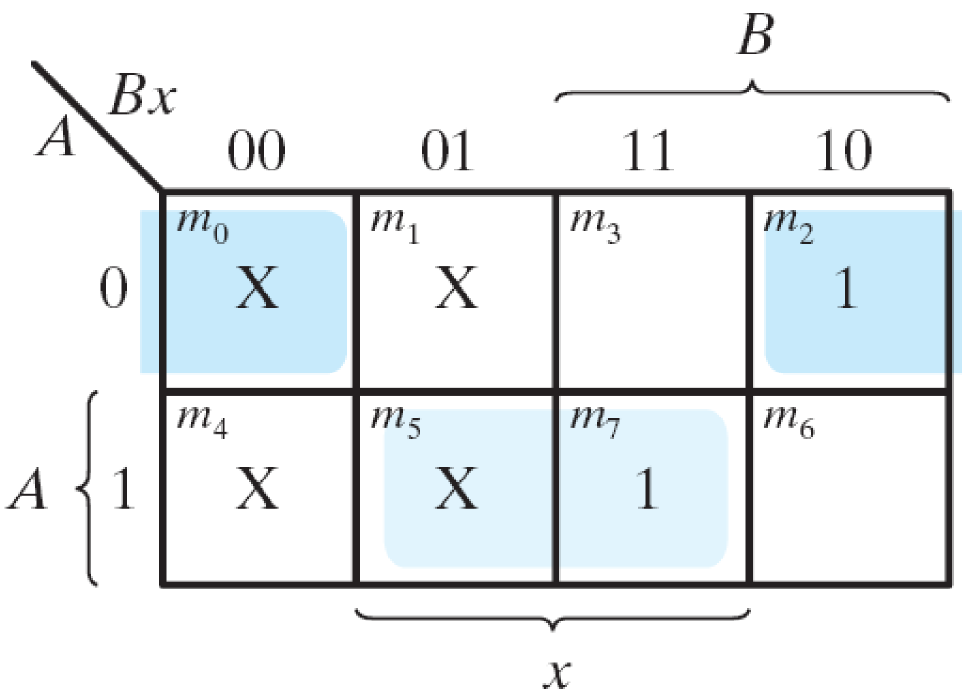
$J_A = Bx'$

$A \backslash Bx$	00	01	11	10
0	m_0 X	m_1 X	m_3 X	m_2 X
1	m_4	m_5	m_7 1	m_6

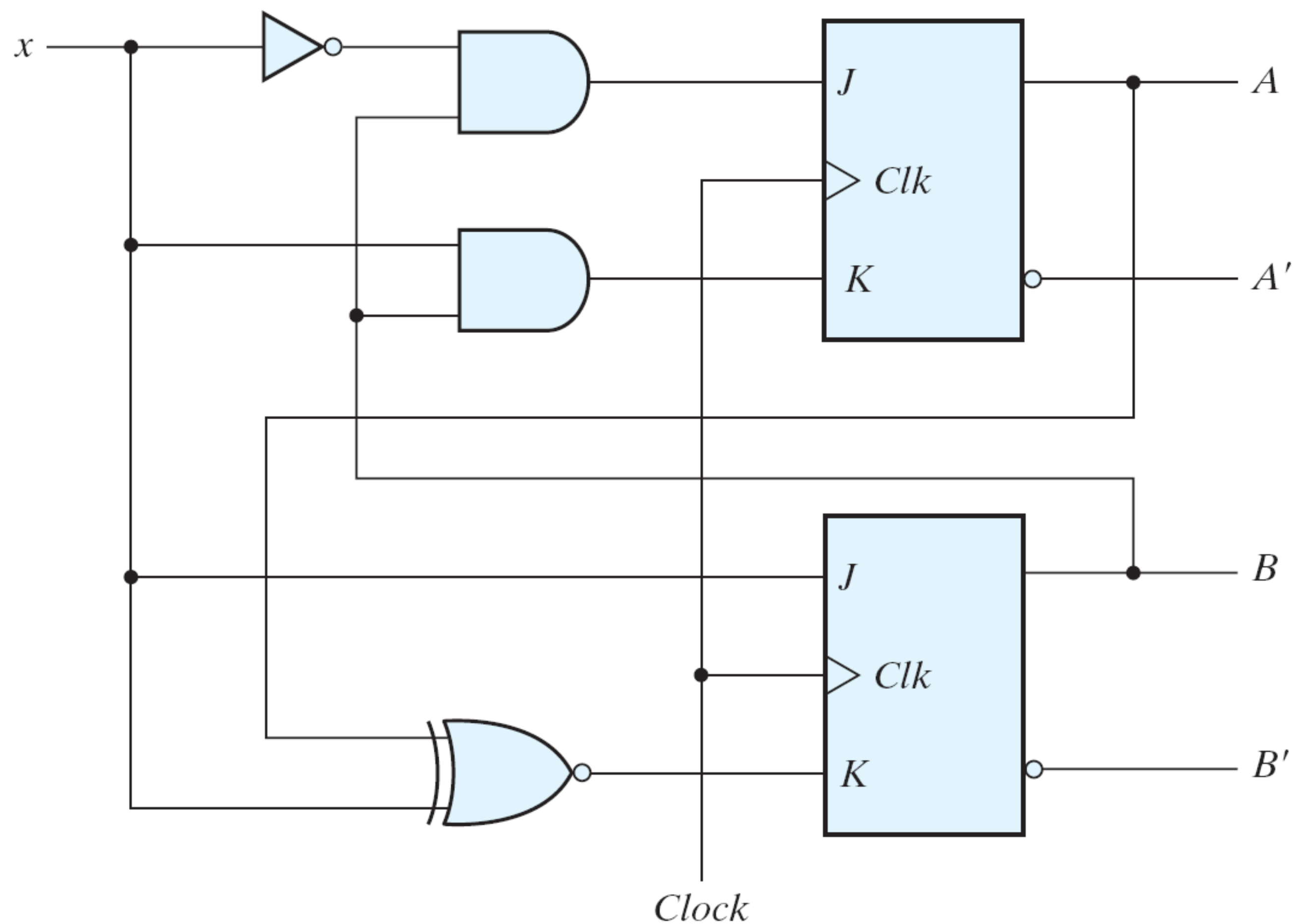
$$K_A = Bx$$



$$J_B = x$$



$$K_B = (A \oplus x)'$$


x
J
Clk
K
A
A′
J
Clk
K
B
B′
Clock