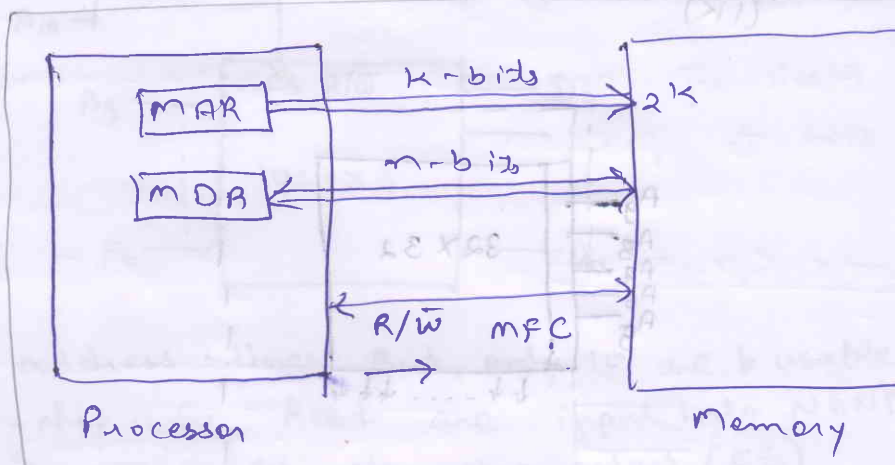
March 3, 2020

Memory System (Hamacher, CH-5)

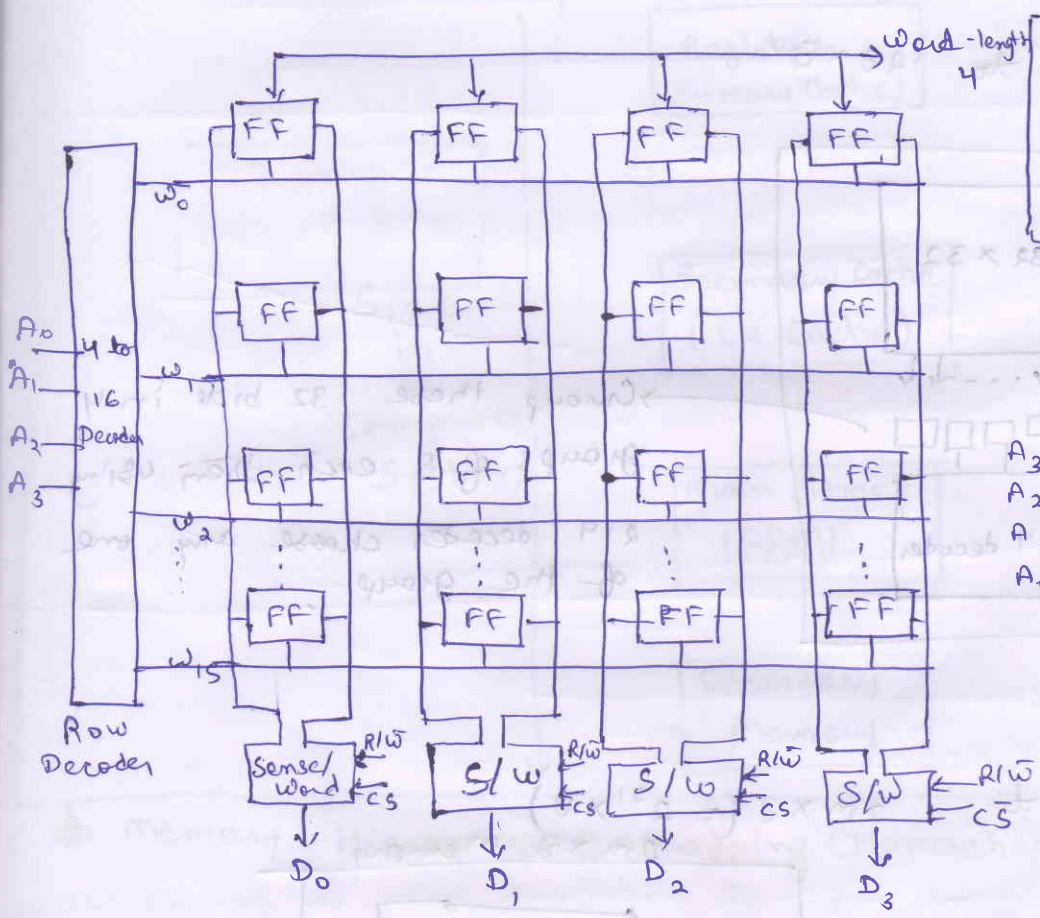


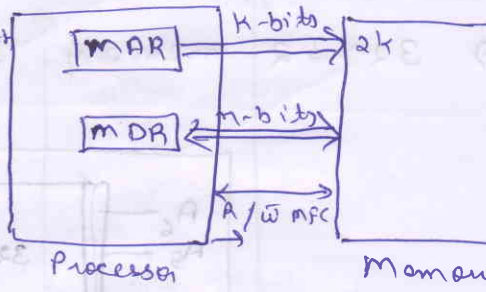
R/W : Read / Write. (known as RD/WR signal)

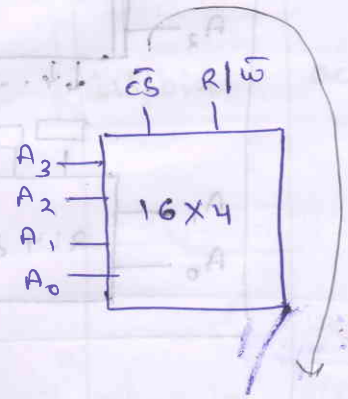
★ MFC: Memory Function Complete.

n = word-length

Internal Organization of Memory:-

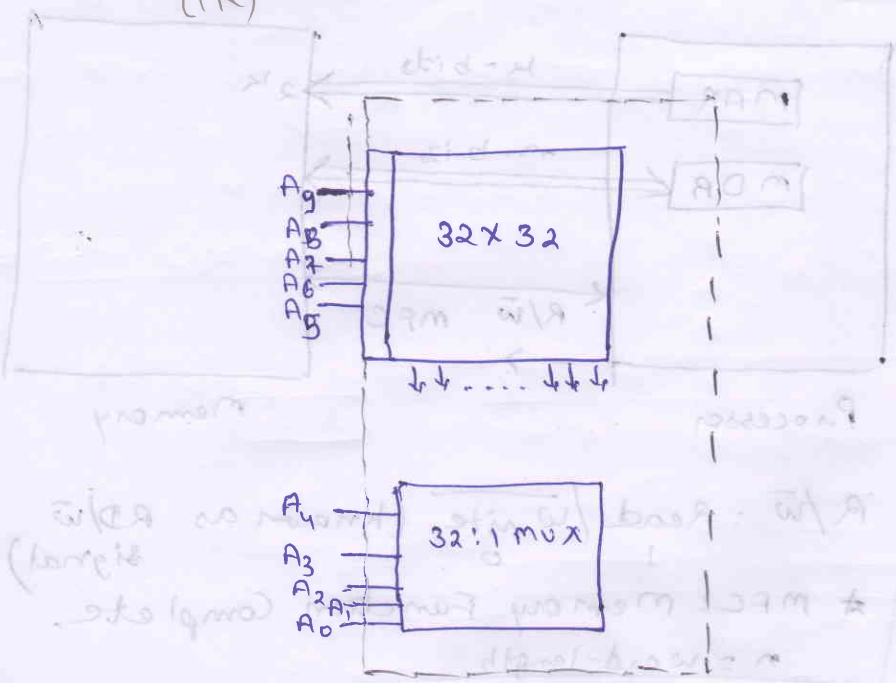




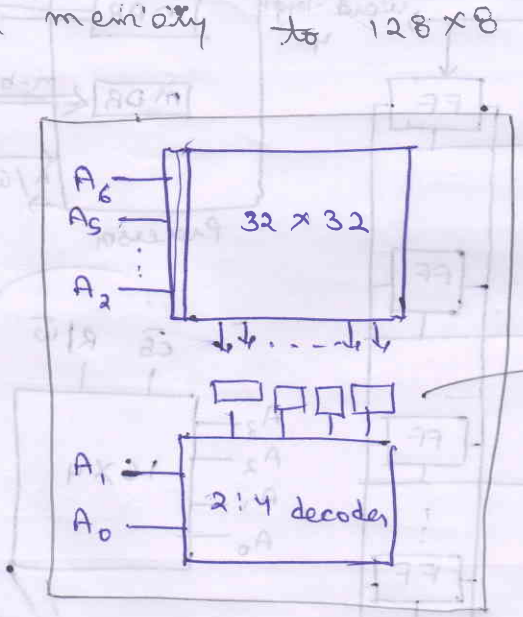


Chip-select: (Comes into picture when many memo blocks are joined.

→ 32×32 (1K) memory to 1024×1 :-



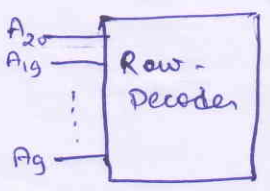
→ 32×32 memory to 128×8

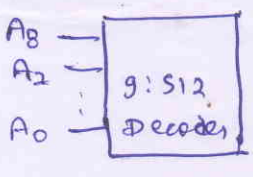


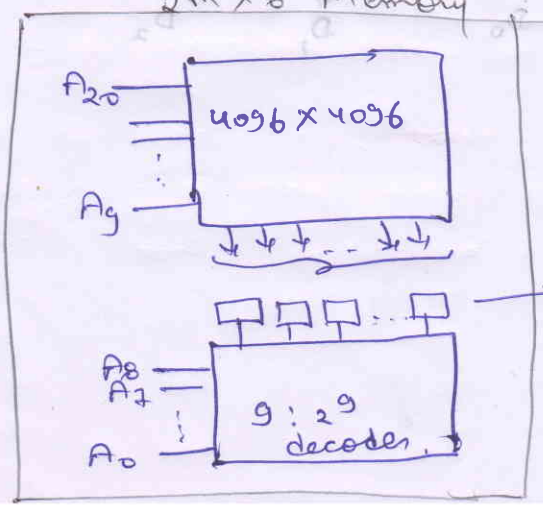
→ Group these 32 bit
groups of 8 each the
2:4 decoder choose a
of the group

→ 4096 × 4096 to $2^{12} \times 2^{12}$ $2^m \times 8 \left(= 2^{21} \times 8\right)$

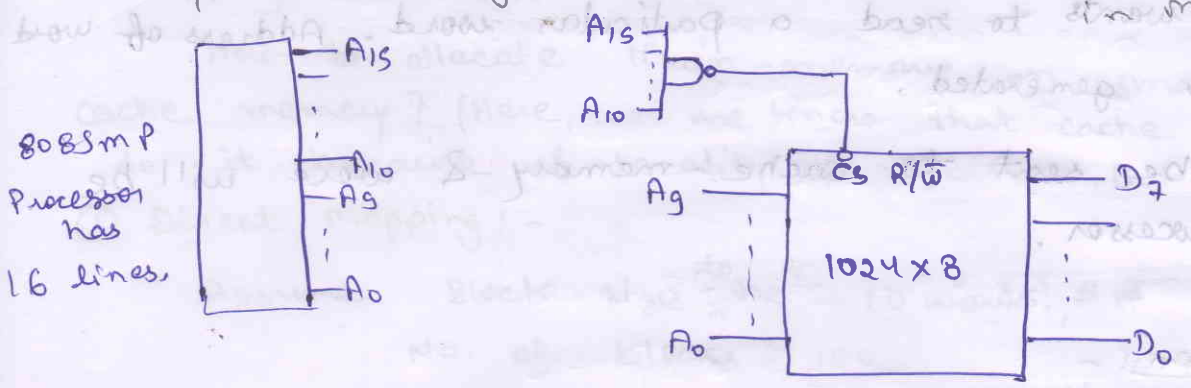
2m×8 memory







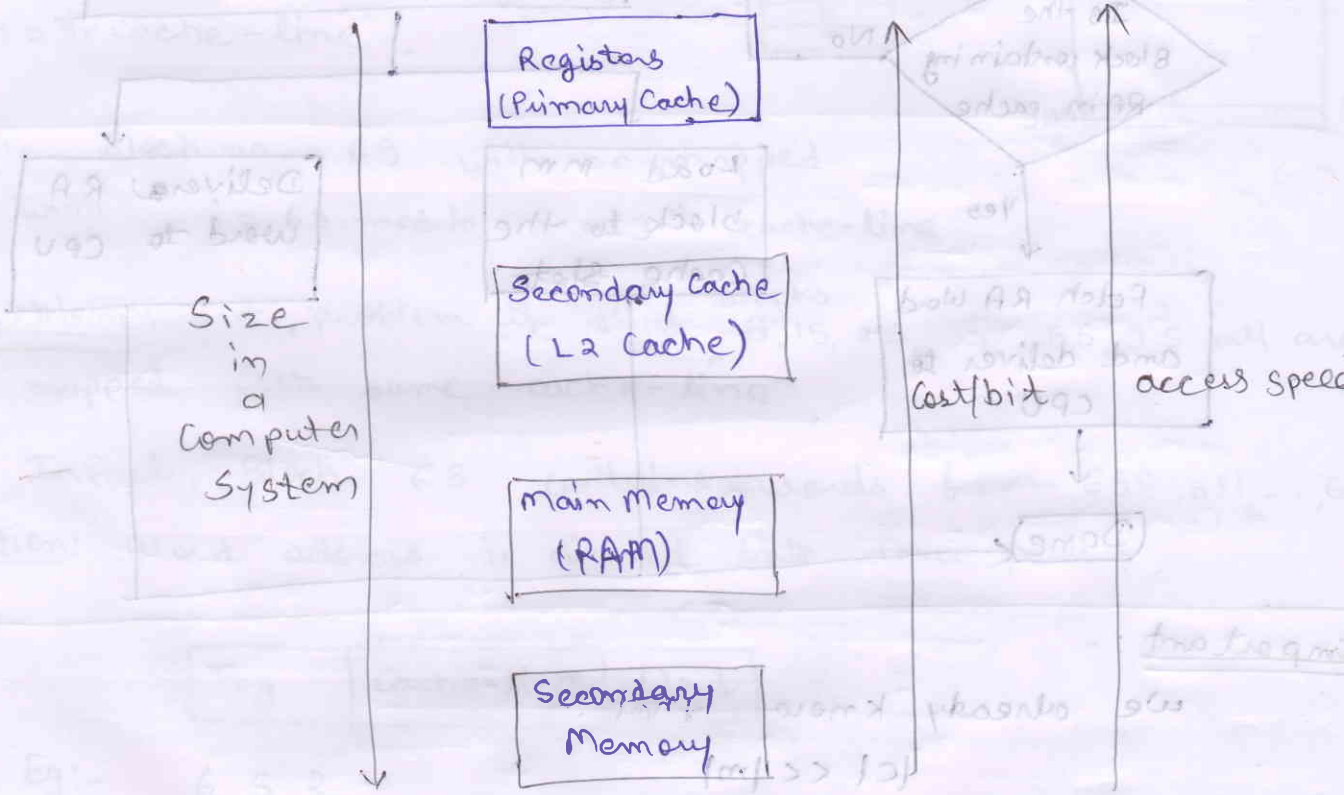
Memory - Interfacing :- (Not in syllabus now, It will be covered in microprocessor subject).



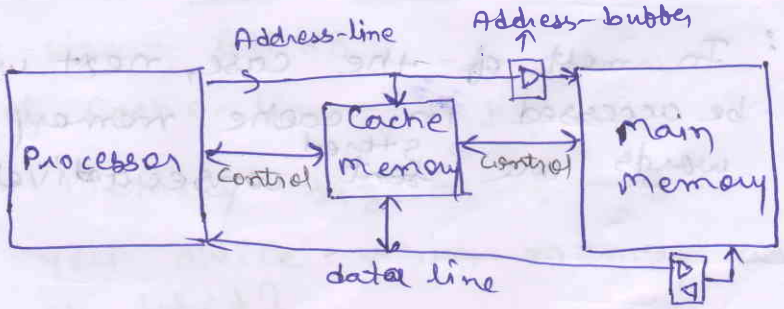
* As there are 16 address-lines, But, only 10 are usable for 1024x8 memory-chip. So, Rest are input into NAND gate & its output is connected to chip-select (CS).

March 4th, 20

Memory Hierarchy :-



Memory Hierarchy & Mapping (Hamacher / Stallings) :-



$|C| << |M|$

⇒ Size of << Size of