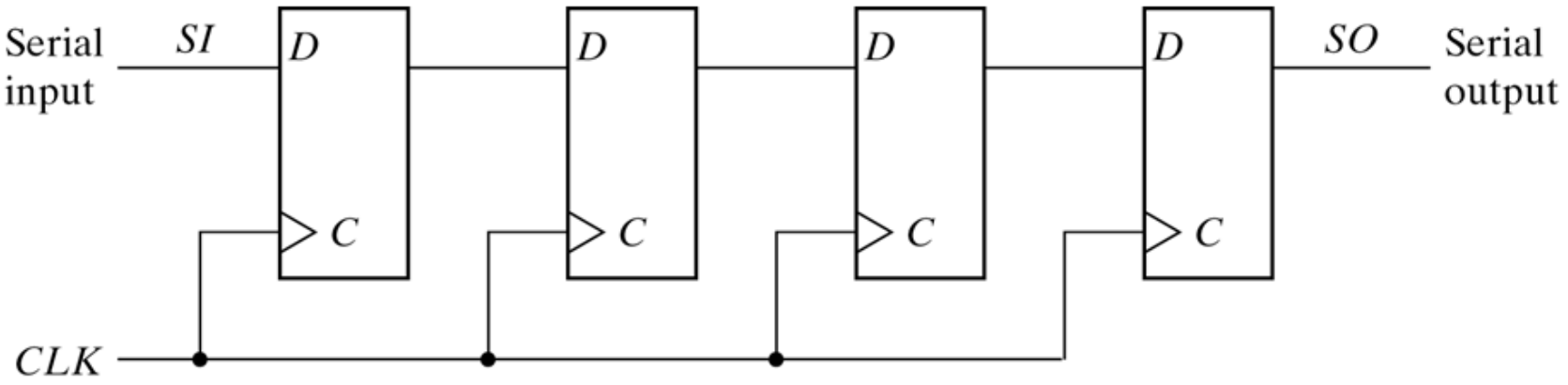
Shift Register

Shift Registers

- A register capable of shifting its binary information in one or both direction is called a *shift register*.
- All flip-flops receive common clock pulses, which activate the shift from one stage to the next.
- The simplest possible shift register is one that uses only flip-flops


Serial input
SI
D
C
D
C
D
C
D
C
SO
Serial output
CLK

- Each clock pulse shifts the contents of the register one bit position to the right.
- The *serial input* determines what goes into the leftmost flip-flop during the shift.
- The *serial output* is taken from the output of the rightmost flip-flop.

Shift Register types

- Shift Register types:
  - Serial-in, serial-out
  - Serial-in, parallel-out
  - Parallel-in, serial-out
  - Parallel-in, parallel-out
  - Bidirectional Shift Registers
- Special Shift Counters

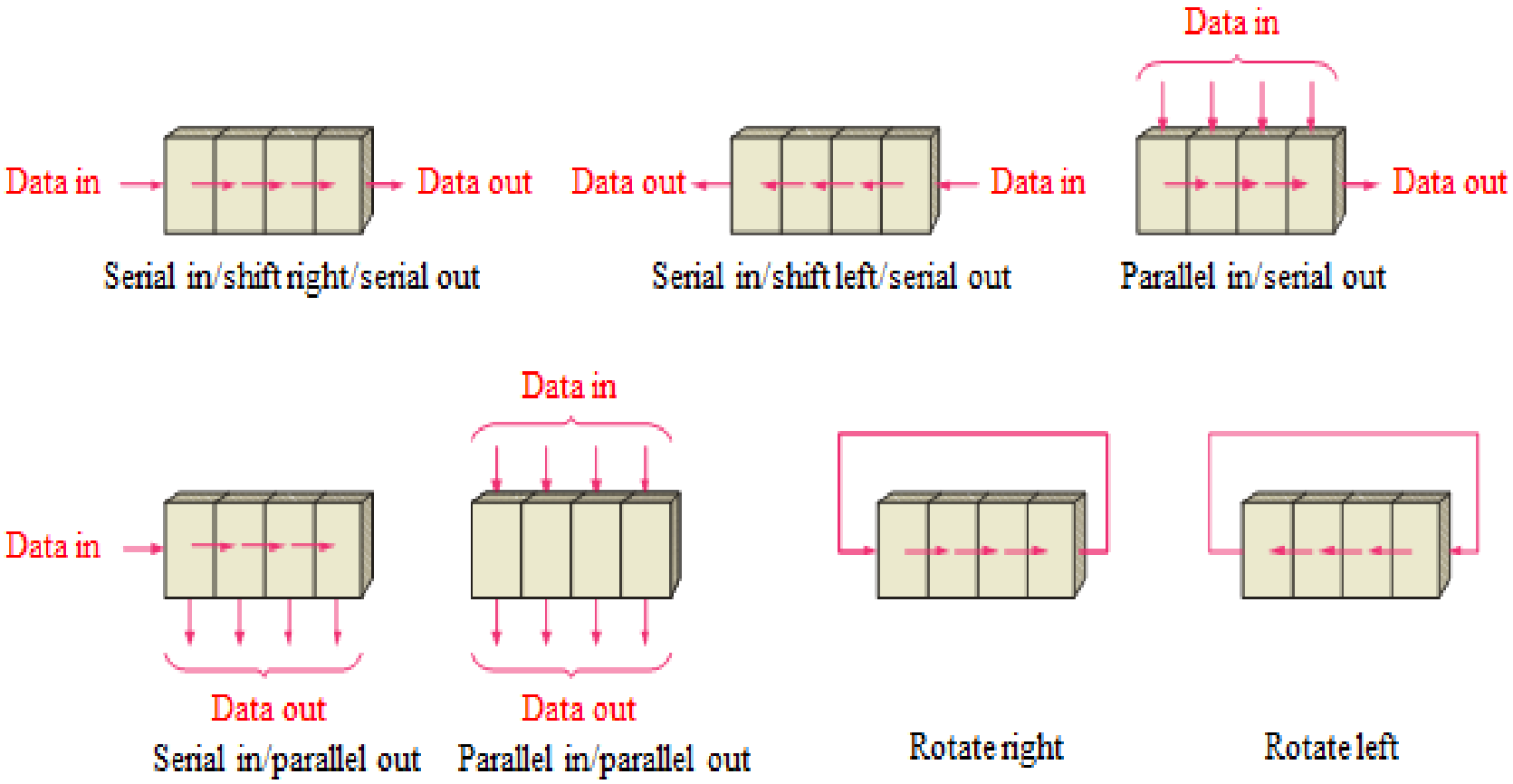
  Ring Counters and Johnson Counter

Serial transfer and parallel transfer

The difference between serial transfer and parallel transfer is:

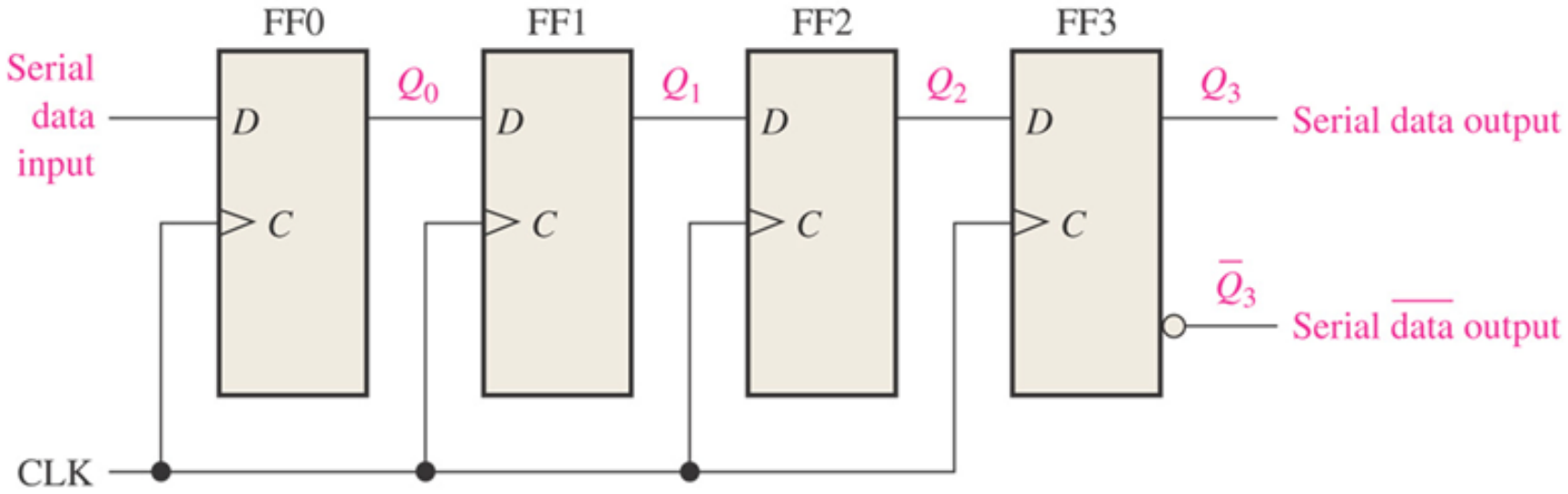
- In the parallel mode information is available from all bits of register and all bits can be transferred simultaneously during one clock pulse.
- In the serial mode, the registers have a single serial input and a single serial output. The information is transferred one bit at a time while registers are shifted in the same direction

- Basic data movements are:

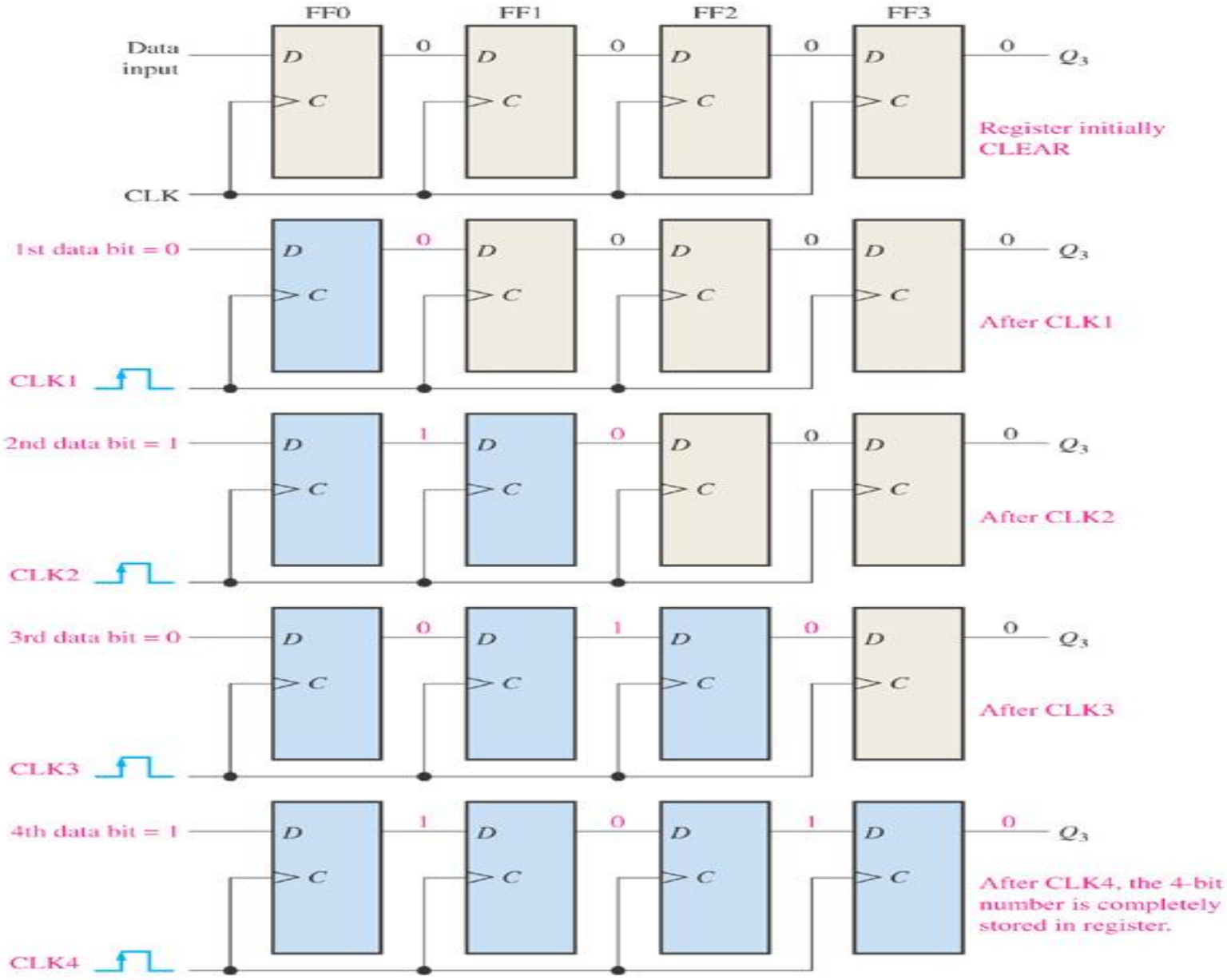


Serial-in/Serial out Shift Register

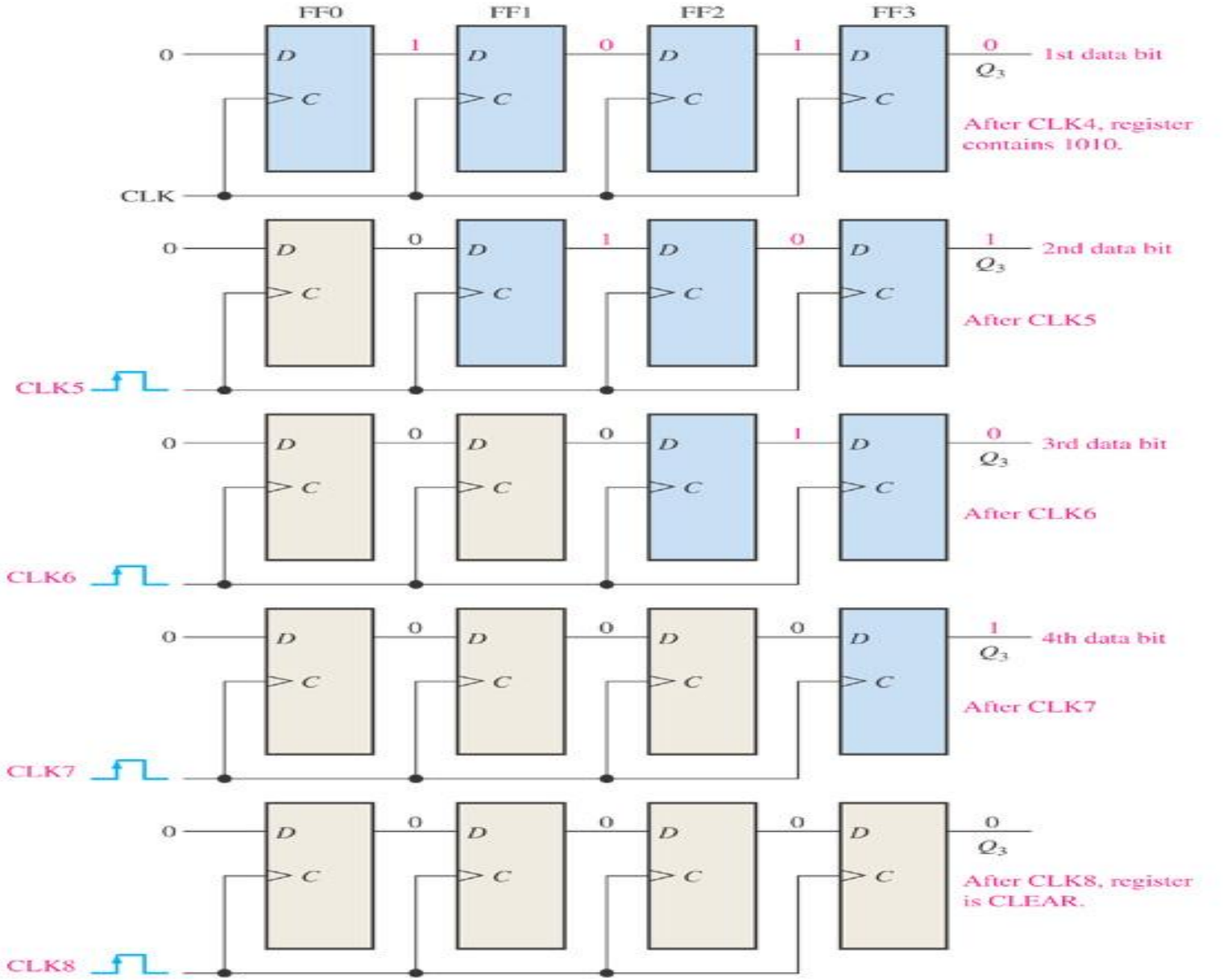
A **Serial In Serial Out** shift register has a single input and a single output



With four stages, this shift register can store up to four bits of data.



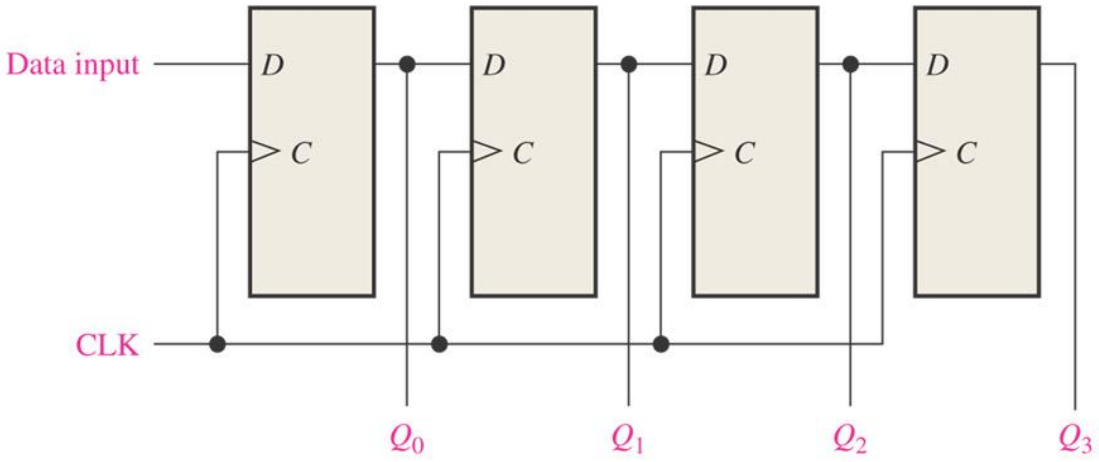
Four bits (1010) being entered serially



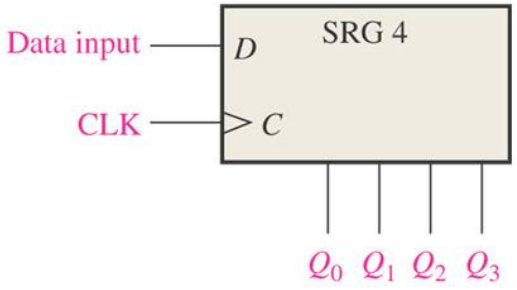
Four bits (1010) being serially shifted out and replaced by all zeros.

Serial In/Parallel Out Shift Registers

A Serial In Parallel Out shift register has a single input and access to all outputs

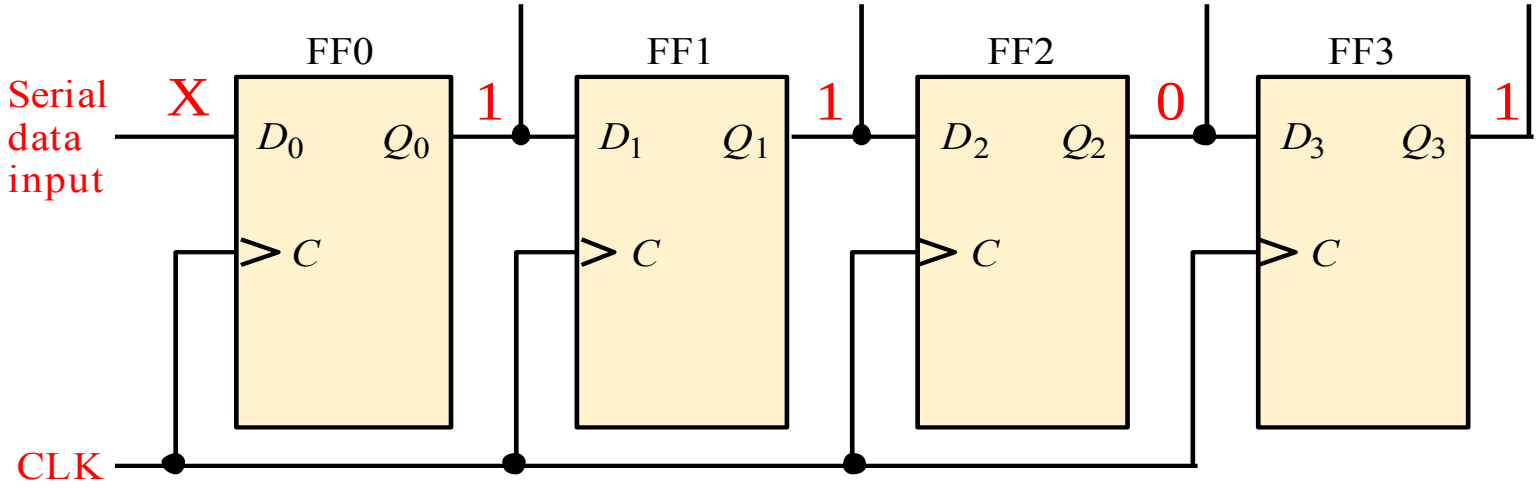


(a)



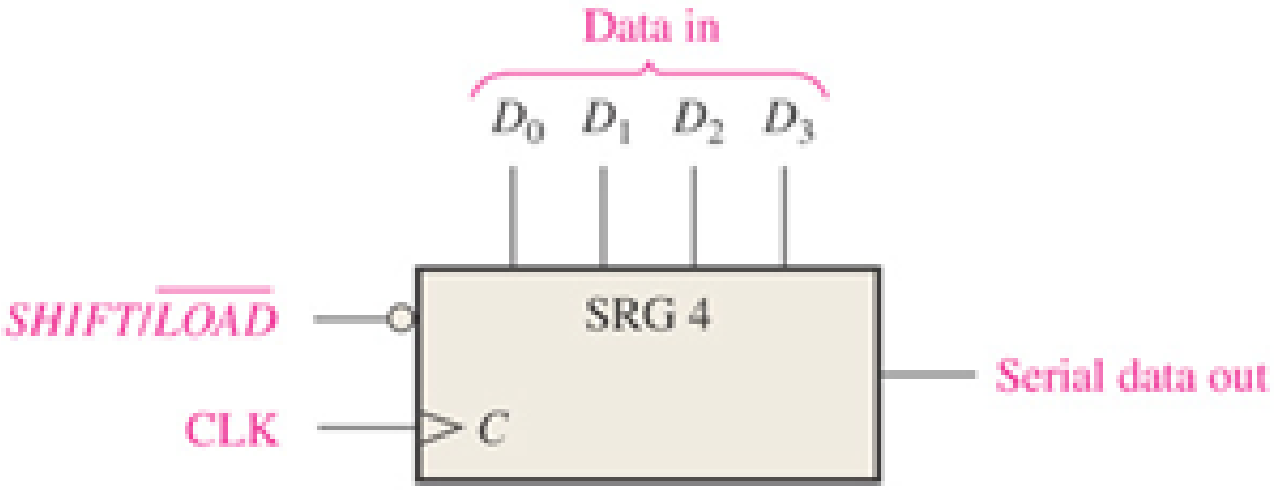
(b)

- 4-bit serial in/parallel out shift register
- For example, assume the binary number 1011 is loaded sequentially, one bit at each clock pulse.

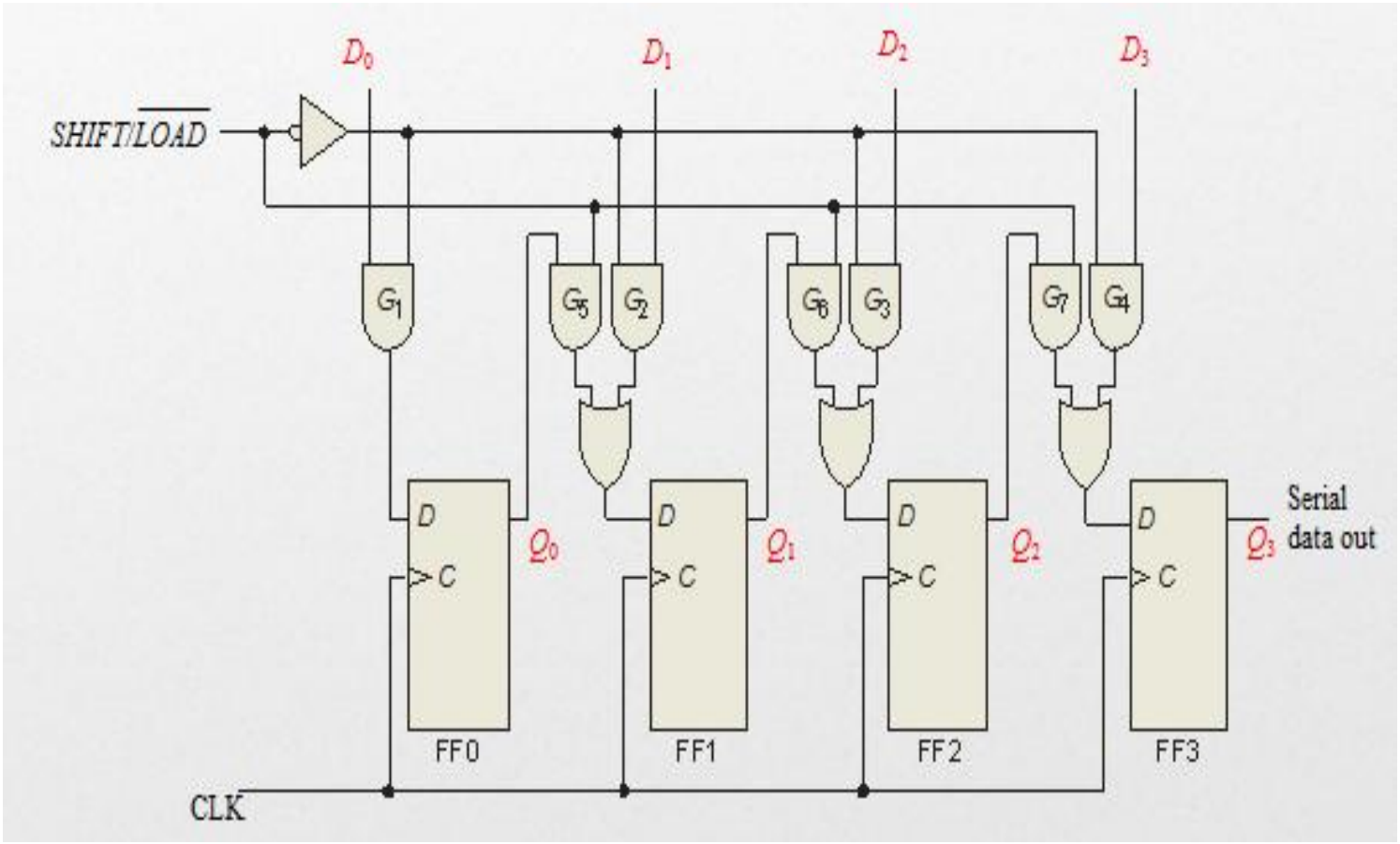


Parallel-In, Serial-Out Shift Register

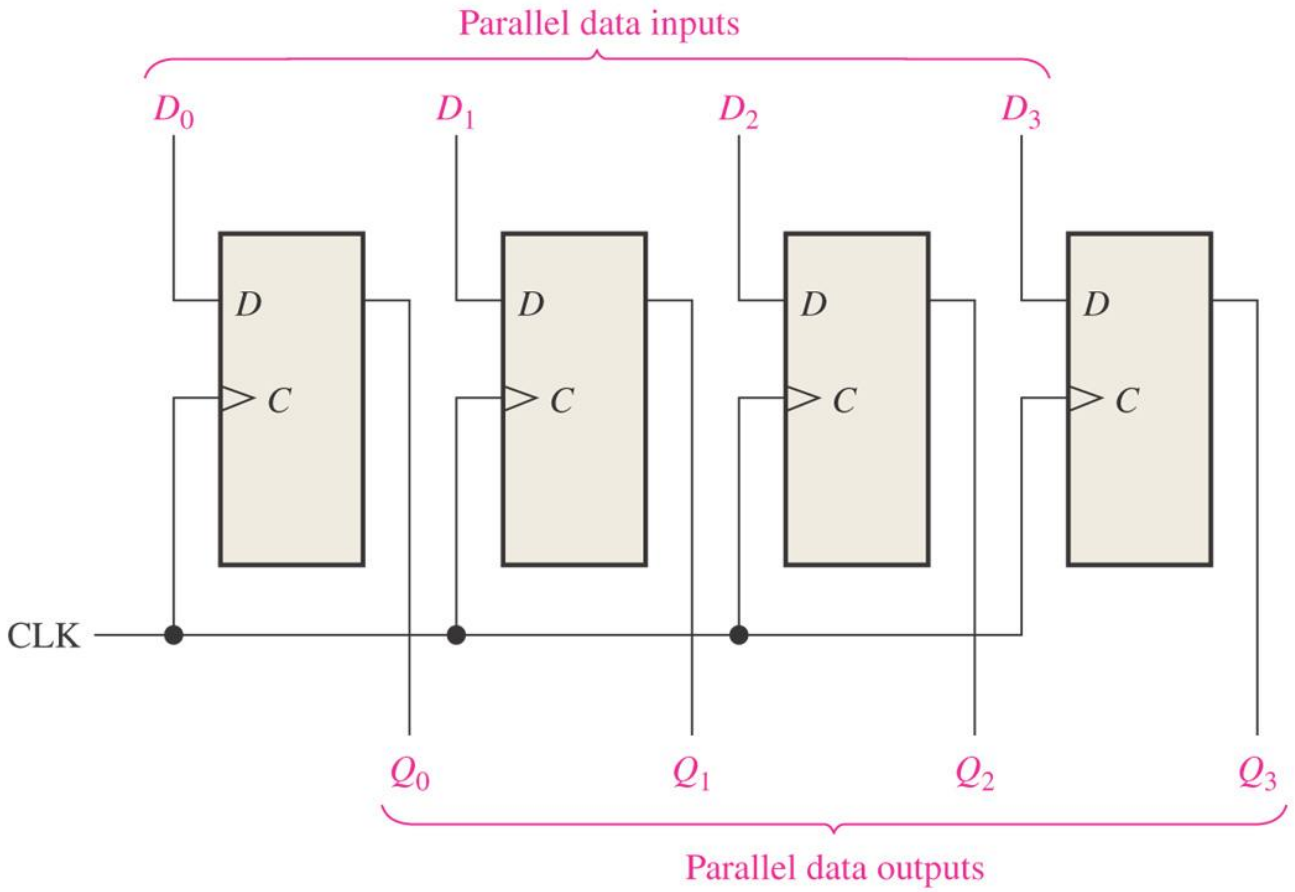
- Shift registers can be used to convert parallel data to serial form



- The bits are entered simultaneously into their respective stages.
- The serial output appears bit by bit per clock pulse.
- To store 4 bits, we need 1 clock pulse
- To shift them out them, we need another 3 clock pulses.

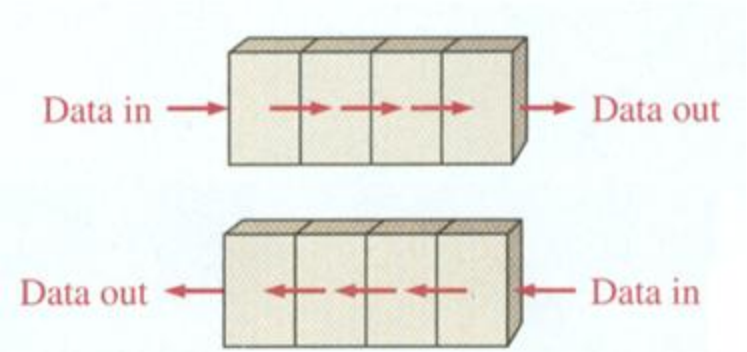

D_0
D_1
D_2
D_3
SHIFT/$\overline{LOAD}$
G_1
G_5
G_2
G_6
G_3
G_7
G_4
D
C
Q_0
Q_1
Q_2
Q_3
FF0
FF1
FF2
FF3
Serial data out
CLK

Parallel-In, Parallel-Out Shift Register

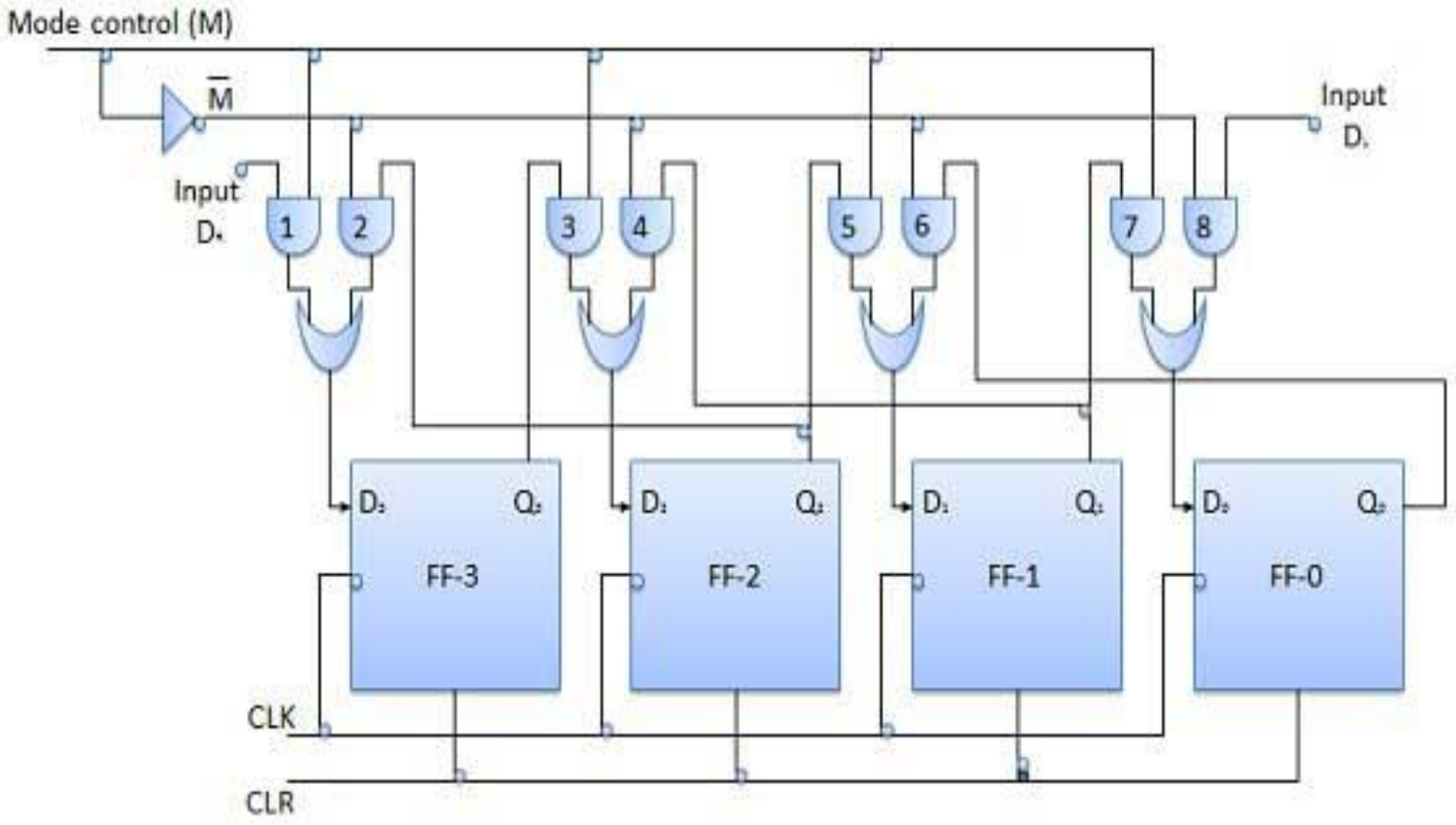


Bidirectional Shift Register

- A bidirectional shift register is one in which the data can be shifted either left or right.
- 4-bit version is given below.



Bidirectional 4-bit Shift Register



OPERATION

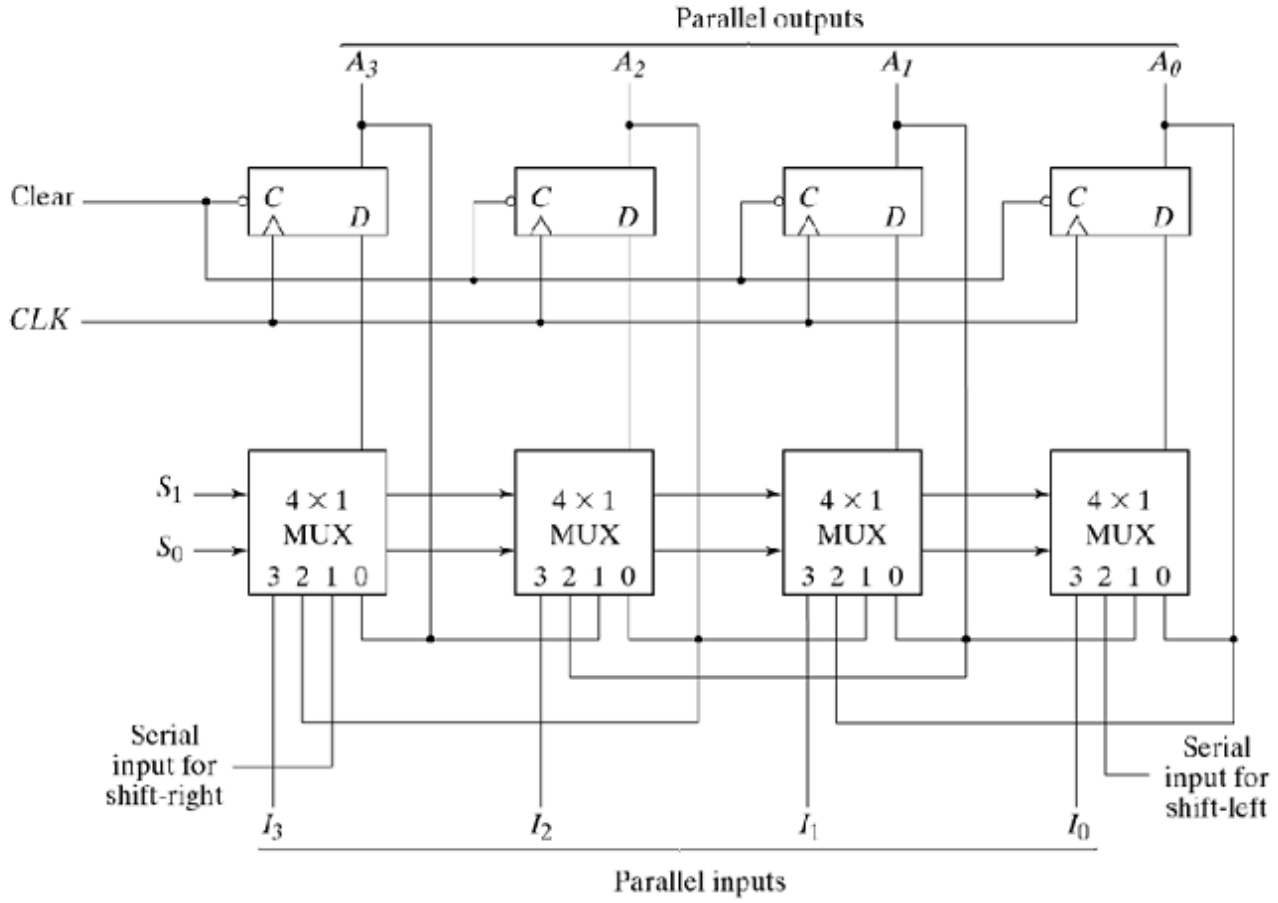
S.N.	Condition	Operation
1	With M = 1 : Shift right operation	▫ If M = 1, then the AND gates 1,3,5 and 7 are enable whereas the remaining AND gates 2,4,6 and 8 will be disabled. ▫ The data at D_R is shifted to right bit by bit from FF-3 to FF-0 on the application of clock pulses. Thus with M = 1 we get the serial right shift operation.
2	With M = 0 : Shift left operation	▫ When the mode control M is connected to 0 then the AND gates 2,4,6 and 8 are enabled while 1,3,5 and 7 are disabled. ▫ The data at D_L is shifted left bit by bit from FF-0 to FF-3 on the application of clock pulses. Thus with M = 0 we get the serial right shift operation.

Universal Shift Registers

- If the register has both shifts (right shift and left shift) and parallel load capabilities, it is referred to as universal shift register.
- A *clear* control to clear the register to 0.
- A *clock* input to synchronize the operations.
- A *shift-right* control to enable the shift operation and the *serial input* and *output* lines associated with the shift right.
- A *shift-left* control to enable the shift operation and the *serial input* and *output* lines associated with the shift left.

- A *parallel-load* control to enable a parallel transfer and the n input lines associated with the parallel transfer.
- n parallel output lines.
- A control state that leaves the information in the register unchanged in the presence of the clock.

4 bit Universal Shift Register



- Function Table

Mode Control		*Register* Operation
S_1	S_0	
0	0	No Change
0	1	Shift right
1	0	Shift Left
1	1	Parallel load

Shift Register Counters

- Shift registers can be used to show predefined sequence of states
- Two types;
  - Ring counter (Simple/Basic)
    - Normal output of the last flip flop is connected as input to the first flip flop (feed back)
  - Johnson Counter(Twisted Ring/Switch-tail)
    - Complemented output of the last flip flop is connected as input to the first flip flop (feed back)