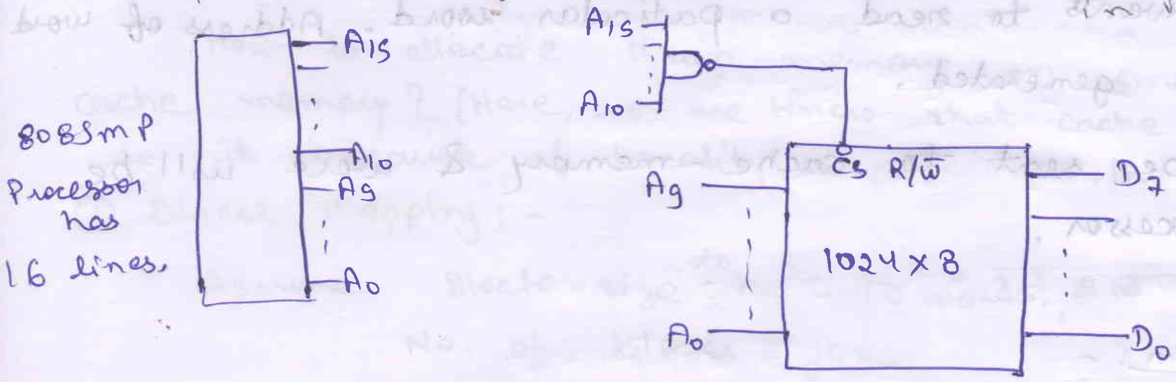
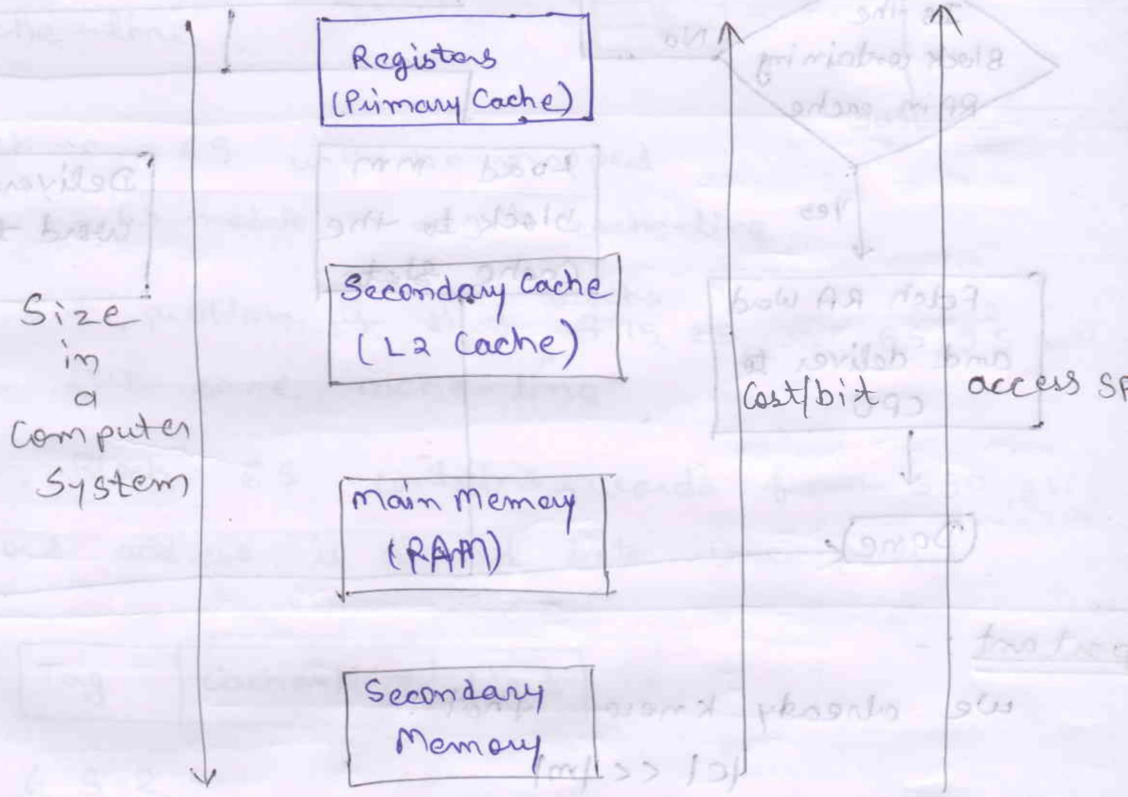
Memory - Interfacing :- (Not in Syllabus now, It will be cove in microproces subject),



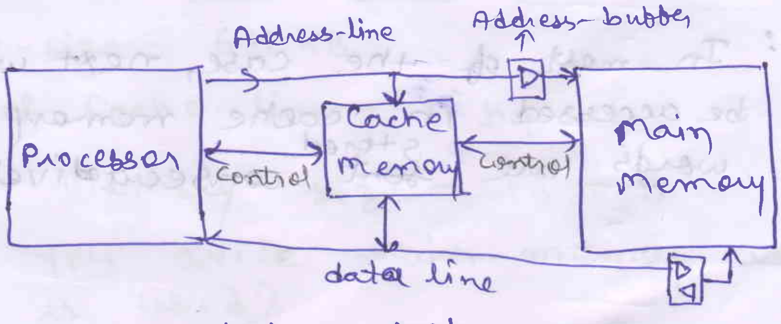
★ As there are 16 address-lines. But, only 10 are to be usal for 1024 x 8 memory-chip. So, Rest are input into NA gate & its output is connected to chip-select (CS),

Memory Hierarchy :-

March 4th,



Memory Hierarchy & Mapping (Hamacher / Stallings) :-



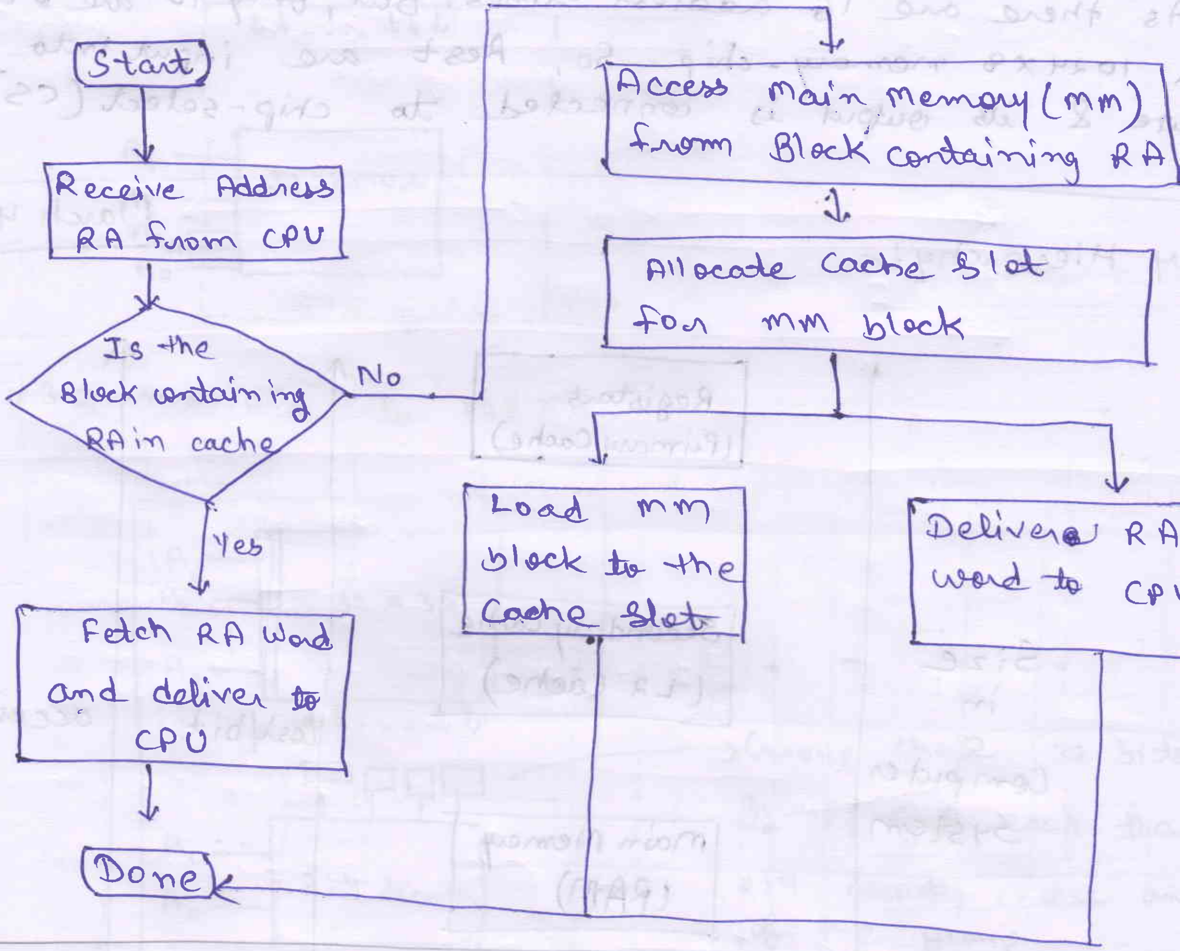
$|C| << |M|$

⇒ Size of cache memory << Size of

→ Processor wants to read a particular word. Address (i.e., '101') is generated.

→ Block will be sent to cache-memory & word wil sent to processor.

Cache Operation :-


Start
Receive Address RA from CPU
Is the Block containing RA in cache
No
Yes
Fetch RA Word and deliver to CPU
Done
Access main memory (mm) from Block containing RA
Allocate cache slot for mm block
Load mm block to the Cache slot
Delivers RA word to CP

Important :-

we already know that :-

$$|c| << |m|$$

- Locality of Reference :-
  - → Temporal : Some types of locations can be acc
  - → Spatial : In most of the case, next word be accessed in cache memory b words are stored consecutively.

→ Mapping scheme :-

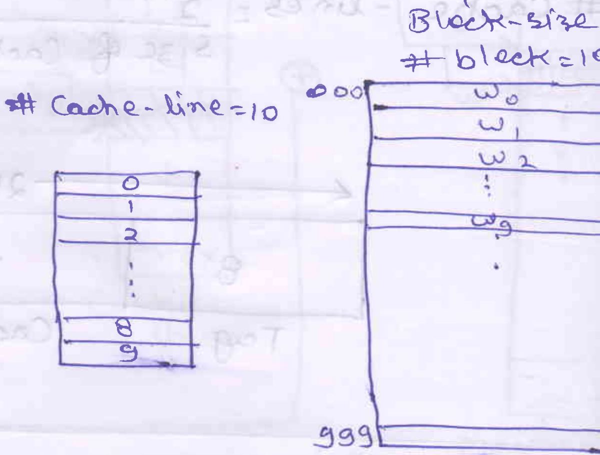
How to allocate Main-memory on smaller sized cache memory? (Here, we ~~are~~ know that cache memory do it because of locality of reference. But that is not topic no

① Direct Mapping :-

Assume Block-size to be 10 words, ~~& 10~~

No. of blocks = 100

& # cache-line = 10 (cache-line are blocks cache-memory



$\boxed{i = j \text{ modulo } m}$, where

i = Cache-line

j = main-memory block number

m = # cache-line.

Eg:- Block no. = 69 will be mapped with i = 69 modulo 10 = 9th cache-line.

Problem: But, problem is that blocks 5, 15, 25, .., 85, 95 all a mapped with same cache-line.

Infact, Block 65 contains words ~~from~~ 650, 651 ..

Solution: word address is divided into three parts :-

Tag	Cache-line	Word

Eg:- 6 5 2
Tag Cache line Word.

Eg:- Cache-size = 64 KB,

Size of Cache-line = 4 bytes

Main-memory size = 16 MB

How do you divide main-memory address if direct mapping is used?

Solution:-

Considering byte-addressable memory:-

16 MB = $2^4 \times 2^{20}$ bytes

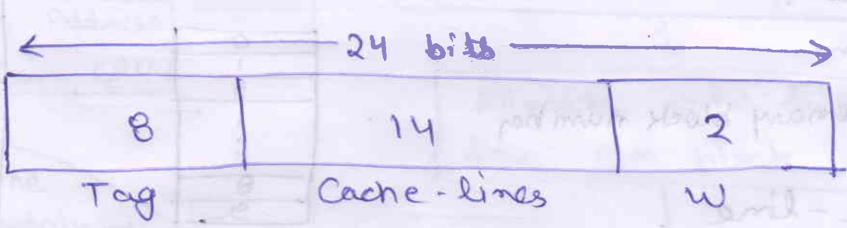
= 2^{24} bytes.

Cache-memory = 64 KB = $2^6 \times 2^{10}$ bytes

= 2^{16} bytes

(cache-line are blocks in cache-memory)

Cache-lines = $\frac{2^{16}}{\text{Size of Cache-line}} = \frac{2^{16}}{4} = 2^{14}$



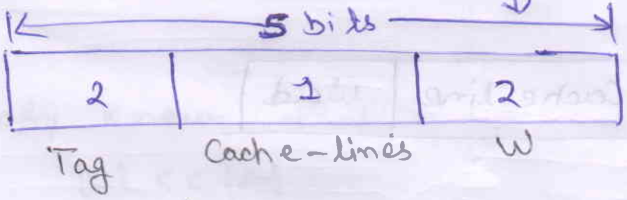
Eg:- mm = 32 bytes,

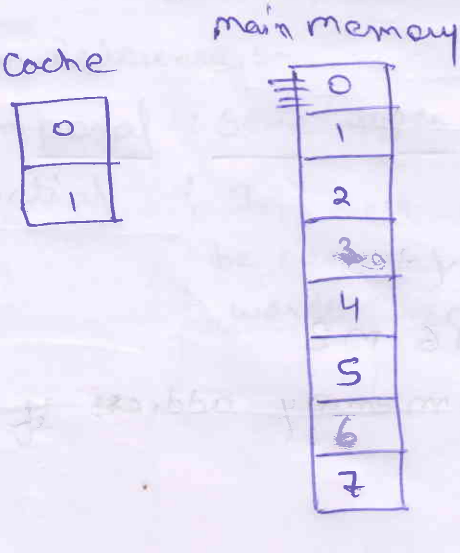
Cache-~~line~~ memory size = 8 bytes.

Block-size = 4 bytes = 2^{2}

mm = 2^5 bytes

Cache-lines = $\frac{8}{4} = 2^{1}$


5 bits
2
1
2
Tag
Cache-lines
W


cache
0
1
main memory
0
1
2
3
4
5
6
7