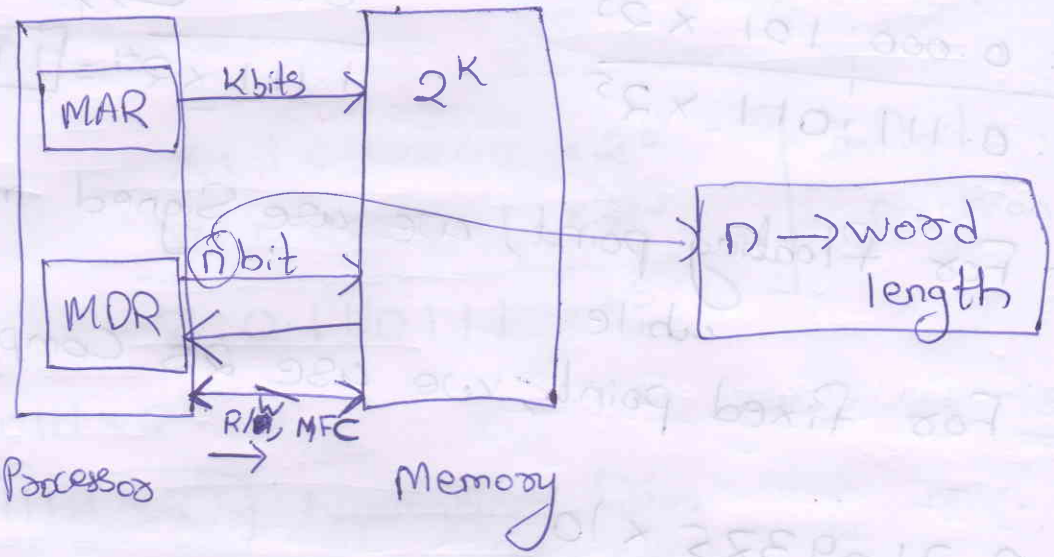
✡) Memory System (Hamacher, ch-5)
(Pls read from)



R/$\bar{W}$: Read 1 write 0 (Known as RD/$\bar{W}$ signal)

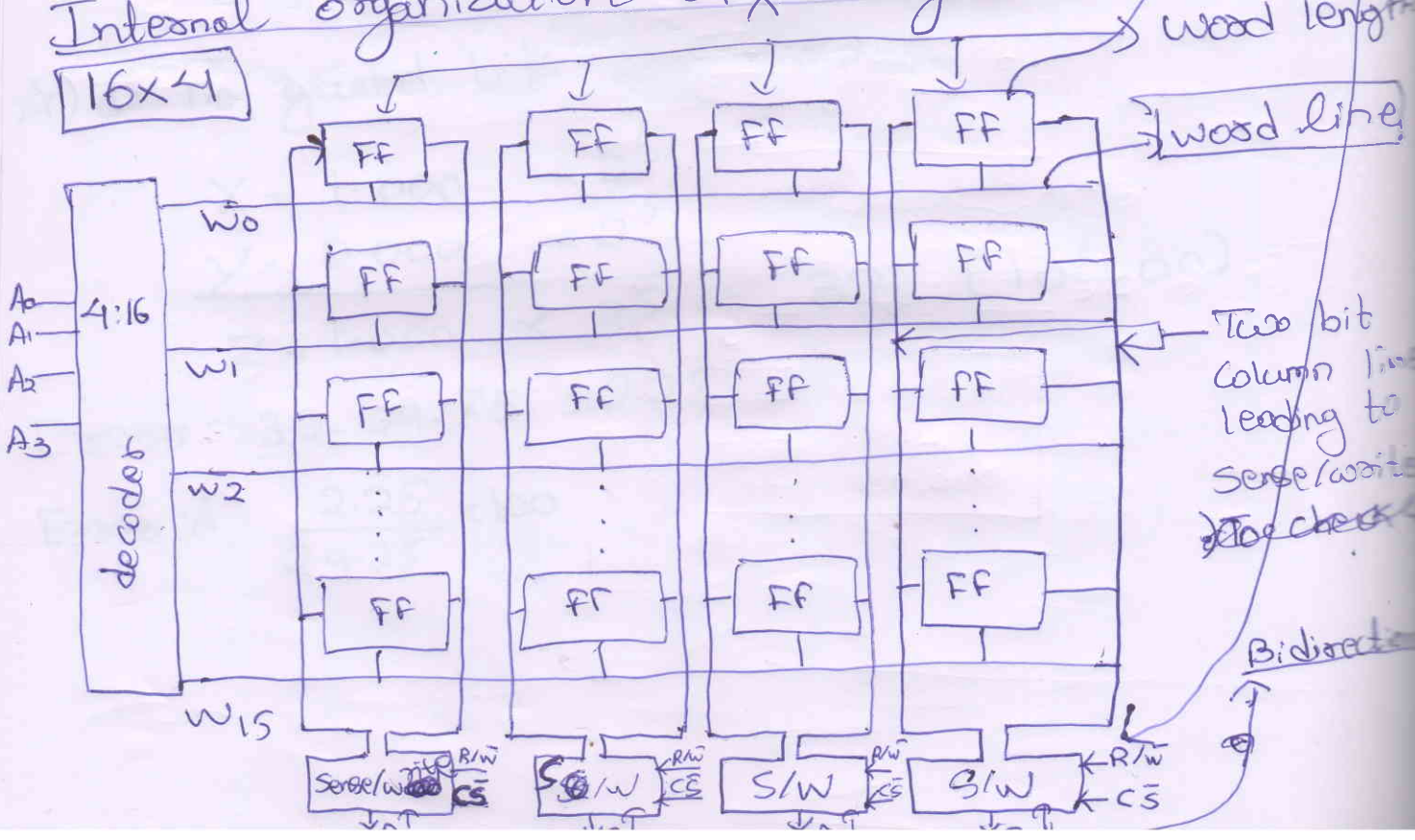
MFC : Memory function Complete

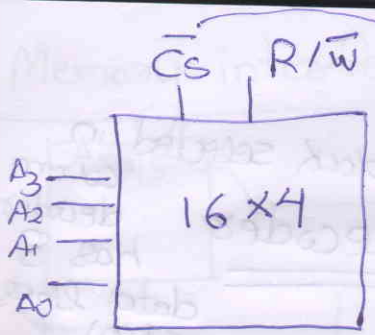
Basic structure of memory:-

memory cell

Internal organization of a memory chip:-

16×4

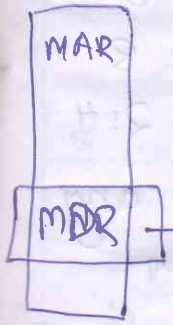




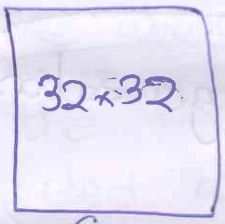
→ Chip select (comes into picture when many memory blocks are joined

• No of ext. connections: #address lines (4) + #data input/output lines (4) + (R/$\overline{W}$ and CS) (2) + (Ground and Power) (2)

= 4+4+2+2 = 12



→ This is connected to the last layer of chips



→ 1K memory

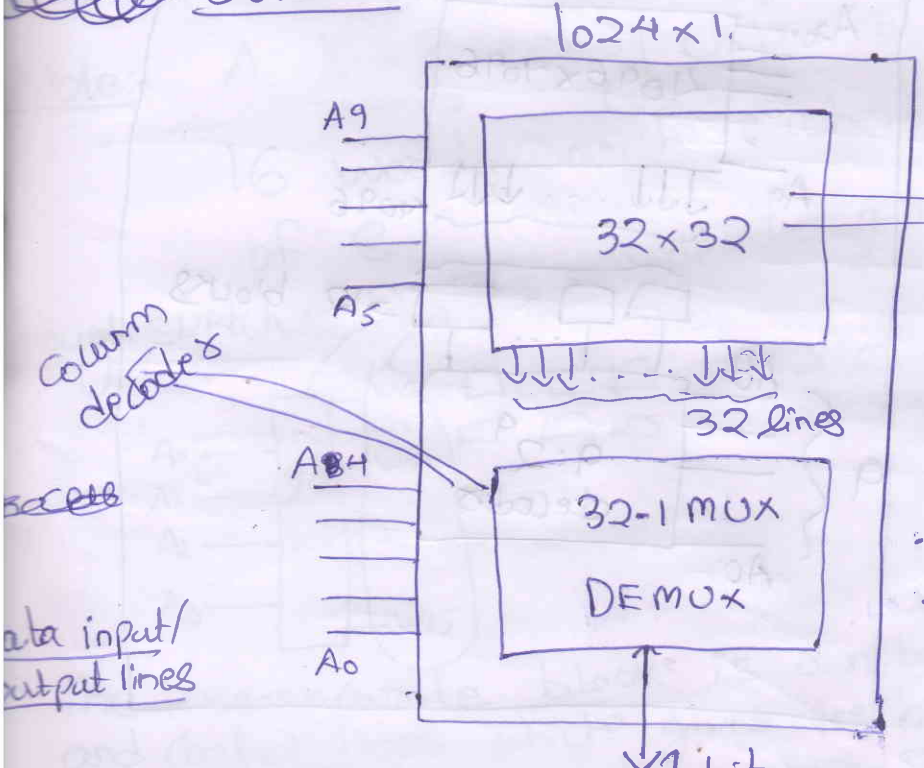
To convert into :-

1024 rows

Each row has 1 cell

1024 × 1

Solution :-



No of external connections

- Address lines :- 10
- Data input/out :- 1
- Read/write & CS : 2
- Power/Ground : 2

∴ 10+1+2+2

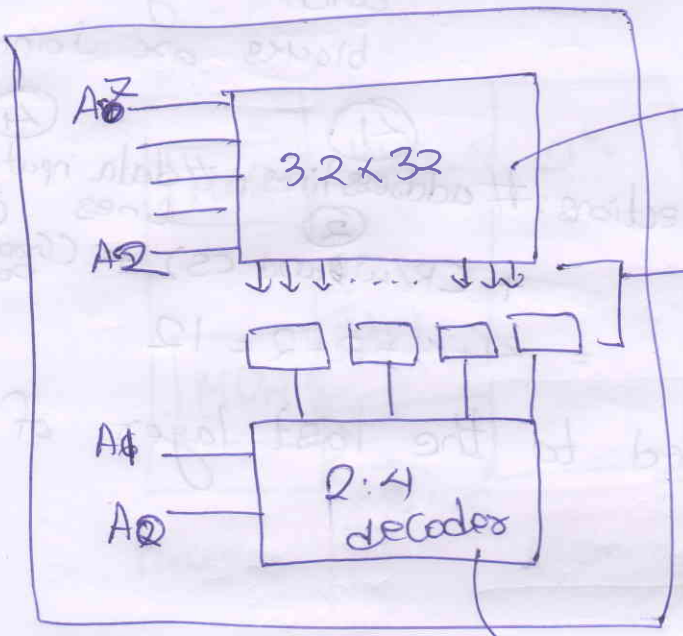
= (15)

•) To form 128×8 :-

No of external :

$7 + 8 + 2 + 2 = 19$

↳ As the block selected in column decoder has 8 data lines (I/O)

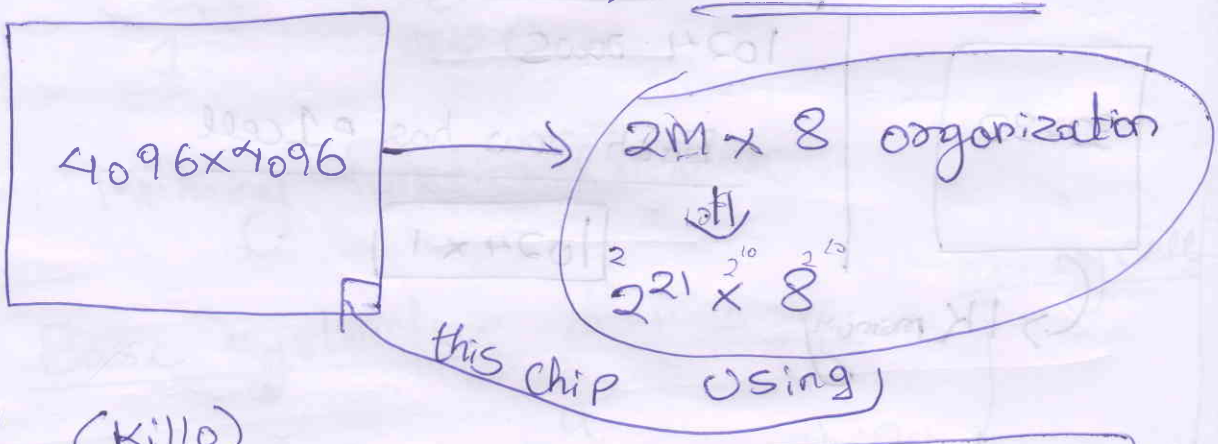


→ Row decoder

→ Group these 32-bits in 4 groups of 8 each then using 2:4 decoder choose any one of the group.

→ Column decoder

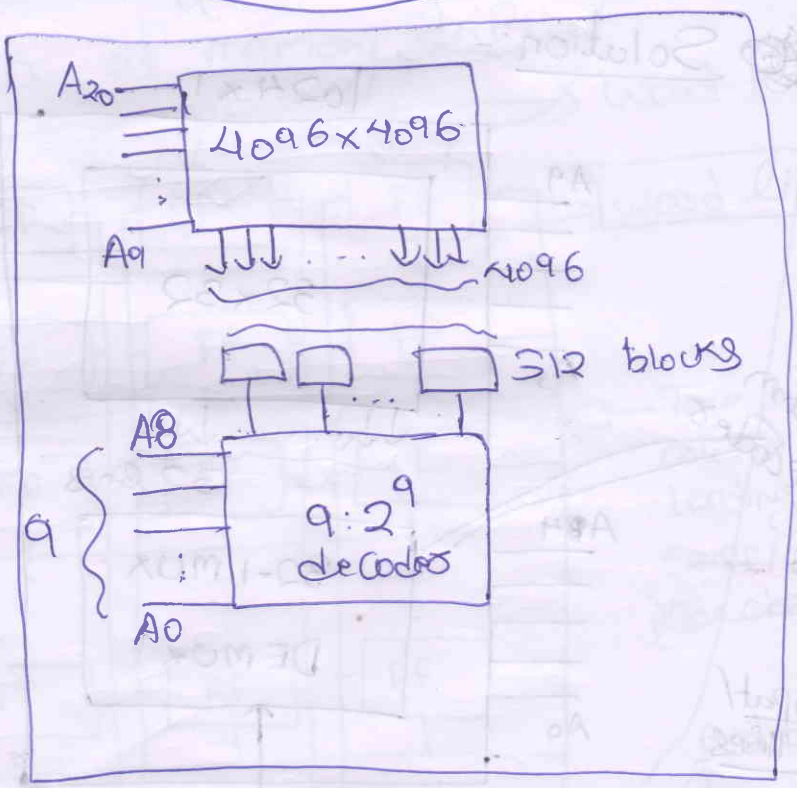
Q.)



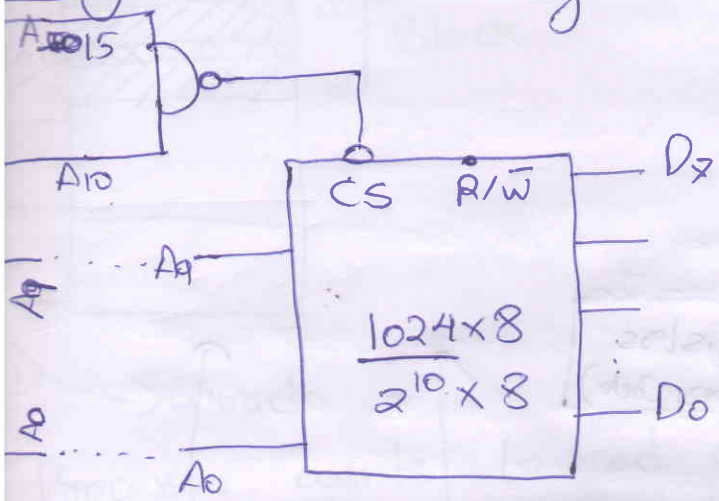
K → 2^{10} (Killo)

M → 2^{20} (Mega)

G → 2^{30} (Giga)



emory-interfacing (Not in Syllabus)



2^{10} 2^{12} ×

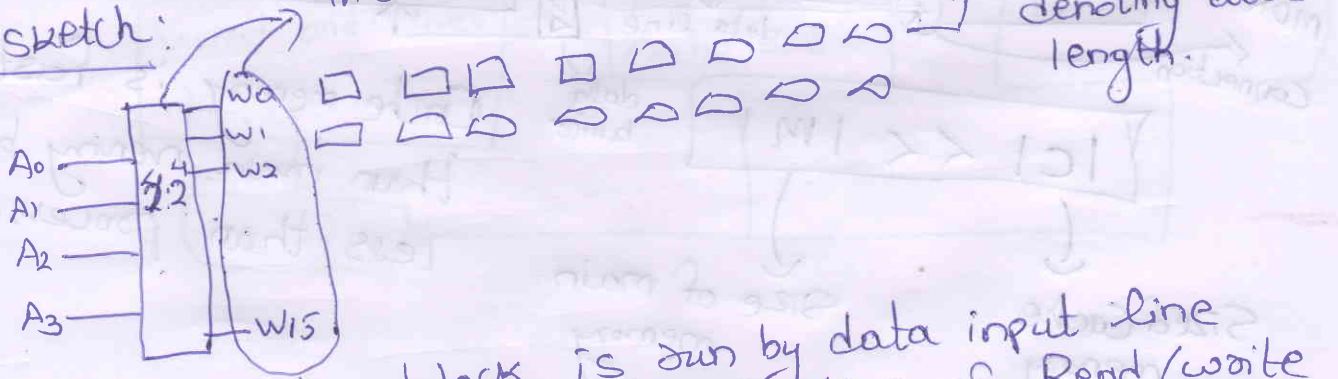
, these are 16 addressable lines, so maximum
e can connect 16 lines (i.e; 2^{16} memory locations)

In the above:- we need to connect 10 lines.
So the first ten lines from (A_0 to A_9) are directly
onnected with corresponding to address lines (A_0 to A_9)
The rest A_{10} to A_{15} are set to zero by connecting
all to a nand-gate with the chip select

(128 bits memory)

ote:- A 16×8 memory chip is meant by:-
16 words with each having word length
of 8.

ugh sketch:



The sense/write block is run by data input line and control lines which gives instruction of Read/write along with the word number. such that for each sense/write block that corresponding memory cell of that word will be chosen.