Roll No: Name:

Department of Computer Science & Engineering, NIT ROURKELA

Subject: Computer Architecture and organization (CS 2002) Class Test June, 2020

Answers must be to the point. Unnecessary long answers may attract **negative mark**.

Full Marks: 15 Time: 40min.

Answer all questions

1. A set-associative cache consists of 64 lines, or slots, divided into four-lines sets. Main memory contains 4K blocks of 128 words each. How do you divide the main memory address 0A831 in hexadecimal into tag, set and word. [3]

2. Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. Answer the following questions. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it? How many total bytes of memory can be stored in the cache?Identify the tag of the memory addres if you consider associative mapping. $[3+1+1]$

3. Write the sequence of control steps required for the single bus CPU organization taught in the class for the each of the following instructions.

   (a) ADDI $\#NUM, R_1$ (Immediate Mode)

   (b) ADD NUM, R_1 (Direct Mode), NUM is a memory location.

   (c) 2020 BR 2076 (Branch to memory location 2076)

   Assume that each instruction consists of two words. The first word specifies the operation and the addressing modes, and the second word contains the operands. $[2+2+3]$