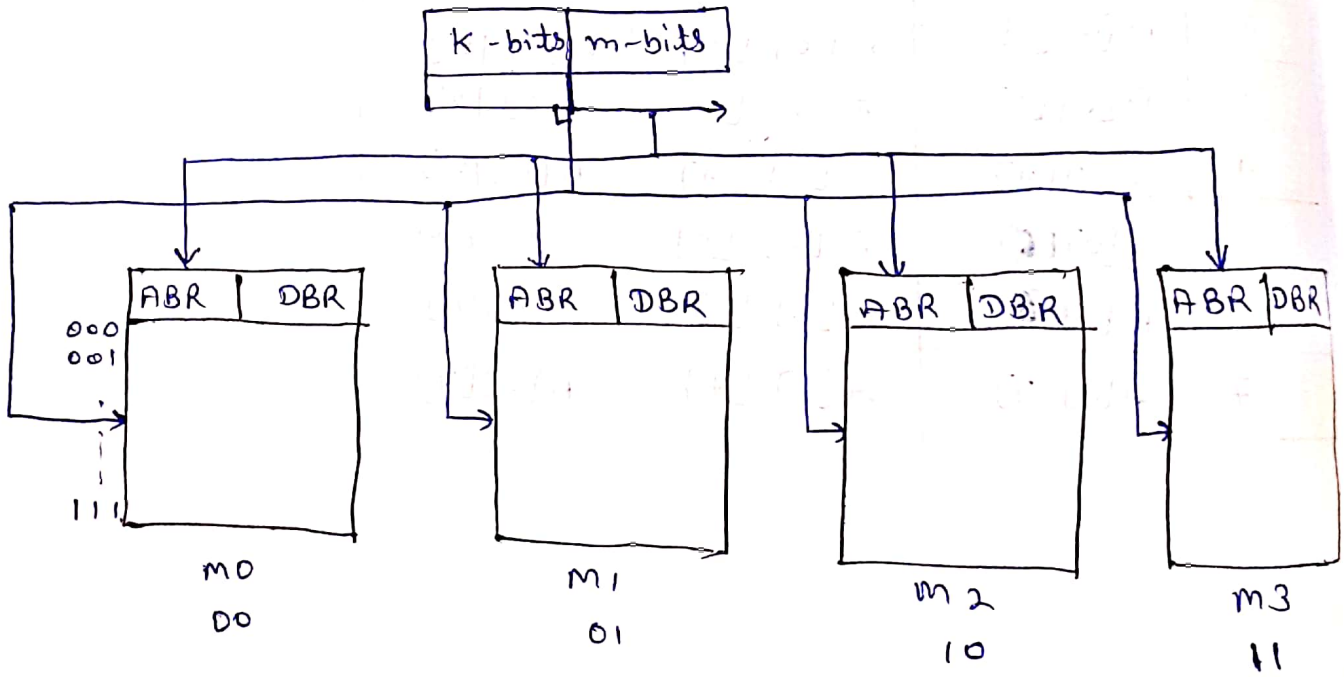
March 12, 2020

Memory Interleaving (Hamacher)

ABR : Address Buffer Register

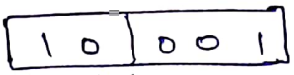
DBR : Data Buffer Register



* Each Module has 8 locations.

→ Total there are 4 Modules i.e., 32 locations.

→ If CPU generates 5 bit address (let's say), then,

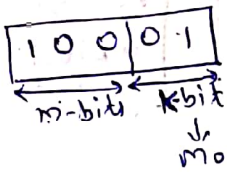


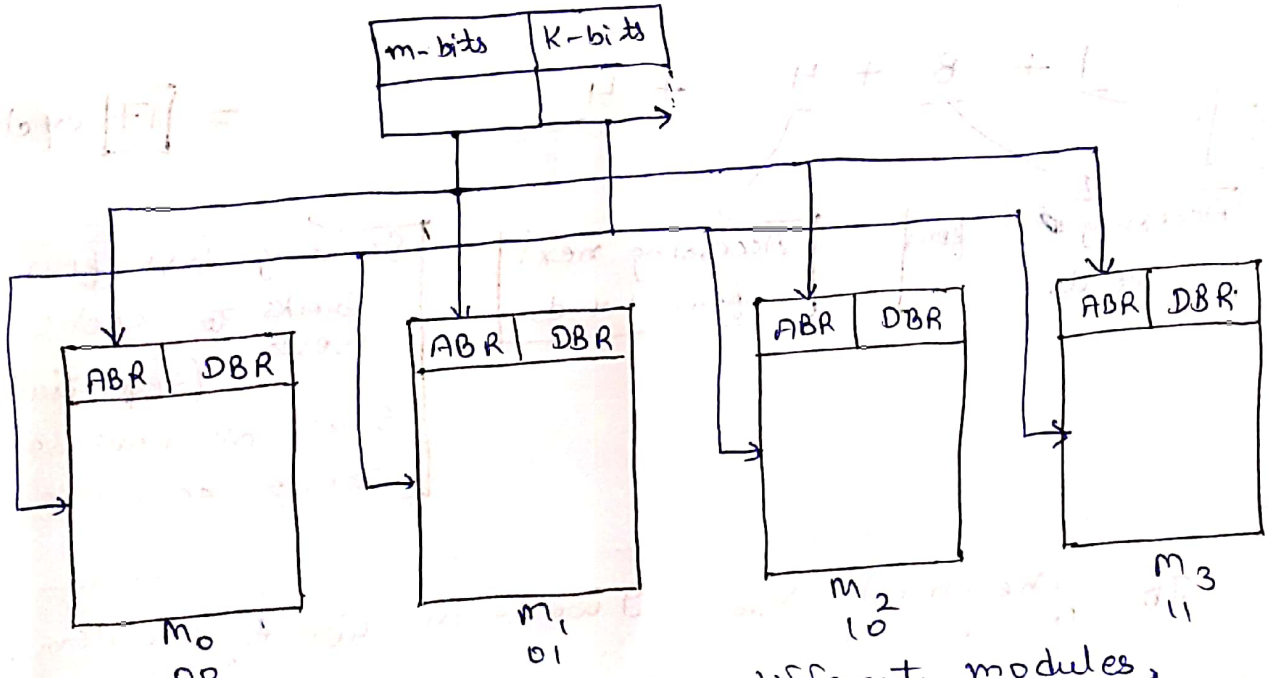
→ 5 bits

→ Consecutive words are in a module. So, We have to access words sequentially. That's why ~~we introduce~~ memory-interlacing has been introduced. In memory-interleaving, all modules work ~~independtly or~~ independently or in parallel.

In memory-interlacing, last two bits of address are used for identifying module.

Eg:-





* Now, Consecutive words are in different modules.

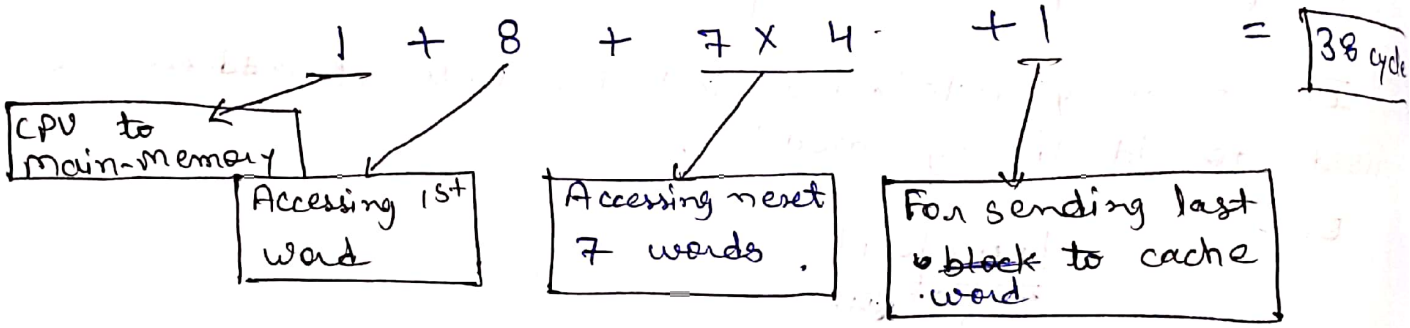
Eg:- Cache-block size = 8 words.

- One cycle is required to send main-memory address from CPU to main-memory.
- 8 clock-cycle for accessing 1st word in a module,
- 4 clock for accessing subsequent words from same module
- One clock cycle for sending one-word to cache,

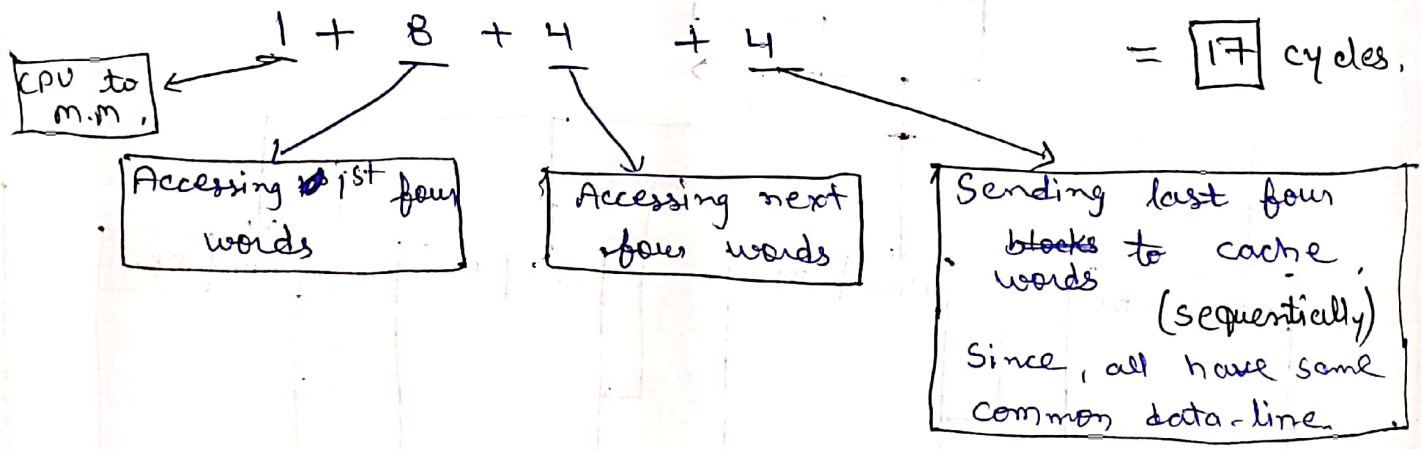
Find the time required to send a block to cache.

Solution:-

Without interleaving:-



In case of interleaving:-



Eg:- If cache-block size = 9 words in above problem.

4 4

⇒ 1 + 8 + 4 + 4 + 1 = 18

1

4 4 1

PBR DBR DBR