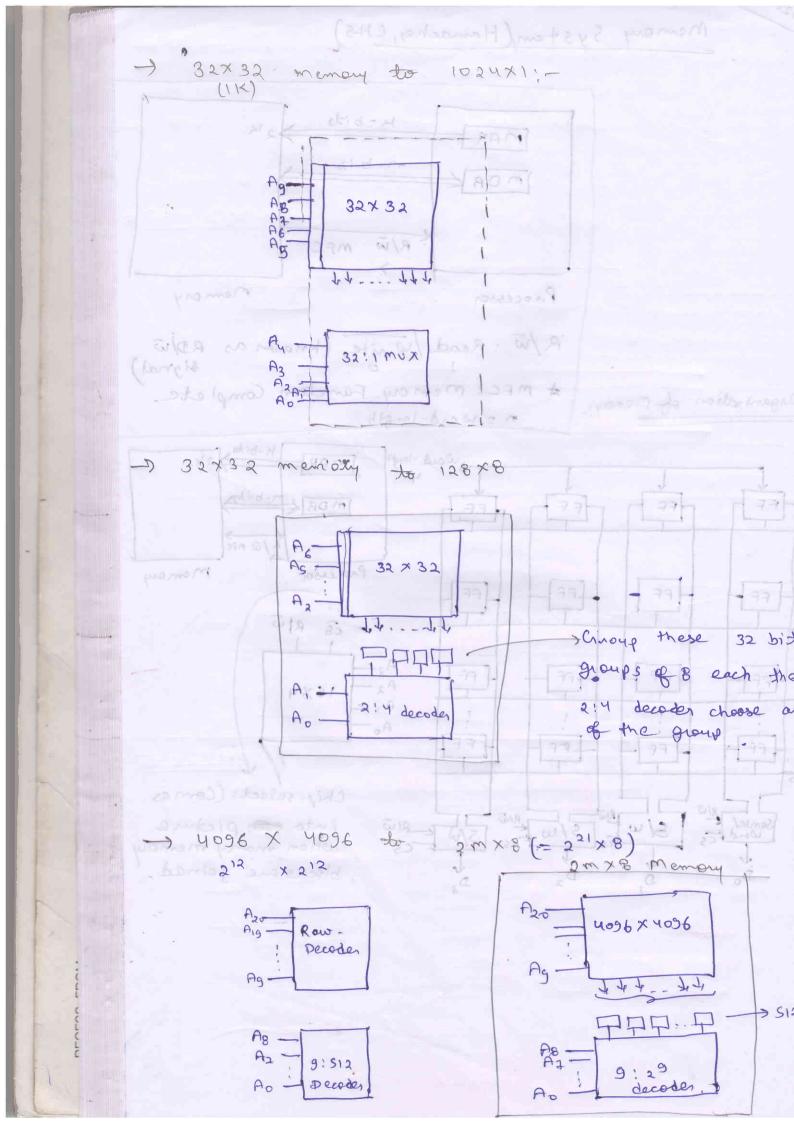
march 3, 2020 Memory System (Hamaches, CH-S) MAR Memory Processon R/w: Read / write. (known as RD/w \* MFC: Memory Function Complete. Internal Organization of memory: m = word-length MAR M DR Z FF RIW A3-Devide A 3 16×4 Chip-select: (Comes RIW Row Decoder into picture when many mema Do blocks are joined. JEOF R Jeon 135 039 B



( not in Syllabus now, It will be covered Memoy - Interforing: -A15 + 9 0 base of it mi croprocessor Ho And H 8085mP Dad May Asold Cs R/W Processon JENT TO PUBLISHEN nas 16 lines, 1024x8 Do Horago artic As there are 16 address lines, But, only 10 are to usable ber 1024x8 memory-drip. So, Rest are input into NAMI get & its output is connected to chip-select (CS). March 4th, 20 # Memory Hierarchy: gri mistro) > Registors (Primary Cache) MY M 10801 DELLIVERS RA van at brown Secondary Cache GOLD AA MORA (La Cache) Cost bit access speed Computer System main memory 5(3mg/ (RAM) Secondary overy phasilo 903 Memory. MISS 131 # memory Hierarchy & mapping (Hamacher 1 Stallings): types of theathers som be accept in loop, Address-bubber Address-line 10stog2 6 busy trans main Processor Control memory Control data line (C) < < (m) 3) size of << size of