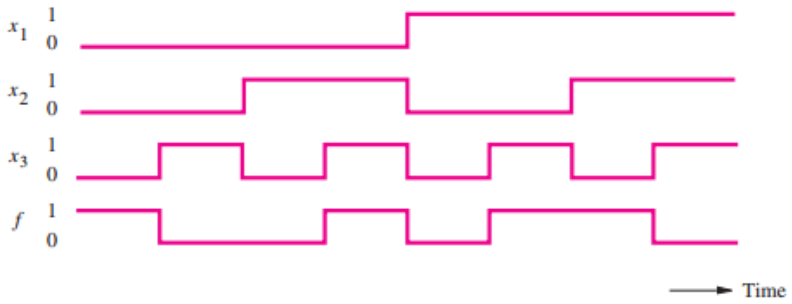
NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA
MID SEMESTER EXAMINATION, 2017-18
SESSION: 2017 – 2018 (Autumn)
B.Tech. 3rd Semester

Subject code: EC-202 **Subject Name: Digital Electronics** Dept. Code: **CS**
No. of pages: 2 Full Marks: 30 Duration: 2 ***Hours***

Figures at the right hand margin indicate marks.
All parts of a question should be answered at one place.

Answer all questions		
Q.No.	Particulars	Marks
1. a)	For the following timing diagram synthesize the function f in simplest SOP form. 	4+2
b)	Convert the following binary number 10101111 to decimal and octal.	
2. a)	Prove the validity of the logic equation $x_1'x_3' + x_2x_3 + x_1x_2' = x_1'x_2 + x_1x_3 + x_2'x_3'$	3+3
b)	Use algebraic manipulations to show that for three input variables x_1, $x_2$and x_3 $\sum m(1,2,3,4,6,7) = x_1 + x_2 + x_3$	
3. a)	Minimize the following Boolean function using K-map and implement the simplified function using basic digital logic gates. F(A, B, C, D)= ∑ m(0,2, 8, 9,10, 15) + D(1,3,6,7)	3+3
b)	A circuit that controls a given digital system has three inputs A, B and C. It has to recognize three different conditions: Condition X is true if C is true and either A is true or B is false Condition Y is true if A is true and either B or C is false Condition Z is true if B is true and either A is true or C is false The control circuit must produce an output of 1 at least two of the conditions X,Y and Z are true. Design the simplest circuit that can be used for this purpose	

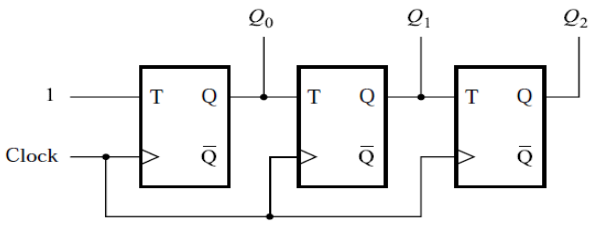
4.	a)	Minimize the four variable function $f(x_1, x_2, x_3, x_4) = \sum m(2,3,5,6,7,10,11,13,14)$ using prime implicants procedure.	3+3
	b)	Consider a minimum cost expression $f = x_1' x_2 x_3 + x_1 x_2' x_3 + x_1 x_2 x_4 + x_1' x_2' x_4$ Draw a gate level synthesized circuit for this function. Assume that all inputs are available in their true form. Use factoral decomposition to minimize the fan in of the gates. Synthesize the gate level minimized function. Also comment on the circuit performance trade off in this process.	
5.	a)	What are the different representations of negative numbers? Which one is most suitable for addition and subtraction in hardware?	3+3
	b)	Design a four bit 2's compliment adder / subtractor unit with clear indication of four bit inputs and other relevant control signals. Provide the gate level diagram for this circuit.	

NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA
END SEMESTER EXAMINATION, 2017
SESSION: 2017 – 2018 (Autumn)
B.Tech. 3rd Semester

Subject code: EC-202 **Subject Name: Digital Electronics** Dept. Code: **CS**
No. of pages: 2 Full Marks: 50 Duration: 3 ***Hours***

Figures at the right hand margin indicate marks.
All parts of a question MUST be answered at one place.

Answer **all** questions		
Q.No.	Particulars	Marks
1	Differentiate between PLA and PAL. Provide the generic gate level diagram for both logics.	5
2	Derive a CMOS complex gate for the minimized form of the logic function $f(A,B,C,D) = \sum m(0,1,2,4,6,8,10,12,14)$	5
3	a) Implement a three input XOR gate with 2:1 multiplexer(s).	3
	b) Design a BCD to seven segment code converter with its truth table and gate level circuit diagram.	2
4	a) Draw a gate level circuit diagram of a positive edge triggered D flip-flop	3
	b) With a clear timing diagram for a D flip-flop define and demonstrate the set up and hold times.	2
5	Design a 4-bit serial input and parallel output shift register with complete diagram.	5
6	a) What is the sequence that the following circuit counts in assuming the initial state to be 000.	3



	b) Design a two digit BCD counter using T flip flops depicting the function using suitable timing diagram.	2
7	Given a 100 MHz clock signal, derive a circuit using T flip flop(s) to generate 25 MHz clock signal. Draw the circuit and timing diagram.	5
8	Design a Mealy type FSM for sequence detection where the output becomes 1 for previous two values of input 00 or 11 and output to 0 for all other cases of inputs. Depict the sate assigned table using grey code and draw the complete digital circuit.	5
9	Design a modulo-8 counter using D flip flop in state machine approach.	5
10	Write a VHDL code for a 4:1 multiplexer using behavioural approach and dataflow approach.	5

NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA
MID SEMESTER EXAMINATION, 2015
SESSION: 2014 – 2015 (Spring)
B.Tech. 4th Semester

Subject code: EC-202 **Subject Name: Digital Electronics** Dept. Code: **EC & EI**
No. of pages: 1 Full Marks: 30 Duration: 2 ***Hours***

Figures at the right hand margin indicate marks.
All parts of a question should be answered at one place.

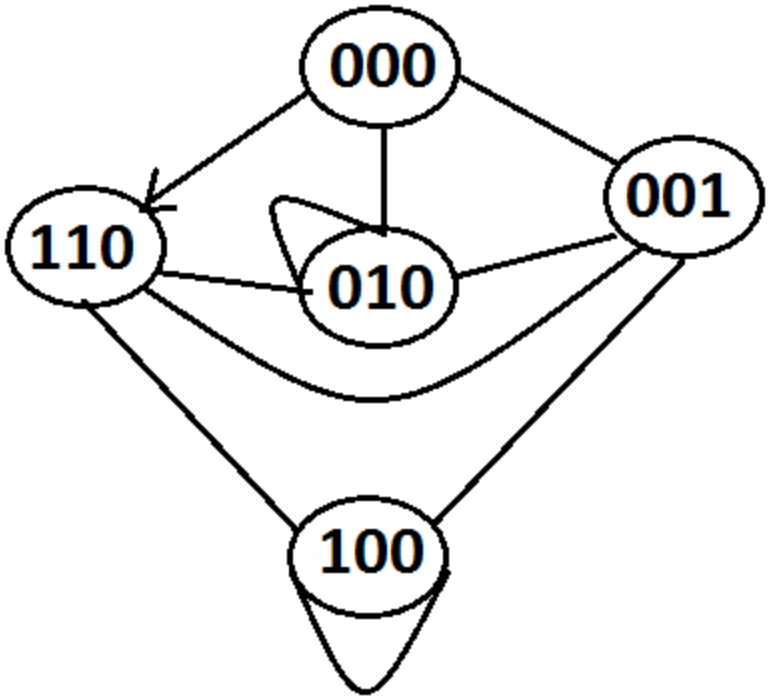
Answer all questions		
Q.No.	Particulars	Marks
1.	Using K-map, simplify the equation: $F(A, B, C, D) = \sum m(0, 2, 8, 9) + d(3, 7, 10, 11, 14, 15)$. Obtain the minimal SOP expression and implement it in NAND logic. In the equation 'm' stands for minterms and 'd' stands for don't care values.	6
2.	Reduce the following four-variable Boolean function using Quine-McCluskey method and implement the simplified function using basic gates only. $F(A, B, C, D) = \sum m(0, 1, 3, 4, 5, 7, 10, 13, 14, 15)$.	6
3.	i) Using the truth table implement a full subtractor using two 4:1 multiplexer.	3
	ii) Design a Binary to Gray code converter.	3
4.	Write down the algorithm of binary subtraction using 2's complement method of addition and design the corresponding circuit.	6
5.	i) Implement the following function using a 3-to- 8 decoder. $F(A, B, C) = \sum m(0, 1, 5, 6)$	3
	ii) Implement the following expression using a single 8:1 multiplexer $F(A, B, C. D) = \sum m(0, 1, 2, 5, 7, 8, 9, 14, 15)$.	3

NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA
END SEMESTER EXAMINATION, 2015
SESSION: 2014 – 2015 (Spring)
B.Tech. 4th Semester

Subject code: EC-202 **Subject Name: Digital Electronics** Dept. Code: **EC & EI**
No. of pages: 2 Full Marks: 50 Duration: 3 ***Hours***

Figures at the right hand margin indicate marks.
All parts of a question should be answered at one place.

Answer all questions		
Q.No.	Particulars	Marks
1.	Design a T flip-flop using SR flip-flop.	5
2.	Design one 3-bit Twisted Ring Counter. How many clock cycles this counter can counts? Explain with the timing diagrams.	5
3.	Design one Modulo-6 Asynchronous counter. Neatly draw the timing diagram and explain the operation of the counter.	5
4.	i) What are the major problems of an Asynchronous circuit?	1
	ii) What do you mean by critical races? Explain with an example.	2
	iii) How will you overcome static hazards? Explain with an example.	2
5.	Using the truth table of literals implement a full subtractor with the help of a suitable PLA.	4
6	What is lockout condition? Design a sequence generator to generate the sequence 0→3→5→4→6, using JK-FF and avoiding the lockout condition.	1 5
7	Design and implement a sequence detector to detect the sequence 1101011 using state diagram and SR-FF.	10

8	Implement the following state diagram using D-FF.  	10

NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA
END SEMESTER EXAMINATION, 2016
SESSION: 2015–2016 (Spring)
B.Tech. 4th Semester

Subject code: EC-202 **Subject Name: Digital Electronics** Dept. Code: **EC, EI & BM**
No. of pages: 1 Full Marks: 50 Duration: 3 ***Hours***

Figures at the right hand margin indicate marks.
All parts of a question should be answered at one place.

Answer all questions		
Q.No.	Particulars	Marks
1.	(a) What is the difference between Latch and Flip-Flop? (b) Write the difference between Mealy and Moore state machines. (c) Explain about "Lock-out" condition in Sequential circuits. (d) Design a T-FF using JK-FF. (e) Given a clock frequency of 200 MHz, how will you generate a signal of 50 MHz?	5x2
2.	(a) Write the excitation table for the JK-FF. (b) Design the state diagram of a sequence detector for "1011" sequence and implement the circuit by using JK-FF.	2 8
3.	Design a bidirectional synchronous shift register using D–FF.	5
4.	Design a modulo-7 counter using JK-FF.	5
5.	Design a 4-bit asynchronous up-counter and explain its operation using timing diagram.	5
6.	Design a JK-FF using D-FF.	5
7.	Design the basic building block of a 3×8 R/W Memory cell using decoder, combinational gates and D-FF and explain its operation.	5
8.	(a) Implement the following output function using a suitable PLA $F(A,B,C,D)=\sum m(3,7,8,9,11,15)$ (b) What do you mean by Static Hazard and how will you overcome it?	2 2+1

NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA
MID SEMESTER EXAMINATION, 2016
SESSION: 2015 – 2016 (Spring)
B.Tech. 4th Semester

Subject code: EC-202 **Subject Name: Digital Electronics** Dept. Code: **EC, EI & BM**
No. of pages: 1 Full Marks: 30 Duration: 2 ***Hours***

Figures at the right hand margin indicate marks.
All parts of a question should be answered at one place.

Answer all questions		
Q.No.	Particulars	Marks
1.	(a) Convert the binary number 1011.111 into octal number. (b) Convert the decimal number 73.625 into binary number. (c) Do the following addition. $(5)_8+(11)_{16}=(?)_3$	0.5 0.5 1
2.	Explain binary subtraction operation using 2's complement method (write for both positive and negative result).	3
3.	Using K-map simplify the following Boolean function. $F(A,B,C,D)=\sum m(0,2,8,9)+d(3,7,10,11,14,15)$ Obtain the minimal sum of product expression and implement it in NAND logic.	4
4.	Implement the following Boolean function using a 4×1 multiplexer. $F(a, b, c)=\sum(0,2,3,4,7)$	3
5.	Construct a 16×1 multiplexer with two 8×1 and one 2×1 multiplexers.	3
6.	Design a digital circuit for Excess-3 to BCD conversion.	4
7.	Simplify the following Boolean function using Quine-McKlusky method of gate minimization $F(A,B,C,D)=\sum(0,2,3,5,7,8,10,11,14,15)$.	4
8.	(a) Design a two input RTL NOR gate and explain current hogging problem of DCTL. (b) Design the following Boolean function using CMOS logic. F=A.(B+C)	1.5 1.5
9.	Explain the carry look ahead generator based addition of two binary numbers.	4

NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA
END SEMESTER EXAMINATION, 2015
SESSION: 2015 – 2016 (Autumn)
B.Tech. 3rd & 5th Semester

Subject code: EC-202 **Subject Name: Digital Electronics** Dept. Code: **CS & BM**
No. of pages: 2 Full Marks: 50 Duration: 3 ***Hours***

Figures at the right hand margin indicate marks.
All parts of a question should be answered at one place.

Answer **all** questions		
Q.No.	Particulars	Marks
1	Implement the look up table to realize $f = x_1x_2 + x_1'x_2'$ by using 2:1 multiplexer(s).	5
2	Realize $f = x_1 \oplus x_2 \oplus x_3$ using 2:1 multiplexer(s) and 4:1 multiplexer(s)	5
3	Implement the function $f(x_1, x_2, x_3) = \sum m(0,1,3,4,6,7)$ by using a 3:8 binary decoder and OR gate.	5
4	Draw a gate level circuit diagram of a clocked D-latch and its timing diagram. Differentiate between the latch and flip flop. Draw the timing diagram of a master slave D flip flop.	3 2
5	Design a 4-bit parallel input and serial output shift register. Comment on the input and output frequency of operation.	5
6	Design a mod (7) synchronous counter using T flip flops depicting the function using suitable timing diagram.	5

7	Given a 100 MHz clock signal, derive a circuit using D flip flops to generate 25 MHz clock signal. Draw the circuit and timing diagram.	5
8	What do you mean by finite state machine? Draw the general form of a sequential circuit. Differentiate between two types of FSMs.	5
9	Design a modulo-4 counter using JK flip flop in state machine approach.	5
10	Write a VHDL/ Verilog HDL code for a 4:1 multiplexer.	5

NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA
MID SEMESTER EXAMINATION, 2015
SESSION: 2015 – 2016 (Autumn)
B.Tech. 3rd & 5th Semester

Subject code: EC-202 **Subject Name: Digital Electronics** Dept. Code: **CS & BM**
No. of pages: 1 Full Marks: 30 Duration: 2 ***Hours***

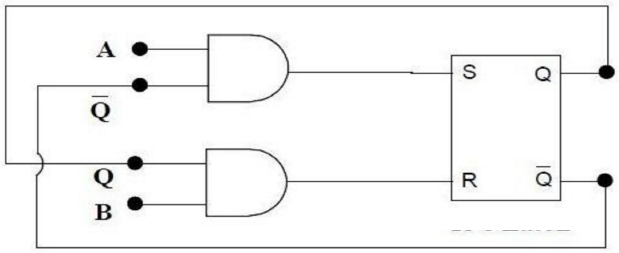
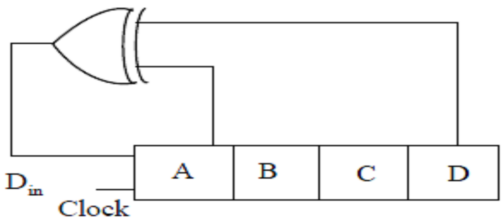
Figures at the right hand margin indicate marks.
All parts of a question should be answered at one place.

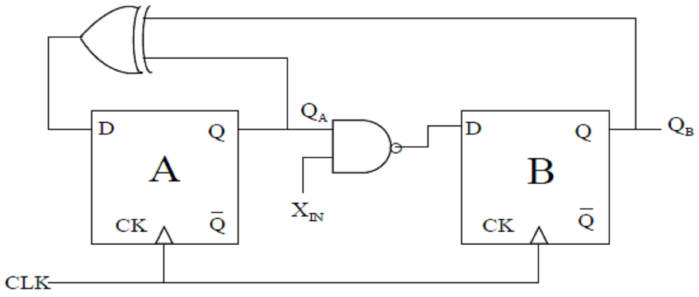
Answer all questions		
Q.No.	Particulars	Marks
1. a)	Perform the following operations involving 2's complement numbers and indicate whether arithmatic overflow occurs. i) 11011111+10111000 ii) 11010011-11101100	4+2
b)	Convert the following binary number 10101111 to decimal and octal.	
2. a)	Design the CMOS circuit to realize the function F=$\overline{A.B+C}$.	3+3
b)	What do you mean by fan-out? What is the approximate fan-out value of a TTL logic gate?	
3. a)	Prove the validity of the logic equation (A+B).(A'+B')=A'.B+A.B'	3+3
b)	Realize AB+C' using NOR gates only	
4. a)	Minimize the following Boolean function using K-map and implement the simplified function using basic digital logic gates. F(A, B, C, D)= ∑ m(0,2, 4, 6,7, 9) + D(10,11)	4+2
b)	Design the simplest circuit that has three inputs A, B, C, D which produces an output value of 1 whenever two or more of the input variables have the value 1 otherwise the output has to be 0.	
5.	Derive the truth table of a full subtractor. Design the circuit using required gates after optimization using K-map.	6

NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA
END SEMESTER EXAMINATION, 2016 – 2017 (Spring)
SEMESTER: 4th / B.TECH (EC/EI/BM)
Subject Name: Digital Electronics

Subject Code: EC202 **Dept. Code: EC**
No. of Pages: 2 **Full Marks: 50** **Duration: 3Hrs.**

All parts of a question should be answered at one place.

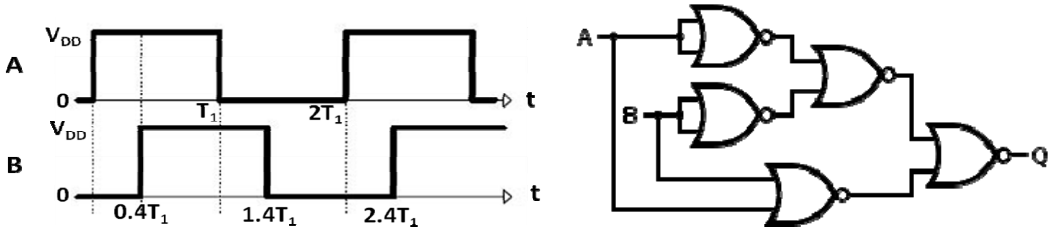
Q. No.		*Answer all the questions*	Marks
1.	(a)	Design a clock pulse transition detector circuit for edge triggering operation.	2
	(b)	Differentiate between latch and flip-flop.	2
	(c)	Show the state transition digram for SR flip-flop.	1
	(d)	Realize JK flip-flop using one T flip-flop and one 2:1 multiplexer.	3
	(e)	Draw the logic circuit diagram for Master slave JK flip-flop.	2
2.	(a)	Explain the Mealy machine using suitable block diagram.	2
	(b)	Consider the input-output relationships of a certain flip-flop XY as follows: for XY = 00, output toggles; for XY = 01, output resets; for XY = 10, output sets; for XY = 11, output remains unchanged. Design this XY flip-flop using JK flip-flop and necessary logic gates.	3
	(c)	If A = 1 and B = 0 in the following circuit, then determine the output Q of the NAND logic based SR flip-flop. 	2
	(d)	Design a MOD-9 ripple up counter. Draw the corresponding timing diagram also.	3
3.	(a)	Consider a 4-bit shift register circuit configured for right shift operation in the following figure. If the initial content of the register is ABCD = 1001, find out the content of the register after 3 clock pulses. 	2

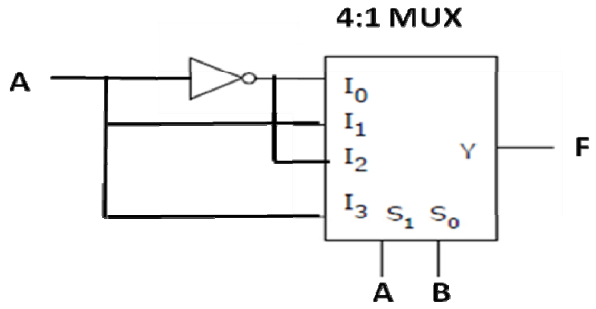
	(b)	**Design a sequential circuit which can act as either serial adder or subtractor (5-bit) depending on a control input. Draw a circuit for PISO shift register.**	**3**
	(c)	**Design a synchronous counter that generates the following sequence (ABC) as 000-010-101-110-000… Assume that the unused states always go to 000 on the next clock pulse. Use JK flipflop for the design.**	**3**
	(d)	**Determine the maximum clock frequency for reliable operation of a MOD-64 synchronous counter considering the propagation delay for each flip-flop and AND (2-input) gates as 40 ns and 15 ns respectively.**	**2**
4.	**(a)**	**If the initial states for two D flip-flops are Q_AQ_B = 00 in the circuit given below; determine the counter sequence obtained at Q_AQ_B as clock pulse continues. Assume X_{IN} = 0.** 	**3**
	(b)	**Design a 3-bit self correcting Johnson counter which is capable of shifting the data in left direction. Use D flipflop for the design.**	**3**
	(c)	**How many undesired states exist for a 5-bit Ring counter?**	**1**
	(d)	**Design a sequence generator circuit using one modulus counter and other necessary 4:1 MUX to generate the sequence 1011011.**	**2**
	(e)	**Which specific sequential circuit scheme can be used to convert a 40 kHz signal into 8 kHz signal?**	**1**
5.	**(a)**	**How many address lines are required for 64 KB memory with each address containing 1 byte data? Construct a 32 KB RAM using necessary 16 KB RAMs.**	**3**
	(b)	**Explain the read/write operation of MOS based dynamic RAM cell.**	**2**
	(c)	**Design a combinational circuit using Diode Matrix ROM which can take 2-bit number as input and produce the square of that input number as its output.**	**2.5**
	(d)	**Write a VHDL code to implement a full subtractor circuit.**	**2.5**

NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA
MID-SEMESTER EXAMINATION, 2016 – 2017 (Spring)
SEMESTER: 4th/ B.TECH (EC/EI/BM)
Subject Name: Digital Electronics

Subject Code: EC202 **Dept. Code: EC**
No. of Pages: 2 **Full Marks: 30** **Duration: 2Hrs.**

All parts of a question should be answered at one place.

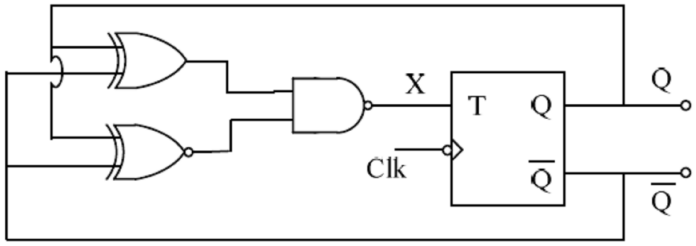
Q. No.		*Answer all the questions*	Marks
1.	(a)	Convert the hexadecimal number $(79)_H$ into octal and decimal number.	1
	(b)	Perform the following operation: $(32)_8 - (20)_4 = (?)_{10} = (?)_6$	1
	(c)	Differentiate between discrete signal and digital signal.	1
	(d)	Design the circuit for 2-bit Gray to Binary code converter.	1.5
	(e)	Using 2's complement of binary representation evaluate the following: $-(37)_{10} + (28)_{10}$	1.5
	(f)	Perform BCD addition for the following: $(637)_{10} + (363)_{10}$	1.5
	(g)	Using maximum four logic gates, design a three inputs (A, B, C) based combinational circuit which produces an output value of 1 whenever majority number of input variables have the value 0 otherwise the output is 0.	2.5
2.	(a)	If $AB + \overline{A}\,\overline{B} = C$, show that $BC + \overline{B}\,\overline{C} = A$ using Boolean laws.	1.5
	(b)	Determine the minimum Sum of Product (SOP) expression for the following function using K-Map and realize the minimized expression with the help of only NAND gates. $$f(A,B,C,D) = \prod^{M}(3,4,5,6,11,14) + \prod^{d}(1,8,13,15)$$	3
	(c)	Determine the output waveform of the following logic circuit for the given input waveform of A and B as shown below. Also calculate the duty cycle of output. 	2.5
	(d)	Represent a 3-input RTL based NOR gate. What is the approximate fan-out value for a CMOS logic gate?	2
	(e)	Write the truth table for 4-input Priority Encoder.	1

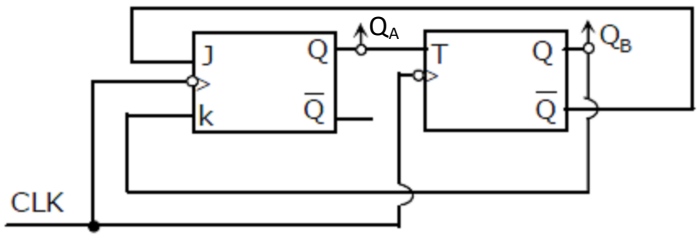
3.	(a)	**Realize a 3-input X-OR gate logic using one 4:1 Multiplexer (MUX).**	**2**
	(b)	**Design a 8:1 Multiplexer using only 2:1 Multiplexers.**	**2**
	(c)	**Implement a single bit magnitude comparator using two 1:2 decoders and two logic gates.**	**2.5**
	(d)	**Determine the logic gate operation which is implemented by the following circuit.**  	**1.5**
	(e)	**Design a CMOS circuit to realize the following function** $Y = A + B\overline{C}D$	**2**

NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA
END SEMESTER EXAMINATION, 2016 – 2017 (Autumn)
SEMESTER: 3rd/ B.TECH (CS)
Subject Name: Digital Electronics

Subject Code: EC202 **Dept. Code: EC**
No. of Pages: 2 **Full Marks: 50** **Duration: 3Hrs.**

All parts of a question should be answered at one place.

Q. No.	*Answer all the questions*	Marks
1. (a)	Design a combinational circuit for one bit magnitude comparator.	2
(b)	Draw the logic circuit diagram for JK flip-flop. Show its state transition diagram also.	3
(c)	Write the excitation table for SR flip-flop.	1
(d)	Realize JK flip-flop using one D flip-flop, one 2:1 MUX and one basic logic gate.	3
(e)	Differentiate between Mealy and Moore type of Finite state machine.	1
2. (a)	Explain the operation of Master slave JK flip-flop using its logic circuit diagram.	2
(b)	How can you design a clock pulse transition detector circuit for edge triggering operation?	1
(c)	The clock frequency applied to the digital circuit shown in the figure below is 10 kHz. If the initial state of the output of the flip-flop is 0, then determine the frequency of the output waveform Q. 	2
(d)	Design a MOD-6 ripple up counter. Draw the corresponding timing diagram also.	3
(e)	Determine the maximum clock frequency for reliable operation of a MOD-32 asynchronous counter with each flip-flop having a propagation delay of 25 ns.	2

3.	(a)	**Design a MOD-4 Gray code synchronous counter.**	**2.5**
	(b)	**Design a synchronous counter that has the following sequence: 000-010-101-110-000… Assume that the unused states always go to 000 on the next clock pulse.**	**3.5**
	(c)	**Draw the logic circuit for bidirectional shift register.**	**2**
	(d)	**Consider the initial content of a 4-bit register is 1011. The register is shifted 5 times to the right with a serial input sequence 11011. Write down the content of the register after each shift.**	**2**
4.	(a)	**Design a 3-bit self correcting Ring counter which is capable of rotating 1 in left direction.**	**3**
	(b)	**Design a 3-bit self correcting Johnson counter. How many undesired states exist for a 4-bit Johnson counter?**	**4**
	(c)	**Design a sequence generator using only one modulus counter and other necessary 4:1 MUX to generate the sequence 110101.**	**2**
	(d)	**Which specific sequential circuit scheme can you use to convert a 50 kHz signal into 5 kHz signal?**	**1**
5.	(a)	**If the state Q_A Q_B of the counter (shown in the following figure) at the clock time t_n is '10', then determine the state Q_A Q_B of the counter at $t_n + 3$.** 	**2**
	(b)	**How many address lines are required for 32 KB memory with each address containing 1 byte word? Write the corresponding ranges of addresses in Hexadecimal starting from $(0000)_H$. Construct a 16 KB RAM using necessary 8 KB RAMs.**	**4**
	(c)	**Explain the read/write operation of static RAM cell based on CMOS circuit.**	**2**
	(d)	**Implement a 3-bit binary to gray code converter using Diode Matrix ROM.**	**2**

NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA

MID-SEMESTER EXAMINATION, 2016 – 2017 (Autumn)

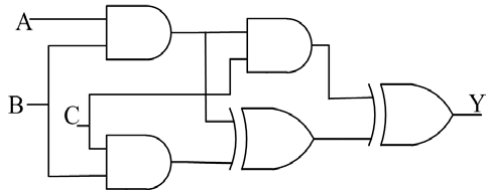
SEMESTER: 3rd/ B.TECH (CS)

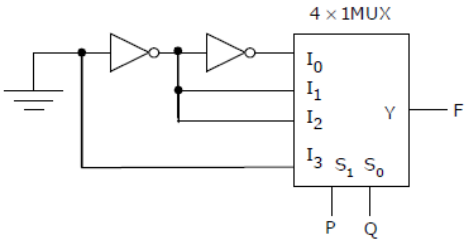
Subject Name: Digital Electronics

Subject Code: EC202 **Dept. Code: EC**

No. of Pages: 2 **Full Marks: 30** **Duration: 2Hrs.**

All parts of a question should be answered at one place.

Q. No.		*Answer all the questions*	Marks
1.	(a)	**Convert the binary number 11110.11 into decimal and hexadecimal number.**	1
	(b)	**Evaluate the following: $(16)_8+(24)_{16} = (?)_{10} = (?)_5$**	1
	(c)	**Convert the gray code into binary equivalent: 101100101**	1
	(d)	**Write two major advantages of digital signal over analog signal?**	1
	(e)	**Perform the subtraction using 2's complement of binary representation for the following: $(63)_{10} - (29)_{10}$**	2
	(f)	**Perform BCD addition for the following: $(546)_{10} + (354)_{10}$**	1.5
	(g)	**Design the simplest combinational circuit that has three inputs A, B, C and it produces an output value of 1 whenever odd number of input variables have the value 1 otherwise the output is 0.**	2.5
2.	(a)	**Prove the following DeMorgan's theorem: $\overline{A+B}=\overline{A}.\overline{B}$ only using Boolean laws.**	2
	(b)	**Obtain the minimum Sum of Product (SOP) expression for the following function using K-Map and realize the minimized expression using only NAND gates.** $f=\sum_m(2,3,4,5,6,8,10)+\sum_d(11,12,13,14,15)$	4
	(c)	**What is the output of the following logic circuit among the given options?**  **Options: (a) A+B+C; (b) A(B+C); (c) B(C+A); (d) C(A+B)**	2
	(d)	**What is meant by fan-out of logic gate? What is the approximate fan-out value for a TTL logic gate ?**	2

3.	**(a)**	**Implement a full adder logic using two 4:1 Multiplexers.**	**3**
	(b)	**Realize a full subtractor logic operation using two 2:4 decoders and other necessary logic gates.**	**2.5**
	(c)	**The logic function implemented by the circuit below resembles to which logic gate operation?** 	**2**
	(d)	**Design a CMOS circuit to realize the following function** $\overline{A.B+C.D}$	**2.5**

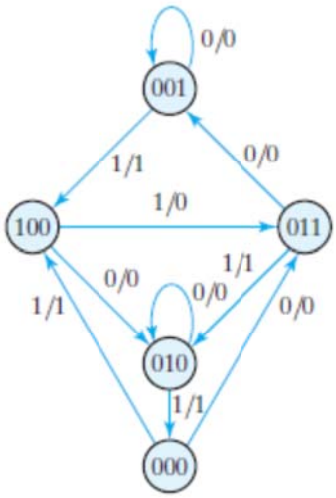
NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA
END - TERM EXAMINATION, 2018
SESSION: 2017 – 2018 (Spring)
B.Tech. 4th Semester (EC, EI, BM, BT)

Subject code: EC202 Subject Name: Digital Electronics Dept. Code: **EC**
No. of pages: 3 Full Marks: 50 Duration: **3 *Hours***

Figures at the right hand margin indicate marks.
All parts of a question should be answered at one place.

Q.No.	Question	Marks
1	The message 1001001011100111101100011011 has been coded in the Hamming code of Table shown below and transmitted through a noisy channel. Decode the message assuming that at most a single error has occurred in each code word.	5
2	Assume that the exclusive-OR gate has a propagation delay of 15 ns and that the AND or OR gates have a propagation delay of 3 ns. What is the total propagation delay time in the four-bit adder.	3
3	Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to- 4-line decoder. Use block diagrams for the components.	3
4	Implement the Boolean function f (A,B, C, D) = $\sum(0, 2, 5, 8, 10)$. with a multiplexer	4

	Digit position and symbol						
Decimal digit	1 p_1	2 p_2	3 m_1	4 p_3	5 m_2	6 m_3	7 m_4
0	0	0	0	0	0	0	0
1	1	1	0	1	0	0	1
2	0	1	0	1	0	1	0
3	1	0	0	0	0	1	1
4	1	0	0	1	1	0	0
5	0	1	0	0	1	0	1
6	1	1	0	0	1	1	0
7	0	0	0	1	1	1	1
8	1	1	1	0	0	0	0
9	0	0	1	1	0	0	1

5.	Using *JK* flip-flops, (a) Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6. (b) Draw the logic diagram of the counter.	8
6.	The contents of a four-bit register is initially 0110. The register is shifted six times to the right with the serial input being 1011100. What is the content of the register after each shift?	3
7.	Design a 4-bit ripple down counter using T-flip flops. How is Johnson counter different than other binary counters?	6
8.	A sequential circuit has three flip-flops *A, B, C* ; one input *x_in* ; and one output *y_out.* The state diagram is shown below . The circuit is to be designed by treating the unused states as don't-care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states using D flip flops.  	6
9.	Draw the state diagram of JK-Flip flop showing clearly the internal states as well as the transitions which take place.	2

10	Design two serial adder circuits, one of type Moore and another of type Mealey. Compare and contrast them and comment which type is useful and for what application. OR For the state table shown below (a) Draw the corresponding state diagram. (b) Tabulate the reduced state table. (c) Draw the state diagram corresponding to the reduced state table.	6

	Next State		Output	
Present State	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

11.	Define the following terms i) Fan-out ii) Propagation delay iii) TTL iv) EPROM	4

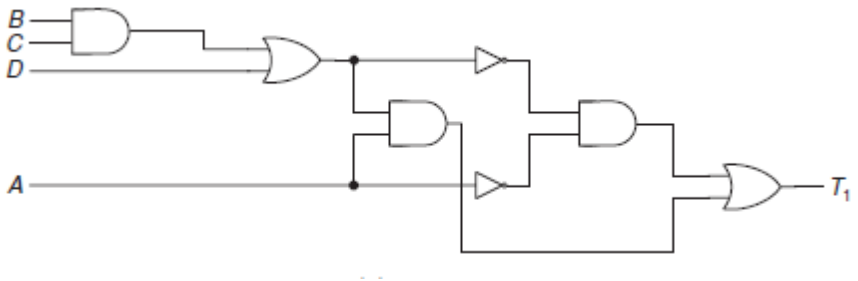
NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA
MID - TERM EXAMINATION, 2018
SESSION: 2017 – 2018 (Spring)
B.Tech. 4th Semester (EC, EI, BM, BT)

Subject code: EC202 Subject Name: Digital Electronics Dept. Code: **EC**
No. of pages: 3 Full Marks: 30 Duration: **2 *Hours***

Figures at the right hand margin indicate marks.
All parts of a question should be answered at one place.

Q.No.	Question	Marks
1	Utilizing Karnaugh map, minimize the function i. f (A,B, C, D, E) = ∑(1, 2, 6, 7, 9, 13, 14, 15, 17, 22, 23, 25, 29, 30, 31). ii. f (A,B, C, D, E) = ∑(0, 1, 4, 8, 12, 13, 15, 16, 17, 23, 29, 31).	6
2	Utilizing Quine–McCluskey Tabular method, minimize the function f (A,B, C, D, E) = ∑(1, 5, 6 , 7 , 9, 13, 14, 15, 17, 18, 19, 21, 22, 23, 25, 29, 30)	10
3	Utilizing the below four expressions design the circuit with 3 half adders D= A⊕ B ⊕ C E= A' B C + A B' C F= A B C'+ (A' + B') C G= A B C	5
4.	Design a two-level code converter from the *Ringtail code* shown in Table below to BCD code.	6

Decimal	Ringtail				
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	1
3	0	0	1	1	1
4	0	1	1	1	1
5	1	1	1	1	1
6	1	1	1	1	0
7	1	1	1	0	0
8	1	1	0	0	0
9	1	0	0	0	0

5.	Express T_1 as functions of A, B, C, and D.  	3
	OR	
5.	Explain the concept of LookAhead Carry with respect to Full Adder.	