Design of Low Power, High Gain PLL using CS-VCO on 180nm Technology

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***Abstract*—This project focuses on the design and optimization of a low-power, high-performance Phase Locked Loop (PLL) circuit, building upon principles outlined in the referenced research paper. The foundational PLL architecture utilizes a dead zone-free Phase Frequency Detector (PFD), charge pump, first-order low pass filter, and a current-starved voltage-controlled oscillator (CS-VCO). While the original work showcased significant advantages in terms of tuning range, VCO gain, and minimized dead zone, our implementation achieves further enhancements in power efficiency and jitter stabilization.**
Through critical design improvements, our proposed PLL significantly reduces the overall power dissipation to 1.4 µW, a notable advancement over the base design, and limits the maximum jitter to 9 ps under standard operating conditions.All simulation and validation procedures were conducted using the latest CADENCE UMC 180nm process technology files.

I. Introduction

Phase Locked Loop (PLL) is a class of circuit, used primarily in communication systems. It is suitable for a wide variety of applications, such as AM radio receivers, frequency demodulators, multipliers, dividers, and frequency synthesizers.Now, the whole PLL circuit can be integrated as part of a larger circuit on a single chip. The design and development of low power and high gain PLL has been a challenge for researchers in recent years.

Basically PLL.constitutes of PFD (Phase Frequency Detector), Charge pump, Loop filter, and VCO (Voltage Control Oscillator); these three are the basic building blocks of the PLL. Phase Frequency Detector (PFD) which generates a pulse output that is proportional to the phase difference between the inputs is one of the important components of a PLL. Output of the PFD is given to a charge pump and Low Pass Filter circuit which regulates the control voltage to be applied to the Voltage Controlled Oscillator (VCO) of the PLL and VCO increases or decreases output frequency according to the control voltage produced by the charge pump.

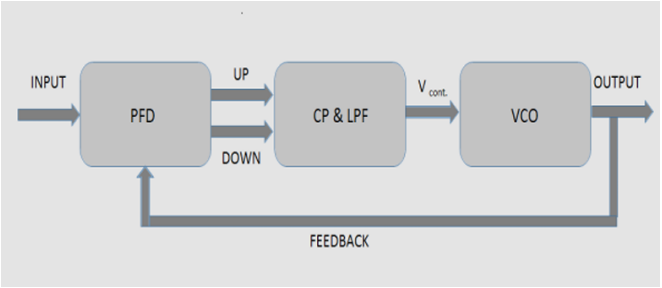

Fig. 1. Basic Building Block of PLL

II. Proposed PLL Circuit Description

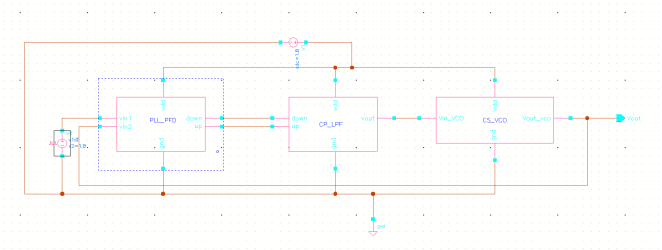

Fig. 2. Proposed PLL Testbench

A. PFD (Phase Frequency Detector)

The Phase Frequency Detector (PFD) compares the phase of the input (reference) signal with the output signal from the VCO, generating phase error signals known as UP and DOWN. An UP signal is triggered when the reference signal is ahead of the VCO output, whereas a HIGH DOWN signal indicates the VCO output leads the reference. As shown in Fig.3, the designed PFD utilizes four inverters, two pass transistors, two NMOS and two PMOS devices. Notably, the absence of a reset circuit ensures the PFD remains dead zone free, allowing it to reliably produce accurate output for any phase difference between the reference and VCO signals.

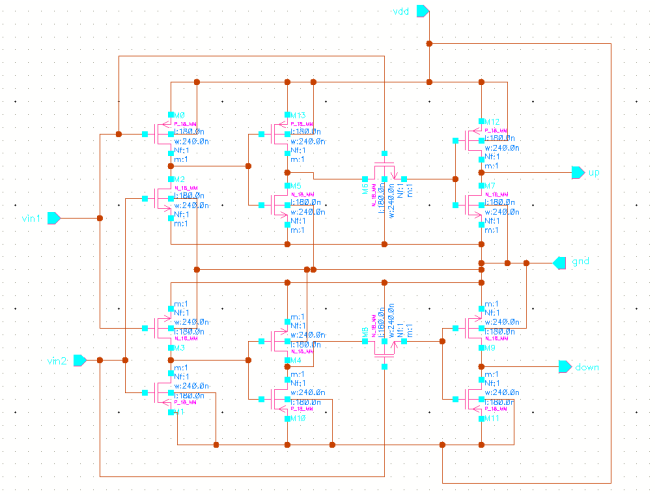

Fig. 3. Phase Frequency Detector Circuit

B. CP and LPF (Charge Pump and Loop Filter)

The charge pump (CP) serves to transform the digital signals output by the PFD into a current, facilitating the creation of a stable and adjustable control signal for the oscillator's frequency. The CP deposits its charge into the loop filter's capacitor. In the proposed design, the low pass filter (LPF) plays a dual role: it filters high-frequency noise from the PFD and stores the charge supplied by the CP, thereby supplying an analog voltage to the CS-VCO. Fig.4 presents the schematics for both the charge pump and the low pass filter, which are driven by the UP and DOWN signals produced by the PFD. When the UP signal is HIGH, transistor MN1 activates, charging the LPF's capacitor; conversely, a HIGH DOWN signal turns on MN2, causing the capacitor to discharge. As determined by the PFD's output, the charge pump may increase, decrease, or maintain the control voltage, ensuring proper oscillator tuning.

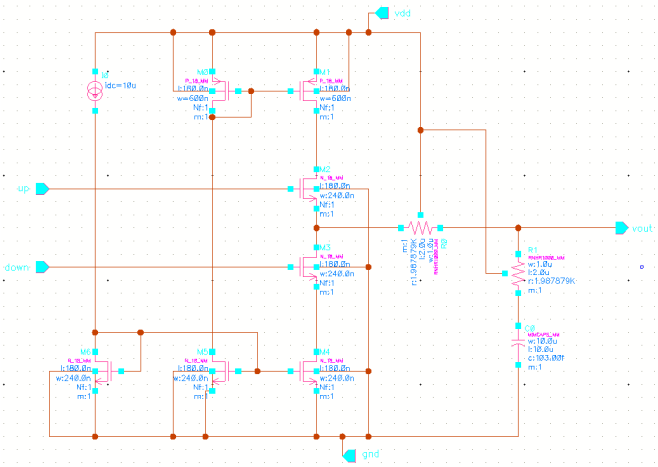

Fig. 4. CP & LPF Circuit

C. CS (Current Starved) - Voltage Controlled Oscillator

The Voltage Controlled Oscillator (VCO) is central to PLL operation, as it modulates the output frequency based on the applied control voltage. Fig.5 illustrates the schematic for the proposed current-starved VCO (CS-VCO). In this design, transistors MP2 and MN2 act as current limiters for the inverter pair (MP7 and MN7). The CS-VCO consists of five such inverters, each with current limiting transistors, connected in sequence for a five-stage configuration. The VCO produces sinusoidal oscillations, and the final inverter (MP12 and MN12) serves to convert the sinusoidal waveform into a square wave, enabling compatibility with digital circuit requirements.

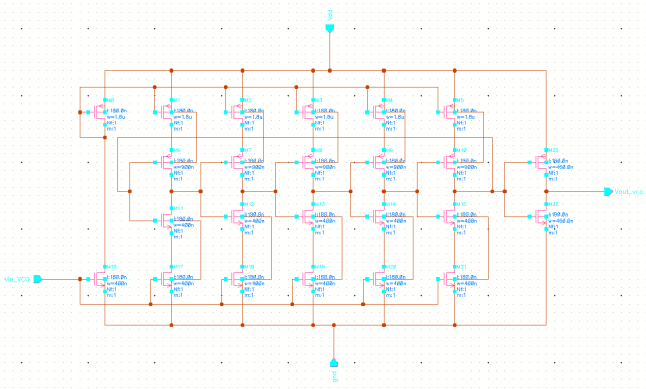

Fig. 5. CS-VCO Circuit

III. ANALYSIS OF PLL IN LOCKED STATE

Fig.6 shows the linear model of proposed PLL. In which G1(s) is the transfer function of PFD, CP and LPF, and G2(S) is the transfer function of VCO.

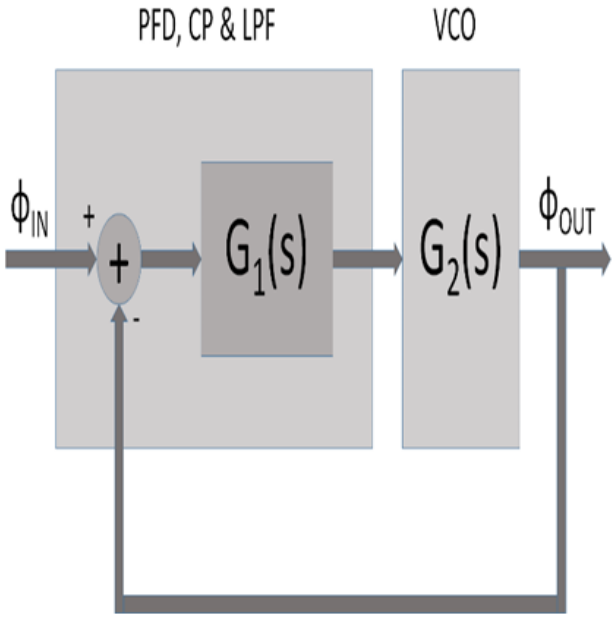

Fig. 6. Linear Model of PLL

$$H(s)_{\text{open}} = \frac{I_{cp}}{2\pi}\left[R_1 + \frac{1}{C_0 s}\right] \cdot \frac{I_{vco}}{s} \tag{1}$$

Closed loop T.F. of this PLL is -

$$H(s)_{\text{close}} = \frac{\varphi_{\text{out}}}{\varphi_{\text{in}}}(s) = \frac{H(s)_{\text{open}}}{1 - H(s)_{\text{open}}} \tag{2}$$

$$\frac{\varphi_{out}(s)}{\varphi_{in}(s)} = \frac{\frac{I_{cp}K_{vco}}{2\pi C_0}(R_1 C_0 s + 1)}{s^2 + \frac{I_{cp}}{2\pi}K_{vco}R_1 s + \frac{I_{cp}}{2\pi C_0}K_{vco}} \tag{3}$$

Since phase and frequency are related by a linear operator, eq. (3) also applies to input and output variations of frequency -

$$\frac{\omega_{out}(s)}{\omega_{in}(s)} = \frac{\frac{I_{cp}K_{vco}}{2\pi C_0}(R_1 C_0 s + 1)}{s^2 + \frac{I_{cp}}{2\pi}K_{vco}R_1 s + \frac{I_{cp}}{2\pi C_0}K_{vco}} \tag{4}$$

According to eq. (3) and eq. (4) -

When φ_{in}/ω_{in} changes very slowly, i.e. ($s \rightarrow 0$), then $H(s)_{close}$ will be one and $\varphi_{out}/\omega_{out}$ change according to φ_{in}/ω_{in}, means PLL in locked state.

When φ_{in}/ω_{in} changes abruptly, but after enough time to settle the system, i.e. ($s \rightarrow 0$), then $H(s)_{close}$ will be one and φ_{out} tracks the φ_{in}, means PLL in locked state.

IV. SIMULATION RESULTS

A. Transient Response of PFD

When the phase of the Vin1 signal advances ahead of Vin2, the UP signal switches HIGH; conversely, if Vin2 leads Vin1 in phase, the DOWN signal becomes HIGH.

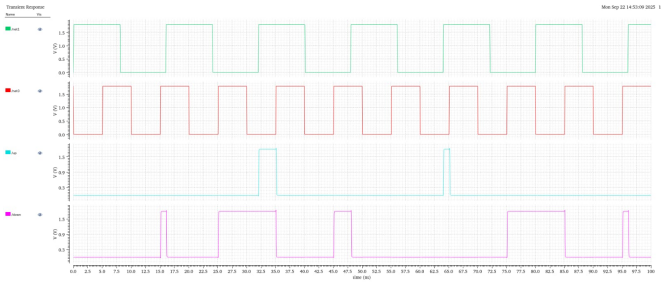

Fig. 7. Transient Response of PFD

B. Transient Response of CP AND LPF

A sequence of UP and DOWN signals from the PFD is applied to the charge pump, which in turn alters the current supplied to the loop filter's capacitor. The resulting control voltage across the LPF capacitor is monitored; when UP signals dominate, the voltage rises due to charging, and when DOWN signals prevail, the voltage falls as the capacitor discharges. The LPF effectively smooths these transitions, providing a stable analog control voltage for the next stage in the PLL.

Fig. 8. Transient Response of CP AND LPF

C. Transient Response of CS-VCO

A ramp signal (0.0 V-1.8 V) is connected to the VCO input as control voltage, and the corresponding oscillation frequency is observed at the VCO output terminal.

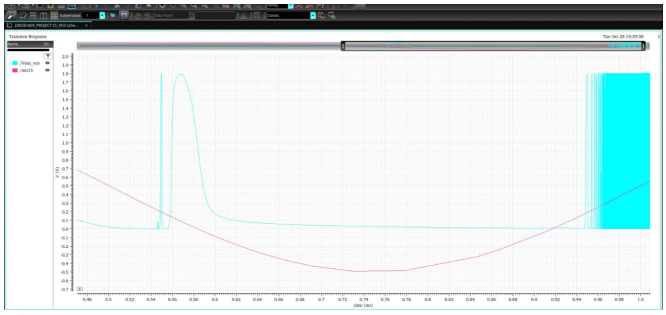

Fig. 9. Transient Response of CS-VCO

D. Transient Analysis of PLL

Fig.10 shows the transient response of PLL. A pulse signal of 1GHz frequency is connected to input reference terminal of the PLL and second input terminal of the PLL is connected with its output terminal, and results are observed as-

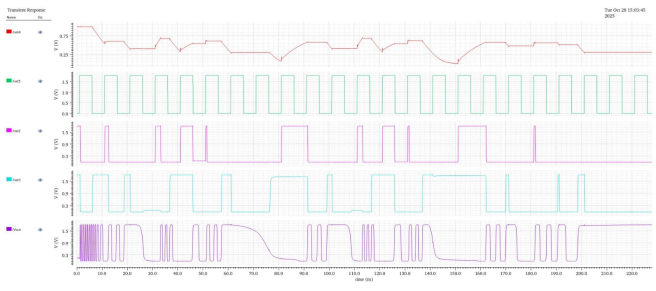

Fig. 10. Transient Analysis of PLL

E. Locking Plot of PLL

Fig.11 VCO output signal is shown in blue, reference signal in red, and control voltage in black. By overlapping them, it is clear that the VCO output is locked with the input reference and the control voltage is constant.

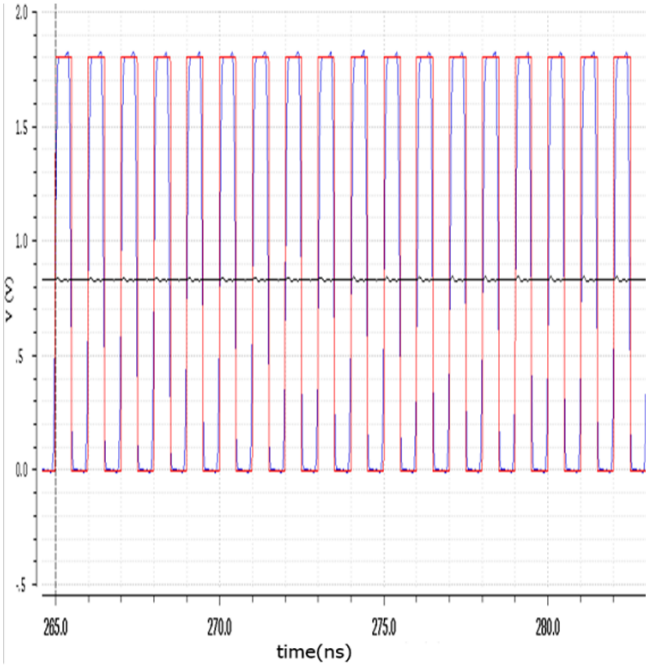

Fig. 11. Locking Plot of PLL

F. Power Dissipation of PLL

The fig.12 shows the total power dissipation by the PLL system:
The Total power dissipation is calculated as:
Pavg = Vdd * Iavg = Vdd * (794.9pA)
From the above simulation results, Pavg is 1.4nW.

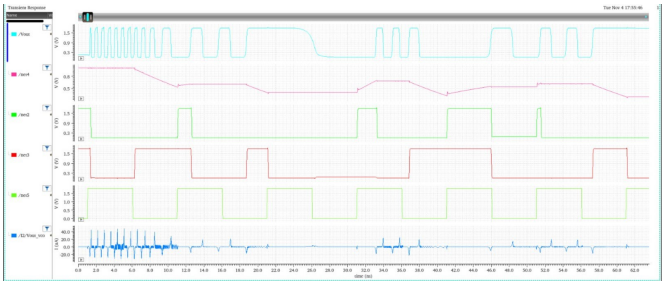

Fig. 12. Power Dissipation of PLL

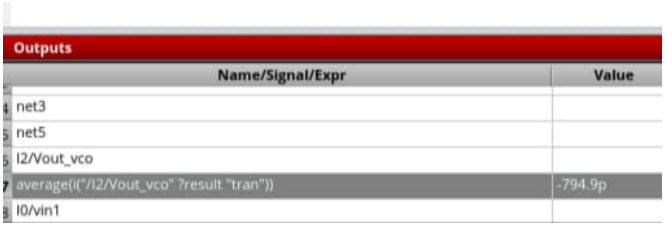

Fig. 13. Average power

CONCLUSION

In this work, we have detailed the design and simulation of a low-power, high-performance Phase Locked Loop (PLL) utilizing a dead zone-free PFD, efficient charge pump, and a current-starved VCO on 180nm CMOS technology. Through targeted architectural optimizations, our PLL achieves a power dissipation of just 1.4nW and a maximum jitter of 9ps, also high gain 2.21GHz/V and larger tuning range 167MHz – 1.711GHz is achieved in designed CS-VCO, marking significant advances in both energy efficiency and timing stability. Rigorous simulation and validation confirm the robustness of the proposed design, making it highly suitable for precision-driven, low-power applications in modern communication, sensor systems, and portable electronics. Future developments can focus on advanced jitter reduction strategies and further miniaturization to enhance applicability in next-generation devices.

NOVELTY

The key novelty in our low-power, high-gain PLL design lies in achieving *ultra-low-power* operation. By carefully reducing the bias current and optimizing the MOSFET W/L ratios, we were able to lower the power consumption from 277.2 uW to 1.4 nW. In addition, the overall system power and area were further minimized by reducing the number of stages in the common-source (CS) voltage-controlled oscillator from five stages to three. This modification resulted in a slight change in the maximum pull-in time, increasing from 265 ns to 280 ns, which remains acceptable

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