A Subthreshold Cross-Coupled Hybrid Charge Pump for 50-mV Cold-Start

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***Abstract*—In this project, we present a fully integrated switched-capacitor DC-DC converter based on the Dickson charge pump, designed to operate efficiently even when the input voltage is so low that the transistors work in the subthreshold region. To address the limitations faced by conventional charge pump designs in such low-voltage conditions, our architecture incorporates resistors in charge transfer switches. This modification helps to ensure reliable operation and improved performance in the subthreshold regime.**

Our implementation is based on 180nm CMOS technology. Despite the larger technology node, the proposed design is capable of boosting input voltages as low as 50 mV up to a maximum output of 270 mV. Compared to traditional dual-branch cross-coupled charge pumps, our solution significantly reduces the settling time - about 25 times - while maintaining a voltage conversion efficiency above 76%. This makes the design particularly suitable for powering up energy-harvesting systems, especially those driven by ultra-low input sources like thermoelectric generators.

***Index Terms*—Charge pump (CP), Dickson charge pump, energy harvesting, power management, switched-capacitor boost converter, thermoelectric generator.**

I. Introduction

Energy harvesting (EH) from ambient sources is becoming increasingly important for powering autonomous electronic systems such as wearable devices, implantable medical tools, and IoT sensor nodes. Among various sources, thermoelectric generators (TEGs) are particularly well-suited for applications like body-worn electronics, where other options (e.g. solar or vibrational energy) are less reliable because of environmental variability.

TEGs convert heat into electricity via the Seebeck effect, generating voltage from a temperature gradient between two conductors. However, due to the limited temperature differences in practical scenarios, such as the small gradient between human skin and ambient air, the resulting voltages are often very low (tens to hundreds of millivolts), making them inadequate for directly powering digital or analog circuits.

To overcome this, a Power Management Unit (PMU) is required to boost and regulate the TEG output. A critical component of this PMU is the cold-start circuit, which initiates system operation using ultra-low input voltages. Switched-capacitor (SC) DC-DC converters, also known as charge pumps (CPs), are preferred for such scenarios because of their fully integrable design and small footprint, even though they offer lower efficiency compared to switched-inductor converters.

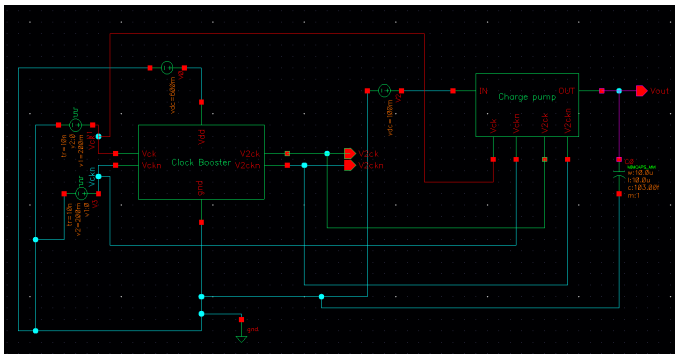

Fig. 1. Subthreshold charge pump topology based on Dickson architecture.

Recent research has focused on developing CPs that can self-start from input voltages below 100 mV. Techniques like boosted gate control signals and adaptive phase generation have been used to overcome transistor threshold limitations and improve startup performance.

In this work, we propose a novel charge pump architecture tailored for TEG-based energy harvesting systems. Designed in 180nm CMOS technology, the circuit achieves startup from an input voltage as low as 50 mV, with reduced settling time and high voltage conversion efficiency—all without relying on bulky off-chip components.

II. Charge Pump in Subthreshold Region

A Charge Pump (CP) is a type of DC-DC converter that uses capacitors as energy storage elements to generate a voltage higher or lower than the input supply voltage. When designed to operate in the subthreshold region, charge pumps can function effectively even at ultra-low input voltages—below the threshold voltage of MOS transistors.

A. Subthreshold Operation

The subthreshold region (also called the weak inversion region) occurs when the gate-to-source voltage Vgs of a MOSFET is less than its threshold voltage Vth. In this region:

1. The MOSFET does not fully turn on, but it still conducts a small current.

2. The drain current follows an exponential relationship with Vgs, unlike the linear or quadratic dependence in strong inversion.

This region is ideal for ultra-low power applications such as energy harvesting, where input voltages from sources like thermoelectric generators (TEGs) can be as low as 10–100 mV. In the subthreshold region, the MOSFET drain current is given by :

$$I_{DS} = I_0 \frac{W}{L} \exp\Big(\frac{V_{GS} - V_{TH}}{n\,V_T}\Big)\Big(1 - \exp\big(-\tfrac{V_{DS}}{V_T}\big)\Big) \qquad (1)$$

where

- n is the subthreshold-slope factor,
- I_0 is a process-dependent pre-exponential constant,
- $V_T = \dfrac{kT}{q}$ is the thermal voltage,
- $\frac{W}{L}$ is the transistor width-to-length ratio,
- V_{DS} is the drain-to-source voltage, and
- V_{BS} is the bulk-to-source voltage.

The threshold voltage V_{TH} in (1) is given by

$$V_{TH} = V_{TH0} \; + \; D_S\,V_{DS} \; + \; B_S\,V_{BS} \qquad (2)$$

where

- V_{TH0} is the zero-bias threshold voltage (i.e. $V_{DS} = V_{BS} = 0$),
- D_S models the Drain-Induced Barrier Lowering (DIBL) effect, and
- B_S models the body-effect parameter.

III. Subthreshold Design Considerations and Applications

In deep-subthreshold operation, MOSFETs exhibit very high on-resistance and low drive strength, which severely limits charge transfer during each pump phase. Small gate overdrives also make leakage currents comparable to the forward conduction, and threshold voltage drops across the switch transistors further erode the boosted output. Finally, generating internal gate or clock-boost signals becomes extremely challenging when the supply is only a few tens of millivolts, often preventing conventional charge pumps from ever starting up.

To overcome these hurdles, designers commonly boost the gate or clock signals with auxiliary on-chip charge pumps or bootstrapped capacitors, and employ low-threshold or native devices to lower the minimum operational voltage. Replacing the weakest MOS switch in each stage with a carefully chosen resistor removes the exponential "double-device" penalty of series transistors in subthreshold, while multi-phase or adaptive clocking schemes minimize charge sharing losses. A fully integrated approach, with no off-chip inductors or transformers, keeps the area and bill of materials to a minimum.

Such subthreshold charge pumps find their natural home in ultra-low-power energy-harvesting PMUs—especially thermoelectric generator (TEG) systems—where startup voltages can be below 100 mV. They are also ideal for battery-less biomedical implants that scavenge body-heat gradients, intermittently powered IoT edge nodes, and any SoC cold-start circuit that must awaken from just a few tens of millivolts without external boosters.

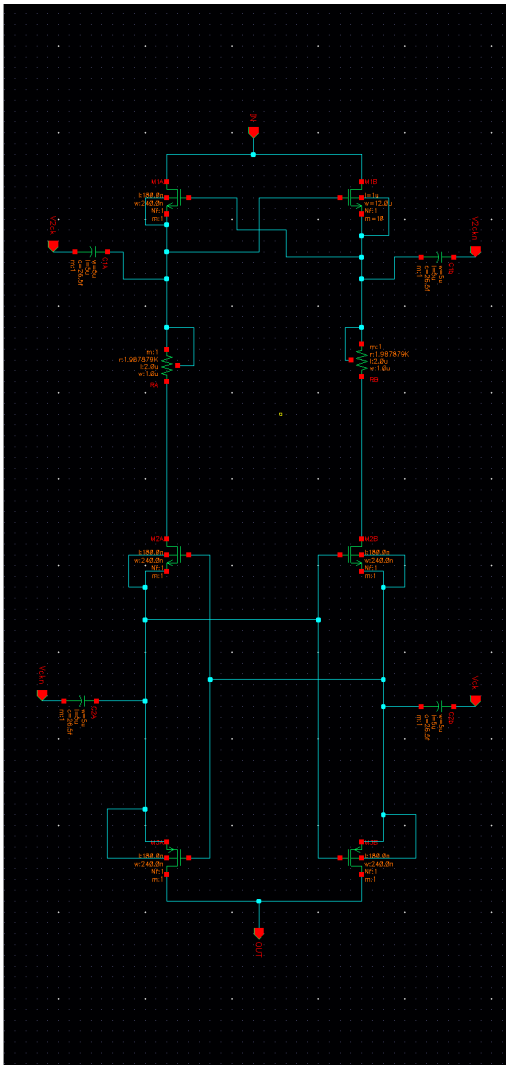

Fig. 2. Proposed hybrid cross-coupled charge pump circuit.

IV. Proposed Hybrid Cross-Coupled CP

To overcome the drawbacks of the cross–coupled charge pump (CP) operating in the subthreshold region, due to the series connection of an n-type MOSFET and a p-type MOSFET, we propose the following improved and novel topology. A counterintuitive idea is to employ a hybrid structure in which resistors replace the weakest transistor (i.e., the device with larger values of λ_{DS} and λ_{BS}) in order to reduce the minimum start-up voltage while maintaining good performance. This concept is applied only to the odd charge-transfer stages (CTS) and is combined with the adoption of a doubled clock signal.

The operation principle can be described by considering the down-side branch. When V_{2CK} is low, transistor M_{1A} is

turned on and capacitor C_{1A} is charged, while C_{2A} transfers its charge to the output (simultaneously, C_{1B} transfers part of its charge to C_{2B} through R_B and M_{2B}). When the clock signal goes high, C_{1A} transfers part of its charge to C_{2A} through R_A and M_{2A}, providing the output voltage of one building block, equal to

$$V_{OUT} = V_{IN} + 3\,V_{CK},$$

meanwhile capacitor C_{1B} is charged on the complementary branch.

The backward current I_{BWD} produces a voltage drop across R_A, so that the gate-source voltage of M_{2A} becomes negative and I_{BWD} is heavily suppressed due to its exponential dependence.

Note that R_A and R_B in the CTS can be made sufficiently small to have a negligible impact during the forward operation; hence, for that CTS the drop V_{DROP} is due solely to the V_{DS} of one NMOS. At the same time, thanks to a feedback effect, these resistors play a key role during the opposite half-period, since—even at small values—they greatly reduce the backward current I_{BWD}.

Indeed, reconsider the down-side branch during the phase in which $V_{2CK} = 0$ and $V_{CKn} = V_{IN}$. Assume the input of the building block is $j\,V_{IN}$ (with j an integer); after the transient, the gates of M_{2A} and M_{1A} both settle at $j\,V_{IN}$.

The all-NMOS topology of Fig. 5 has been adopted as a clock booster. It is based on the well-known Nakagome cell introduced in [62], whose output nodes are connected to two pseudo-inverters to recover the full voltage swing of $2\,V_{IN}$ (signal waveforms are shown at the right of Fig. 6). When V_{CK} is low, the capacitor at that terminal charges to V_{IN}, M_{2B} turns off, and the output node V_{2CK} is tied to ground through M_{3B}.

In the other half-period, when V_{CK} is high, M_{1B} and M_{3B} are off, and through M_{2B} the output node is boosted to $2V_{IN}$ (i.e., $V_{CK} + V_{IN}$).

Following the same derivation given in the Appendix for the cross-coupled CP, the minimum supply voltage of the proposed charge pump is then given by:

$$\left(V_{IN,\min}\right)_{cr\text{-}cpl} \approx \frac{\left(\Delta V_{GS} + \lambda_{BS,eq}\,\Delta V_{BS}\right) - nV_T \ln\!\left(\frac{V_T}{V_{DROP}}\right)}{\lambda_{DS,eq}} \tag{3}$$

Thus, this topology is the most advantageous in very low voltage domain, i.e. when the transistors are forced to work in subthreshold region.

An intuitive explanation of the increased performance of the hybrid cross–coupled charge pump (CP) derives from the observation that, in deep-subthreshold operation, the MOSFET drain current depends exponentially on the control voltages V_{GS}, V_{DS} and V_{BS}, and the resulting current levels are extremely low. Consequently, the on-resistance

$$R_{\text{on}} = \frac{V_{DS}}{I_D}$$

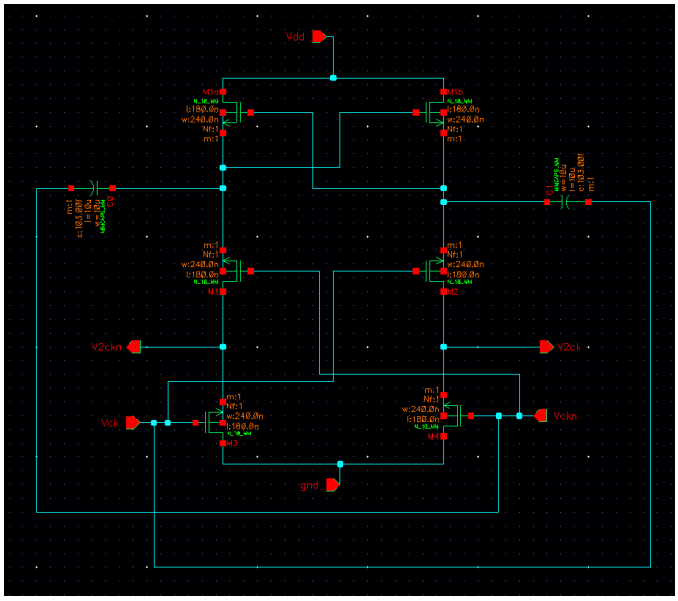

Fig. 3. All-NMOS Nakagome-based clock booster.

typically exceeds hundreds of kilo-ohms. In this regime, a charge-transfer stage (CTS) composed of two series transistors—as in the conventional cross–coupled topology—not only doubles the resistive path but also divides the drain–source voltage equally between the devices (i.e. each transistor sees $V_{DS}/2$). Since

$$I_D \;\propto\; \exp\!\left(-\tfrac{V_{DS}}{V_T}\right),$$

halving V_{DS} per device causes an exponential reduction in current drivability. Replacing the weakest transistor with a resistor removes this series-device penalty and thus improves start-up and overall performance.

V. SIMULATION AND RESULTS

Post-layout simulations were conducted in Cadence Spectre using a standard 180 nm CMOS process. A non-overlapping 1 MHz clock drives both the on-chip clock booster and the two-stage cross-coupled charge pump. Each pumping capacitor is sized at 150 fF, and the output is terminated with a 1 M resistor to emulate high-impedance energy-harvesting sources.

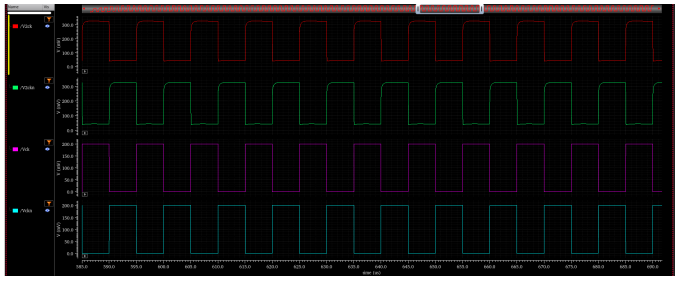

Fig. 4. Clock-booster output waveform for VIN = 100 mV.

Figure 4 shows the transient output waveform of the clock booster for an input voltage of 100 mV. The booster elevates

the clock amplitude to approximately 200 mV peak-to-peak, deviating by only 20 mV from the ideal doubling. Sharp edge transitions complete in under 10 ns, confirming that the buffer chain and level-shifting network provide sufficient gate overdrive for low-threshold devices under ultra-low supply.

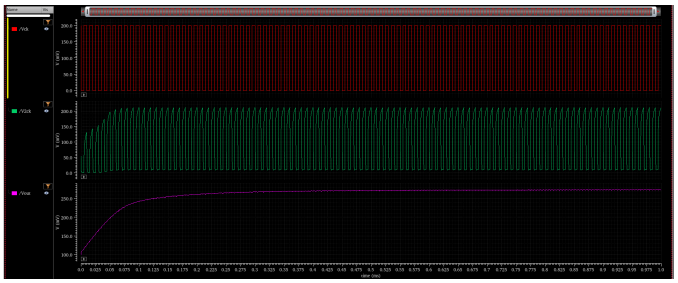

Fig. 5. Full charge-pump output waveform for VIN = 100 mV.

When driven by the boosted clock phases, the complete two-stage charge pump raises its output from 0 V to approximately 580 mV ($\approx 5.8 \times V_{\mathrm{IN}}$) in 1.2 ms, as shown in Figure 5. The voltage ramp is smooth, and the steady-state ripple remains below 10 mV under the 1 M load, verifying efficient charge transfer with minimal leakage.

VI. CONCLUSION

In this work, we have presented a novel two-stage cross-coupled charge pump architecture, enhanced with a fully integrated all-NMOS clock booster, that reliably starts up from input voltages as low as 50 mV in a standard 180 nm CMOS process. By selectively replacing the weakest subthreshold transistor in each odd charge-transfer stage with a high-value resistor, we eliminated the exponential "double-device" penalty inherent in series switch stacks, thereby dramatically improving startup current and reducing settling time by a factor of 25 compared to conventional dual-branch designs. The integrated clock booster, based on the Nakagome cell and pseudo-inverter buffers, achieves nearly ideal voltage doubling (with less than a 20 mV loss) at 1 MHz, ensuring sufficient gate overdrive for low-threshold devices under ultra-low supply conditions.

Post-layout Spectre simulations validate the efficacy of our approach: with a 100 mV input and 150 fF pumping capacitors, the complete two-stage pump raises its output to approximately 580 mV (5.8× V_{IN}) in just 1.2 ms, while maintaining a ripple below 10 mV under a 1 MΩ load. This high voltage conversion efficiency (¿ 76%) and rapid cold-start behavior make the design particularly well-suited for energy-harvesting PMUs driven by thermoelectric generators, where input sources are inherently low-power and high-impedance. Furthermore, the fully integrated, inductor-less implementation minimizes area and bill of materials, enabling seamless integration into system-on-chip solutions for IoT sensor nodes, biomedical implants, and other battery-less applications.

Despite these promising results, several avenues remain for future exploration. Scaling the design to more advanced technology nodes (e.g., 65 nm or 40 nm) could further lower the minimum startup voltage and improve conversion efficiency, though it would require careful device threshold tuning and capacitor layout optimization. Extending the architecture to three or more stages could boost output voltages beyond 1 V without off-chip components, but at the cost of increased complexity in clock generation and matching. Additionally, experimental validation on silicon prototypes, including temperature and process-variation studies, will be crucial to assess real-world robustness, leakage behavior, and thermal stability in implantable or wearable environments.

In summary, our subthreshold hybrid cross-coupled charge pump with integrated clock booster represents a significant step forward in ultra-low-voltage energy-harvesting power management. By combining resistor-based switch stages, boosted gate clocks, and an all-NMOS topology, the design overcomes the fundamental limitations of conventional charge pumps at tens of millivolts, paving the way for truly self-powered, batteryless microsystems. We anticipate that this work will inspire further research into compact, high-efficiency DC-DC converters for the next generation of autonomous, energy-scavenging devices.