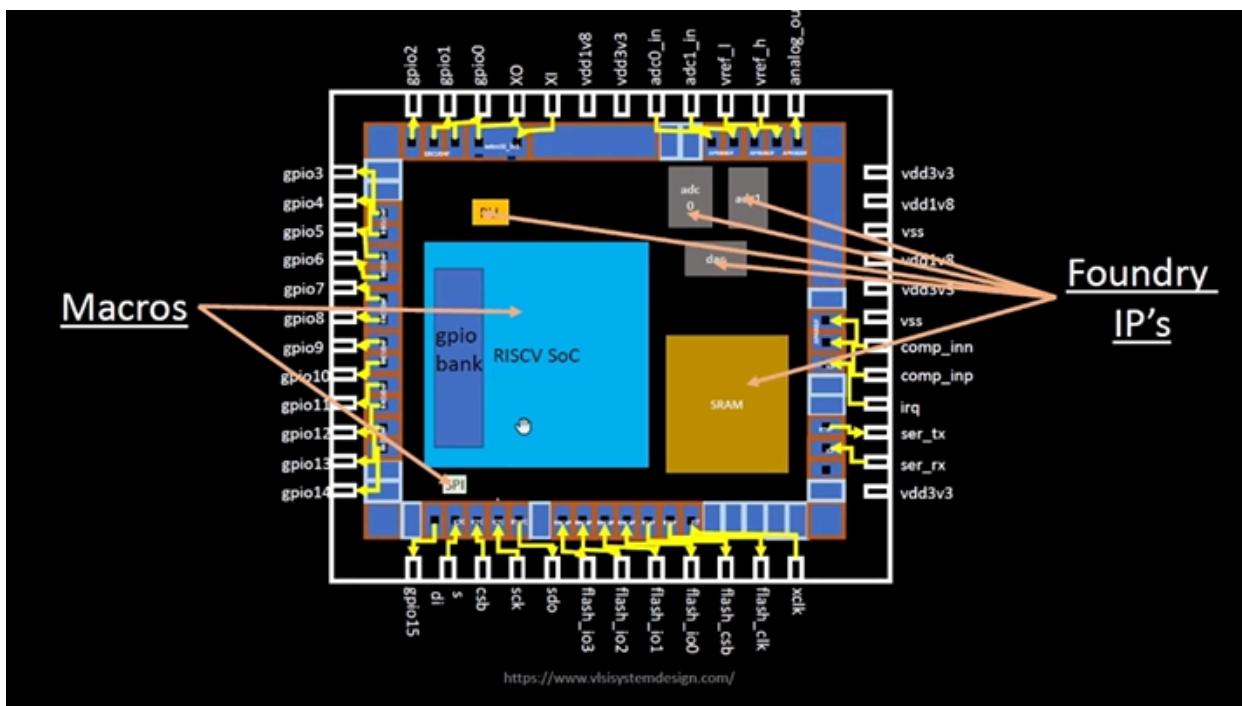
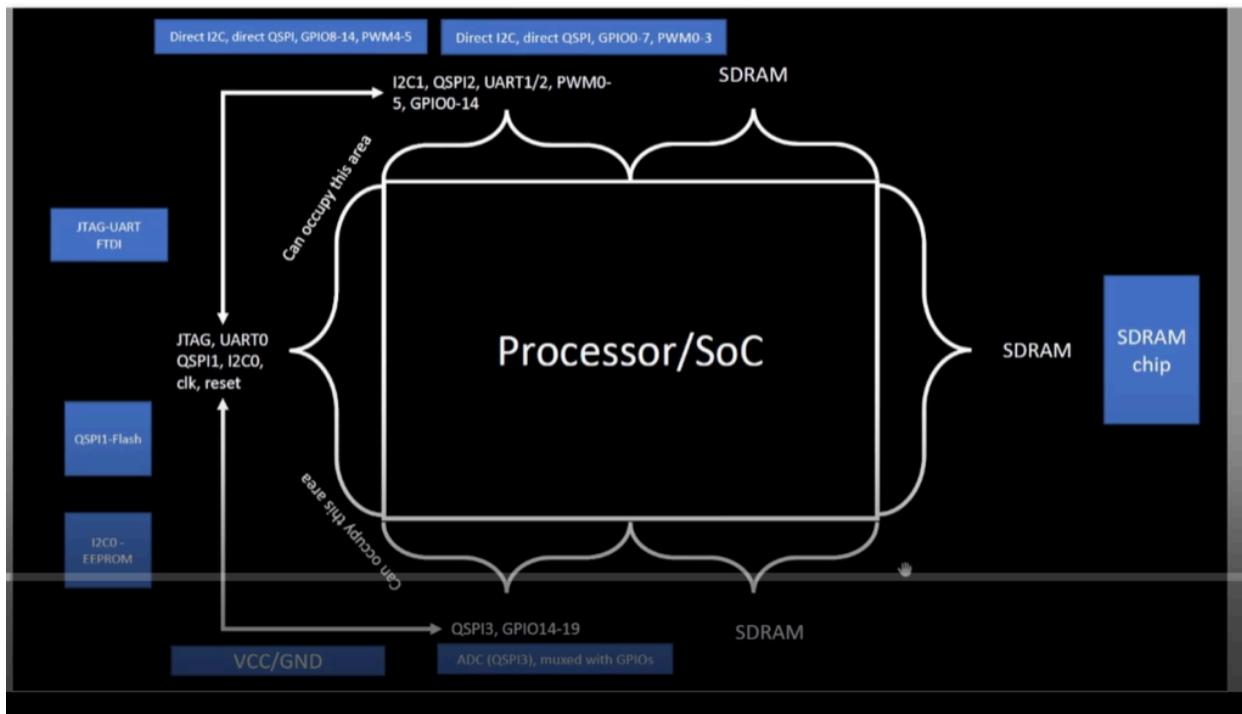


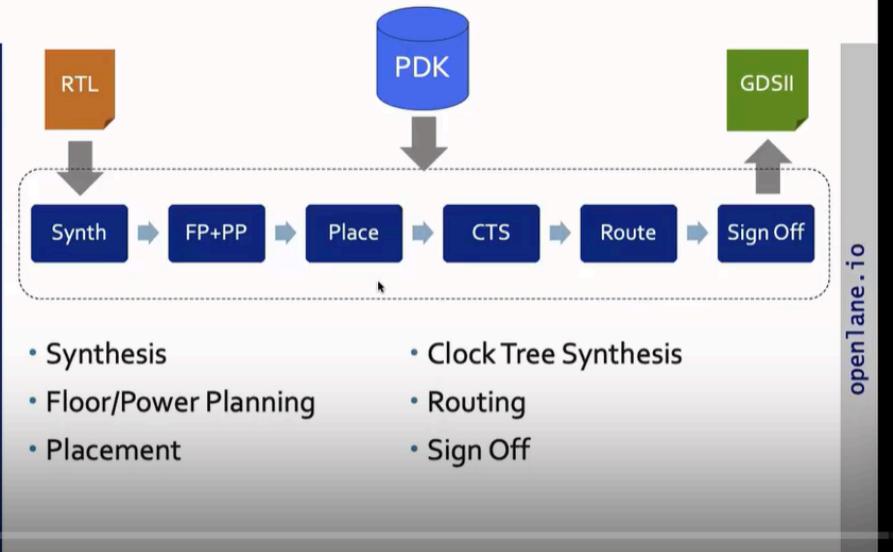
Tab 1

Placement and RTL to GDSII flow of chip design overview:

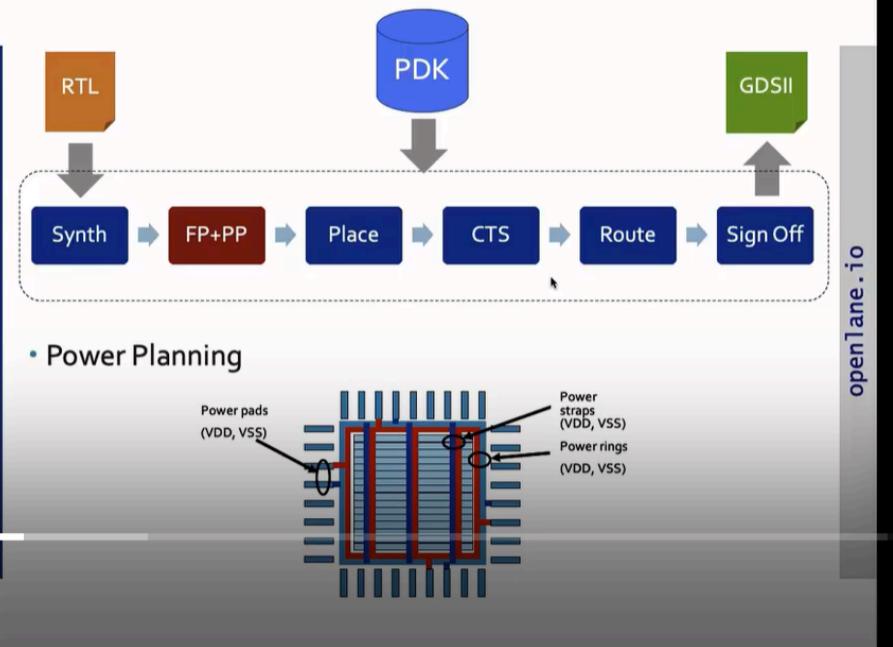


Ip: Intellectual property

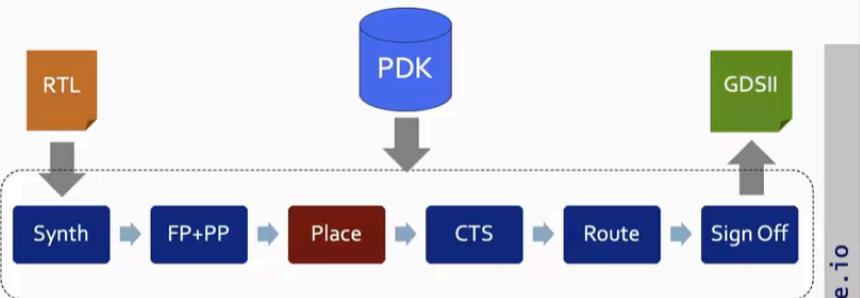
Simplified RTL to GDSII Flow



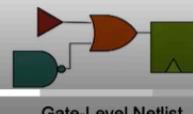
Floor and Power Planning



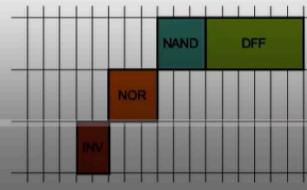
Placement



- Place the cells on the floorplan rows, aligned with the sites

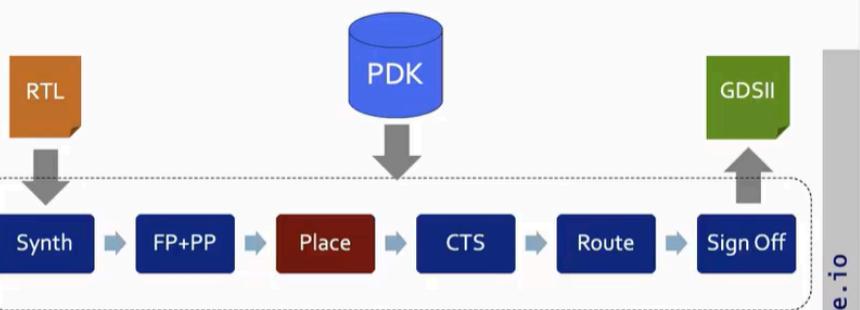


Gate-Level Netlist

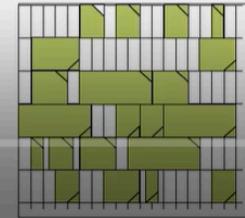
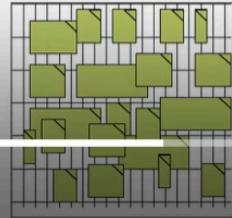


26

Placement

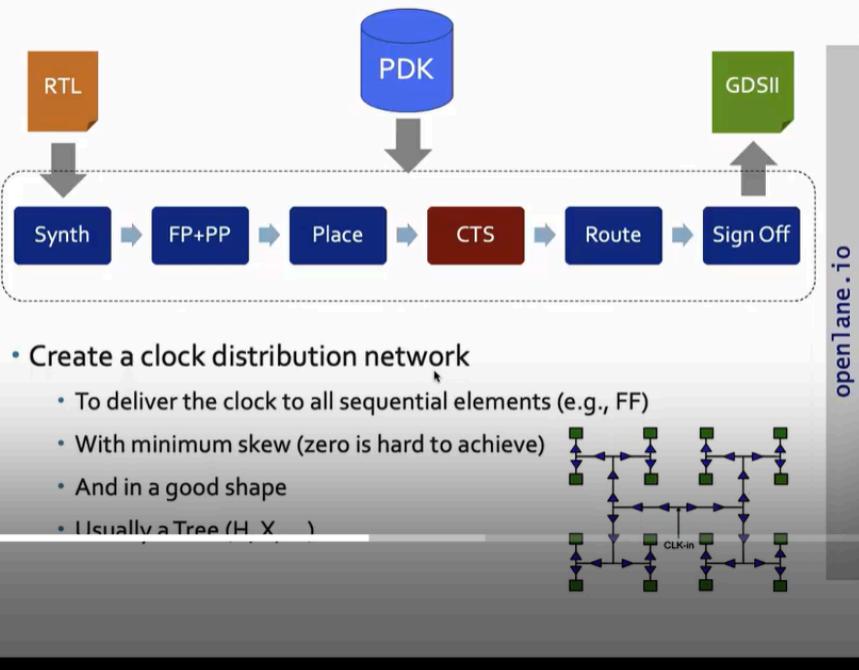


- Usually done in 2 steps: Global and Detailed

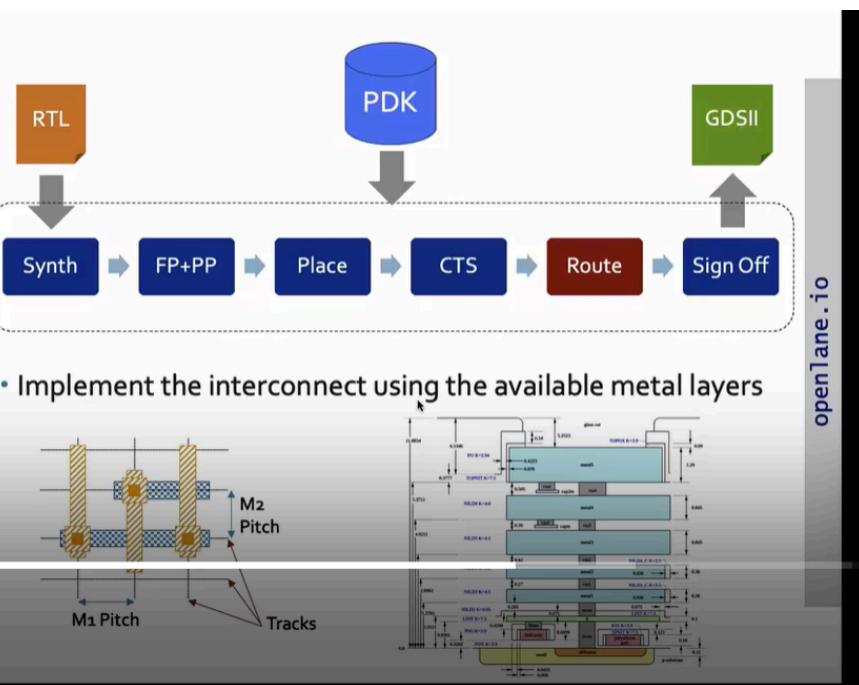


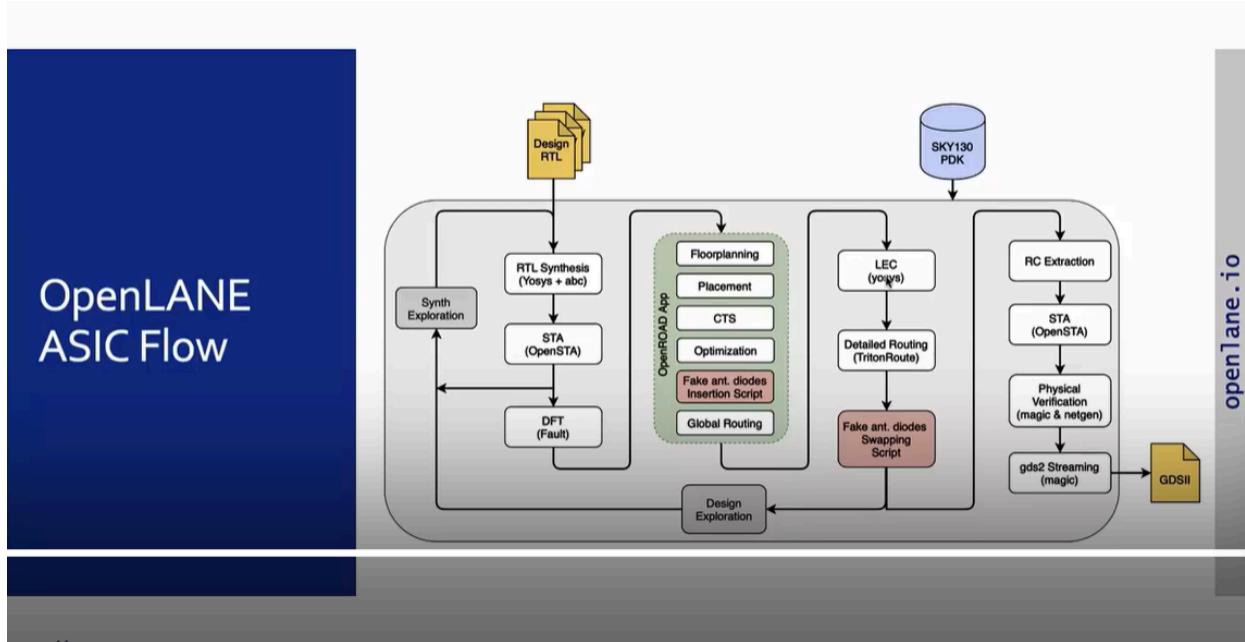
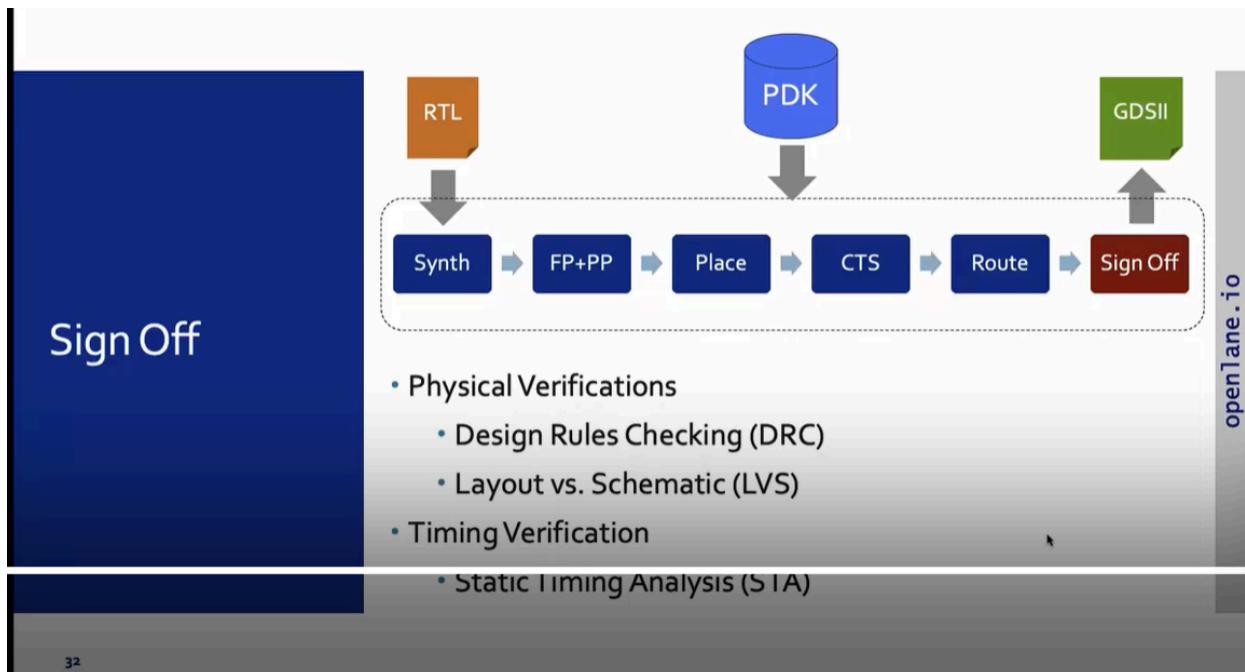
28

Clock Tree Synthesis



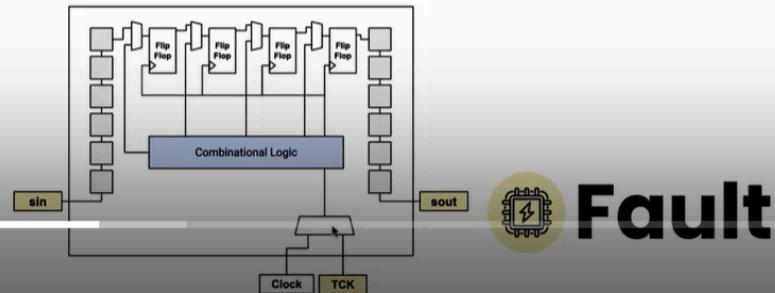
Routing





Design for Test (DFT)

- Scan Insertion
- Automatic Test Pattern Generation (ATPG)
- Test Patterns Compaction
- Fault Coverage
- Fault Simulation



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Logic Equivalence Check (LEC)

- Every time the netlist is modified, verification must be performed
 - CTS modifies the netlist
 - Post Placement optimizations modifies the netlist
- LEC is used to formally confirm that the function did not change after modifying the netlist

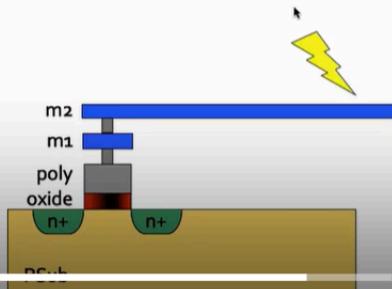
Yosys

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Dealing with Antenna Rules Violations

- When a metal wire segment is fabricated, it can act as an antenna.
 - Reactive ion etching causes charge to accumulate on the wire.
 - Transistor gates can be damaged during fabrication

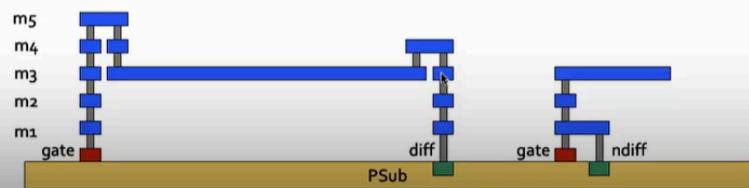


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Dealing with Antenna Rules Violations

- Two solutions:
 - Bridging attaches a higher layer intermediary
 - Requires Router awareness (not there yet!)
 - Add antenna diode cell to leak away charges
 - Antenna diodes are provided by the SCL

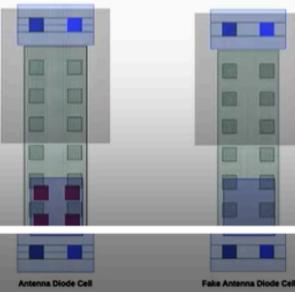


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Dealing with Antenna Rules Violations

- We took a preventive approach
 - Add a Fake Antenna Diode next to every cell input after placement
 - Run the Antenna Checker (Magic) on the routed layout
 - If the checker reports a violation on the cell input pin, replace the Fake Diode cell by a real one



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Physical Verification DRC & LVS

- Magic is used for Design Rules Checking and SPICE Extraction from Layout
- Magic and Netgen are used for LVS
 - Extracted SPICE by Magic vs. Verilog netlist

netgen

Magic VLSI Layout Tool

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Layout parameters:

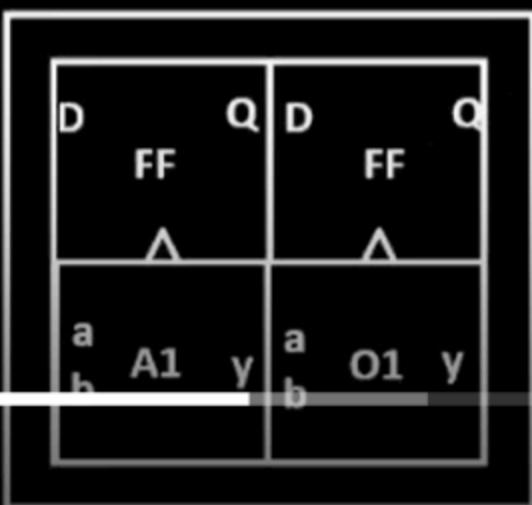
1) Define Width and Height of Core and Die

How to arrive on its dimensions?

Place all logical cells inside the 'core'

The logical cells occupies the complete
area of the core

100 % Utilization

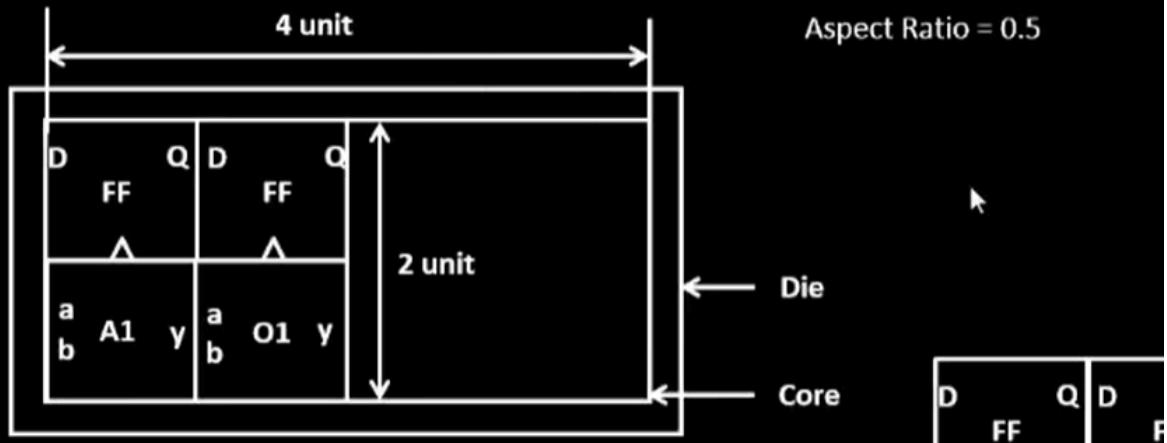


(Area Occupied by Netlist)

Utilization Factor = $\frac{\text{(Area Occupied by Netlist)}}{\text{(Total Area of the Core)}}$

1) Define Width and Height of Core and Die

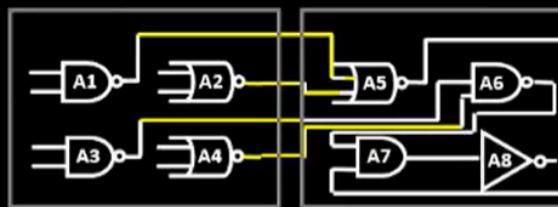
Utilization Factor = 0.5



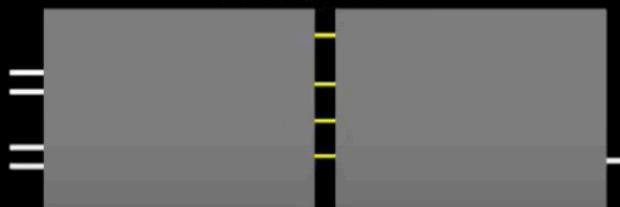
2) Define Locations of Preplaced Cells

Block 1

Block 2



Black Box the boxes



Separate the Black Boxes as two different IP's or modules



2) Define Locations of *Preplaced Cells*

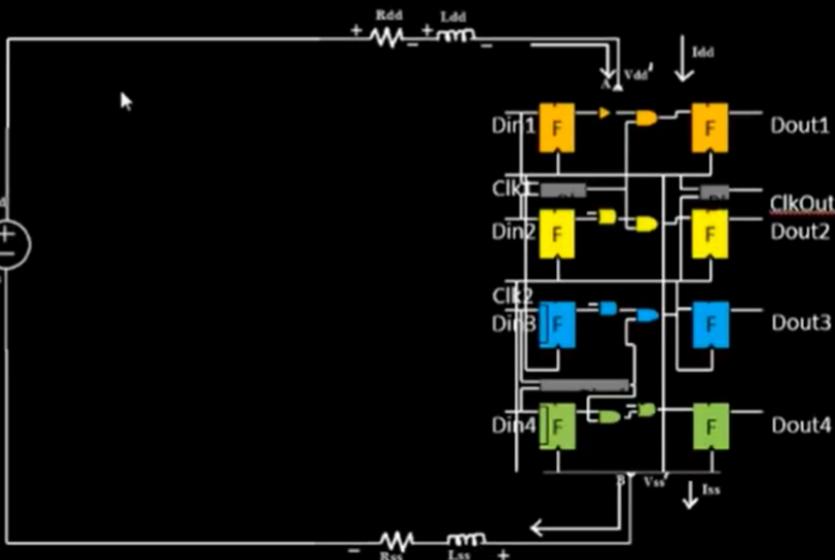
- Similarly, there are other IP's also available, for eg.



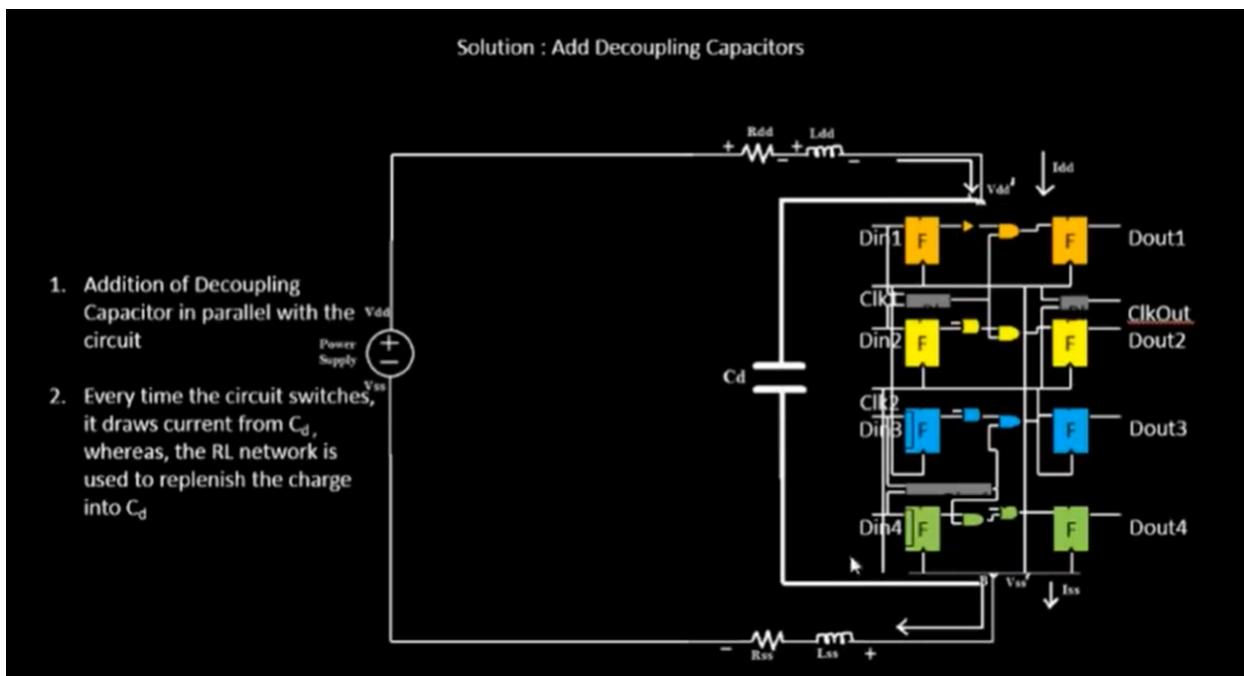
- The arrangement of these IP's in a chip is referred as Floorplanning
- These IP's/blocks have user-defined locations, and hence are placed in chip before automated placement-and-routing and are called as *pre-placed cells*.
- Automated placement and routing tools places the remaining logical cells in the design onto chip

Consider the amount of the switching current required
for a complex circuit something like below

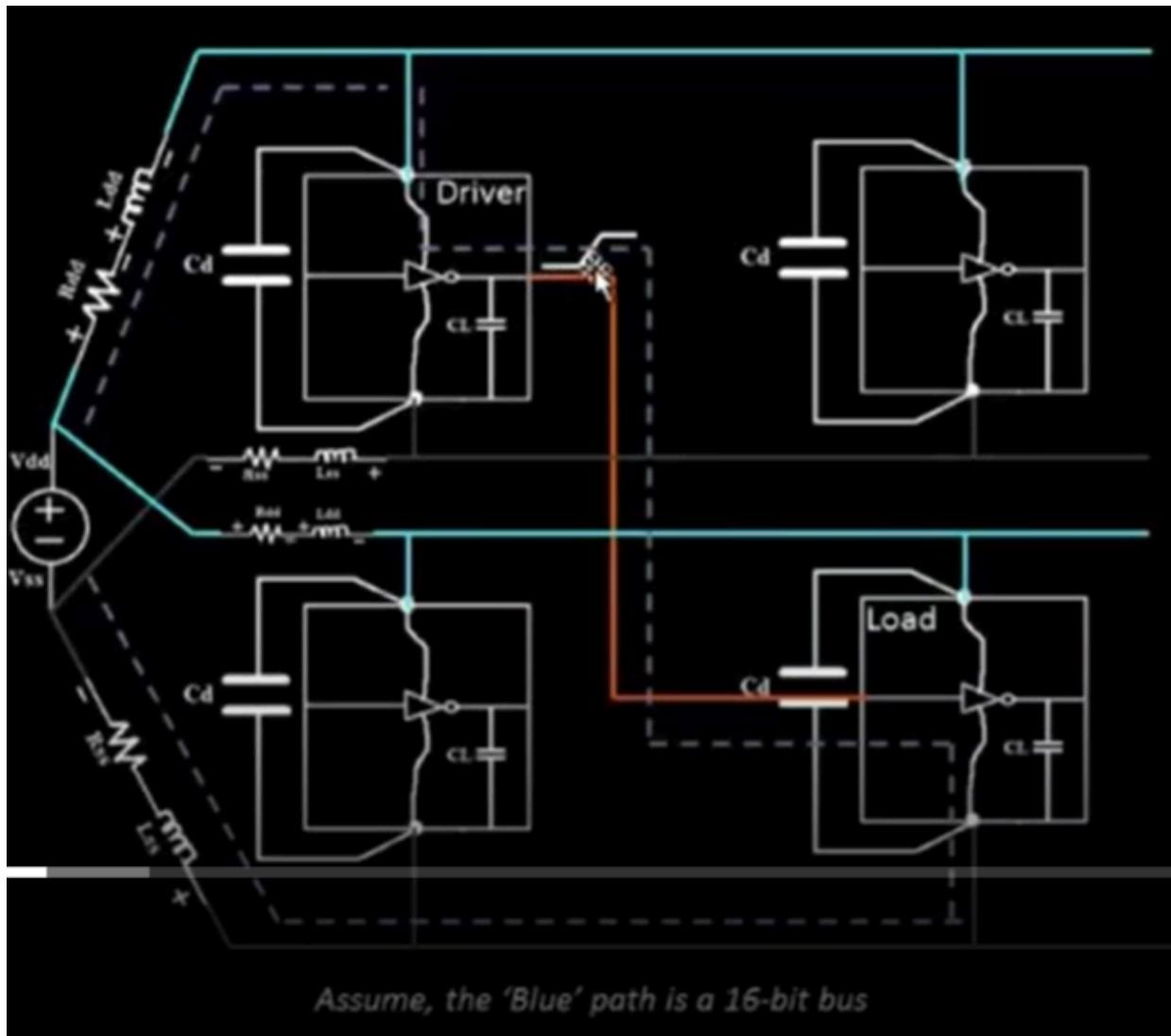
- Consider capacitance to be zero for the discussion.
 R_{dd} , R_{ss} , L_{dd} and L_{ss} are well defined values.
- During switching operation, the circuit demands switching current i.e. peak current (I_{peak}).
- Now, due to the presence of R_{dd} and L_{dd} , there will be a voltage drop across them and the voltage at Node 'A' would be V_{dd}' instead of V_{dd} .

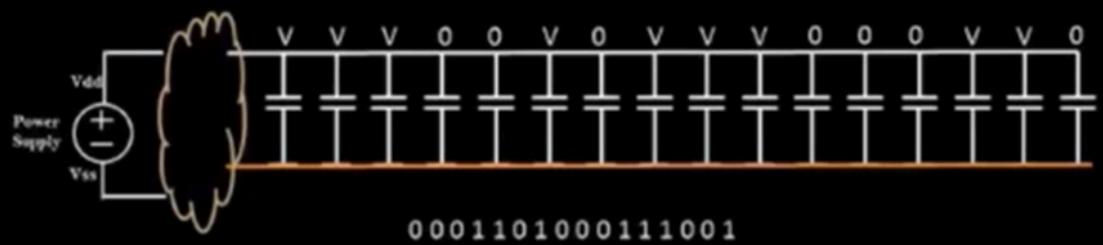


Solution : Add Decoupling Capacitors



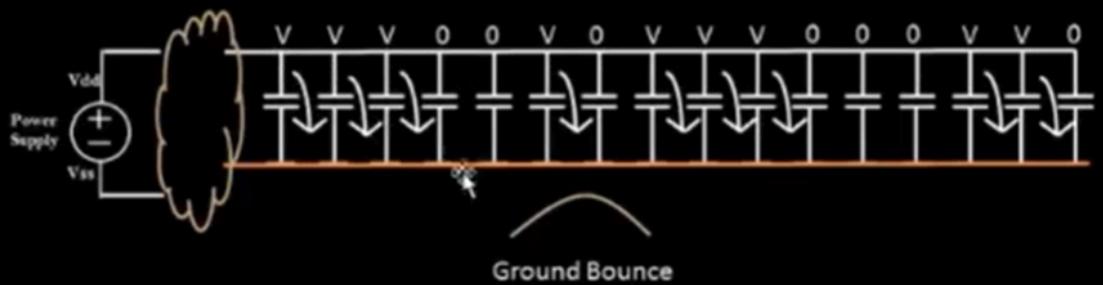
Power planning - several such circuit blocks



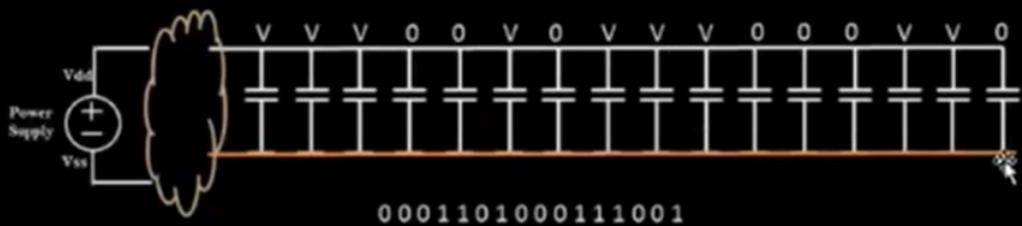


What does this mean?

This means, all capacitors which were charged to ' V ' volts will have to discharge to '0' volts through single 'Ground' tap point. This will cause a bump in 'Ground' tap point.

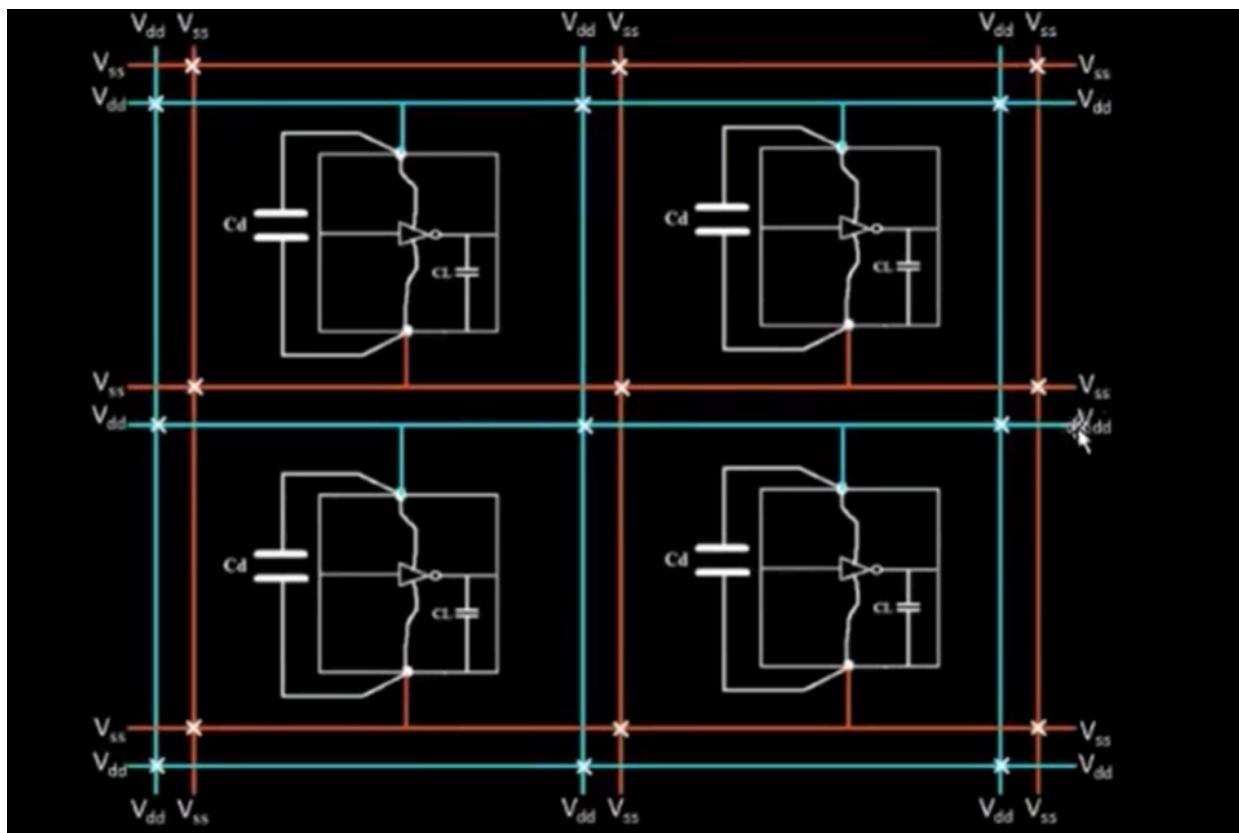
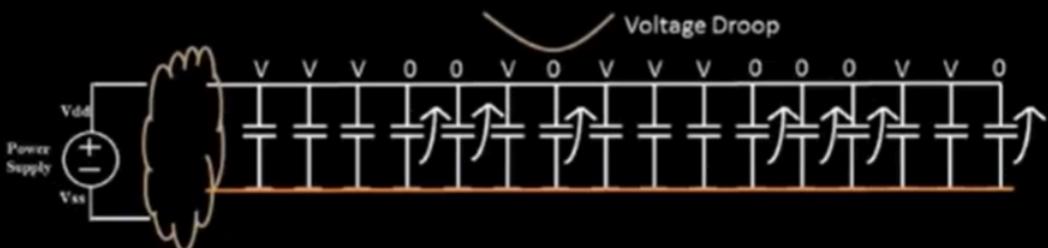


Ground bounce>noise margin - my result in uncertainty



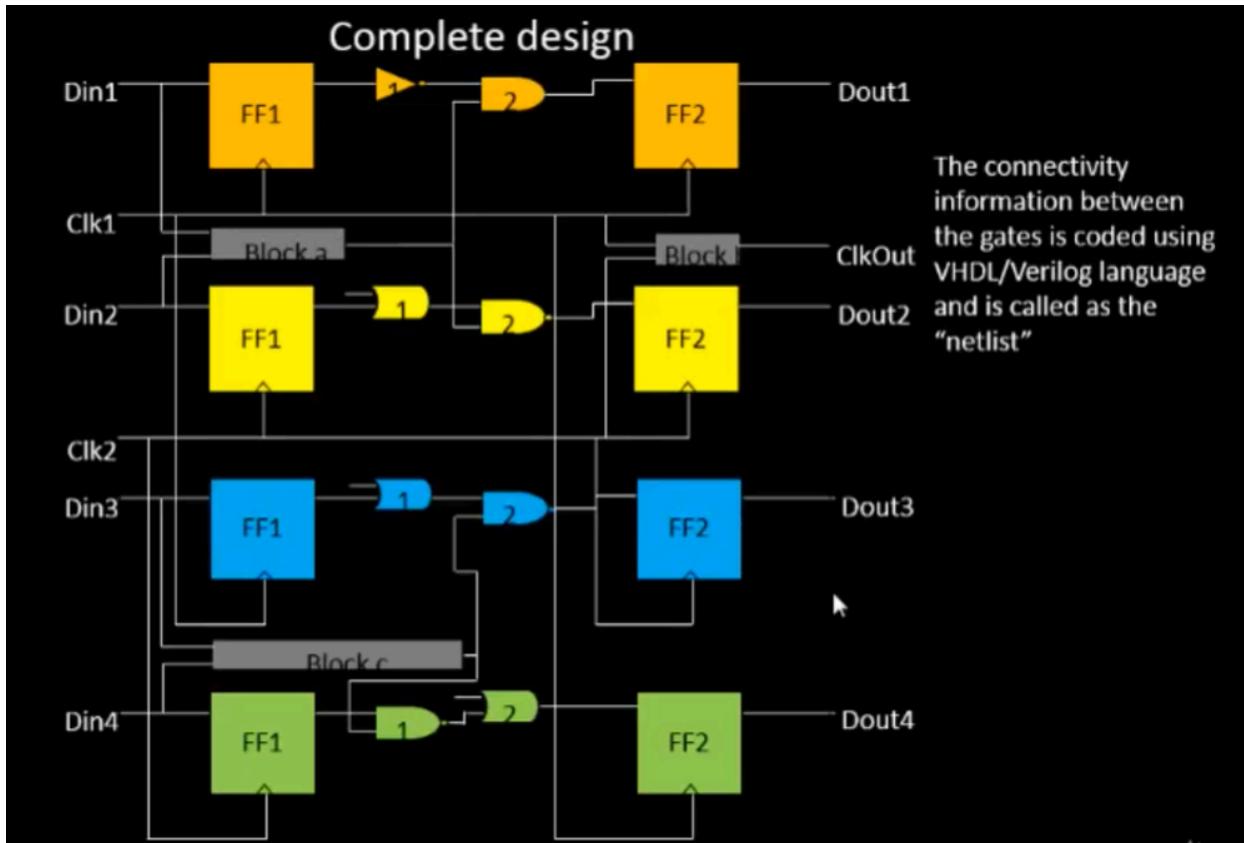
What does this mean?

Also, all capacitors which were '0' volts will have to charge to 'V' volts through single 'Vdd' tap point. This will cause lowering of voltage at 'Vdd' tap point.



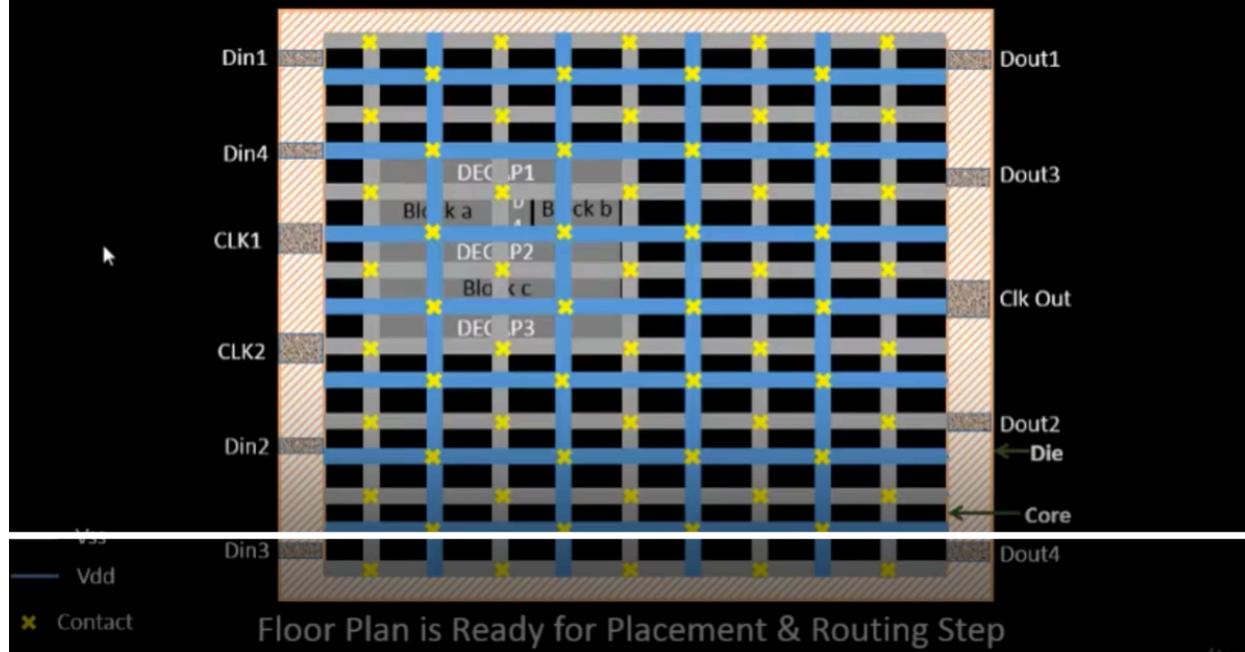
Multiple power supplies

Pin placement / connections

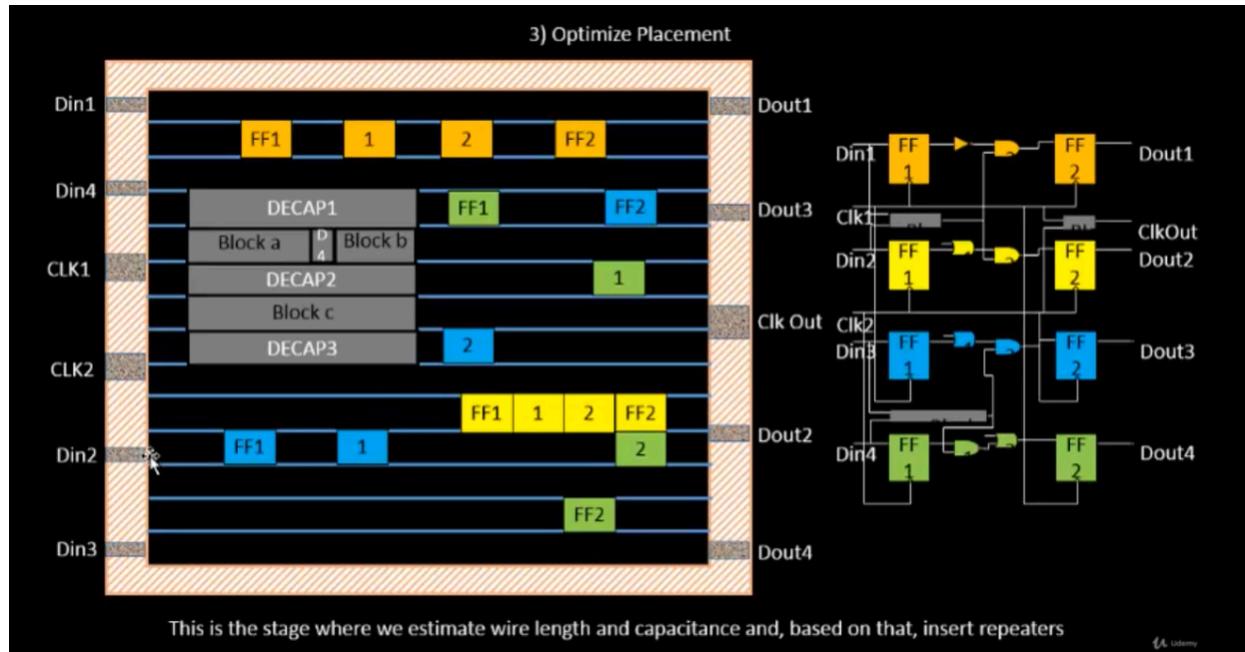


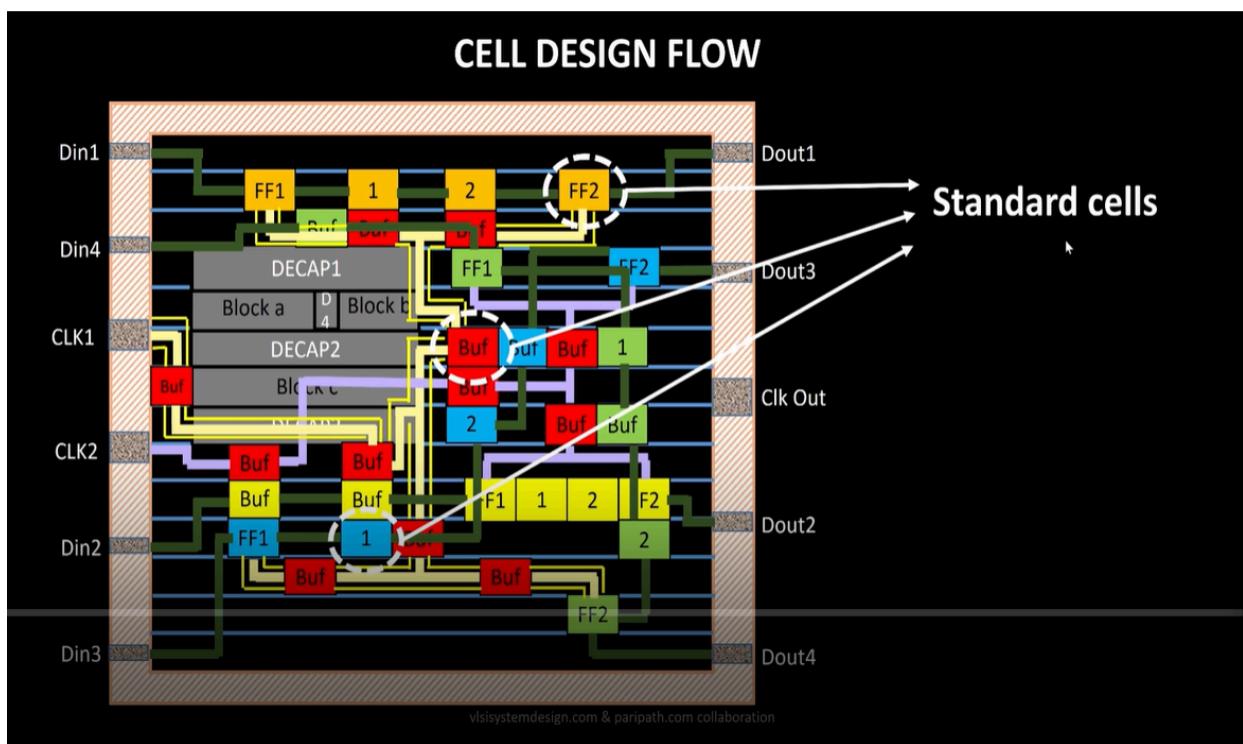
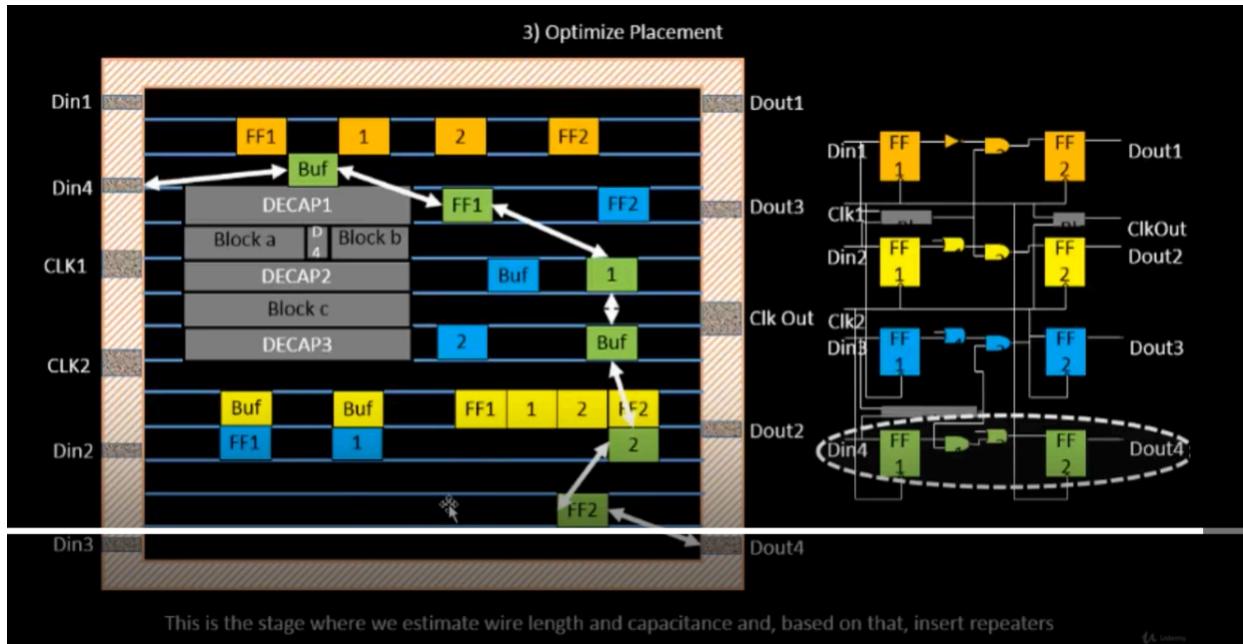
We need least resistance paths for the clocks

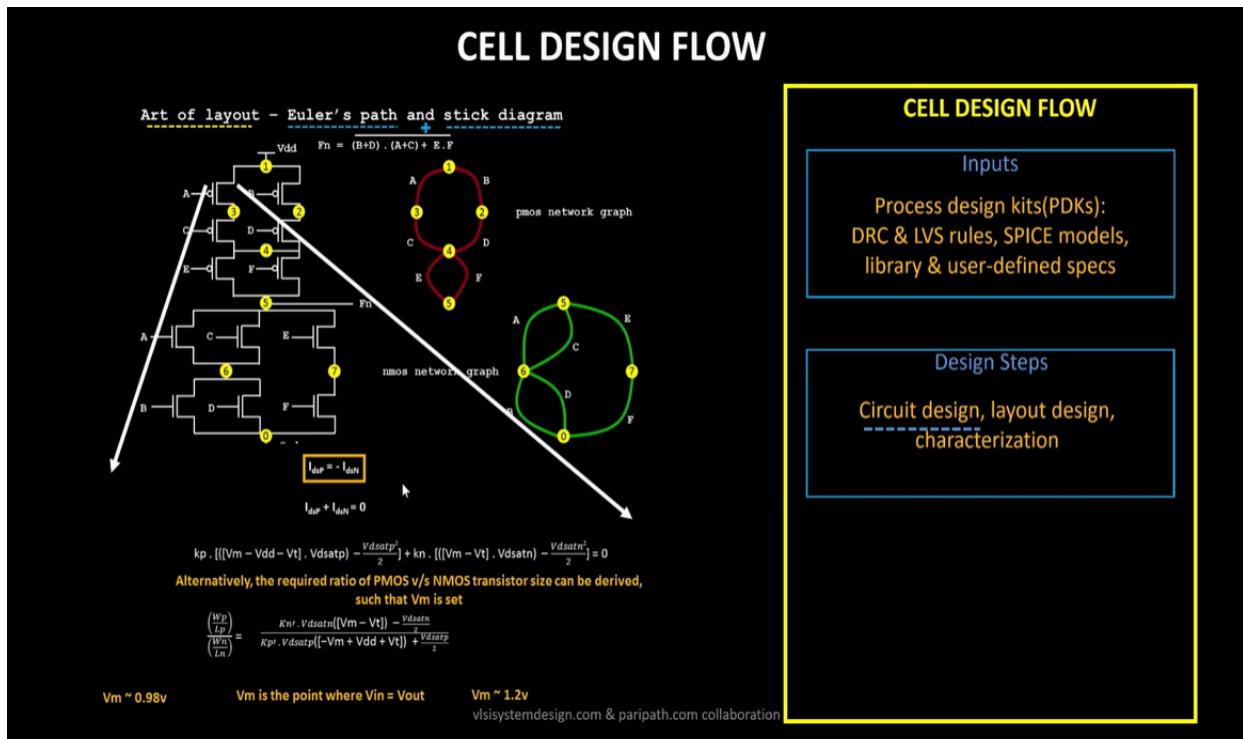
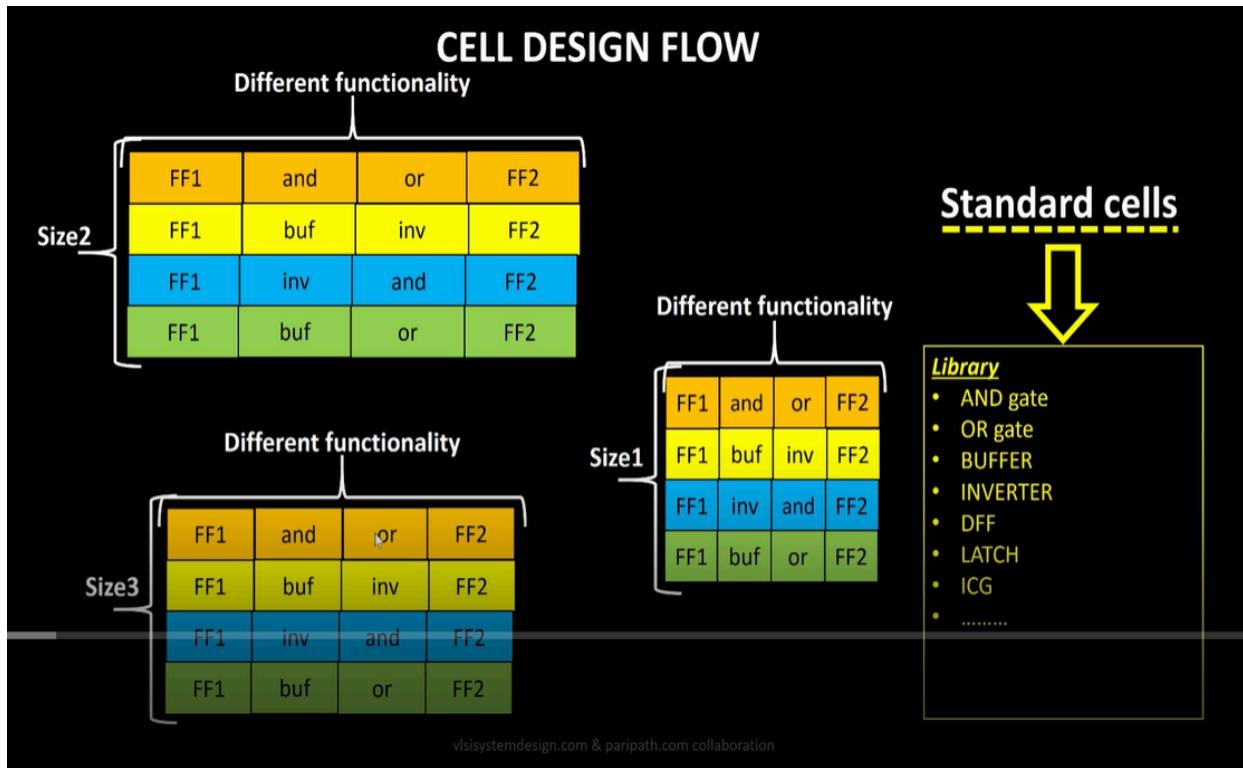
6) Logical Cell Placement Blockage



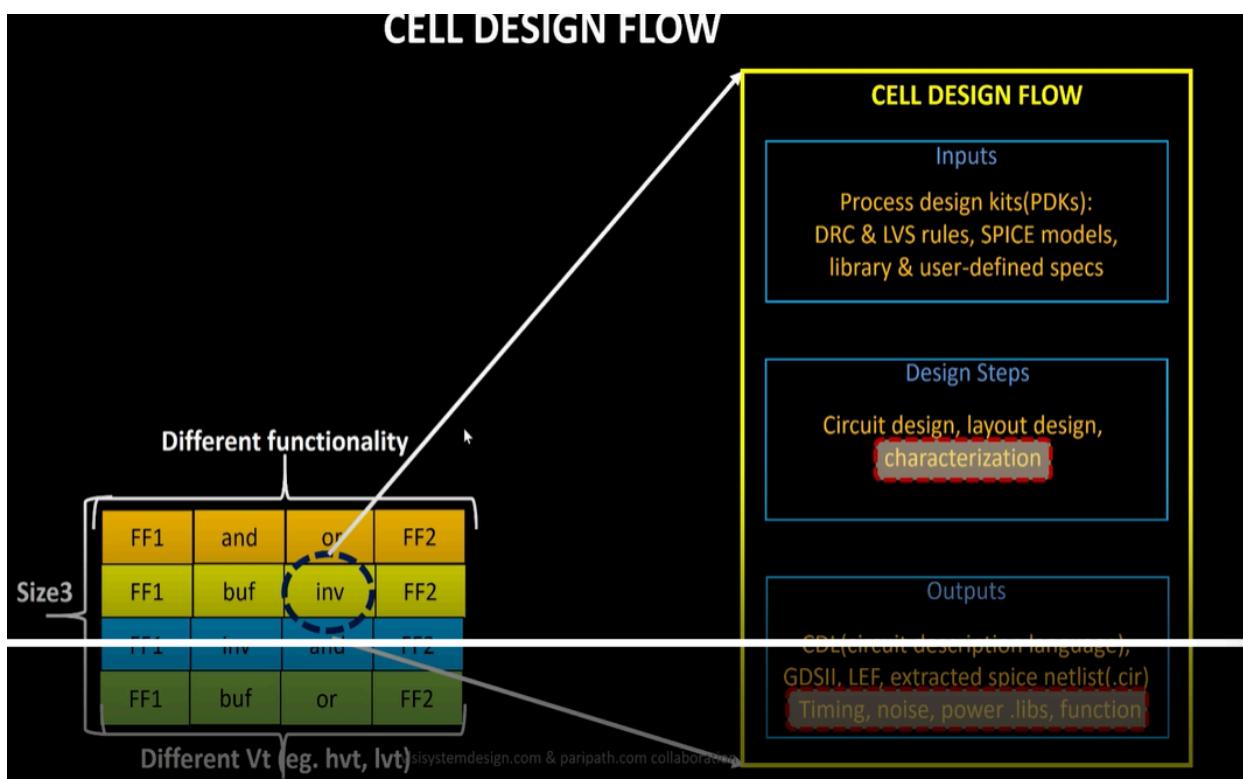
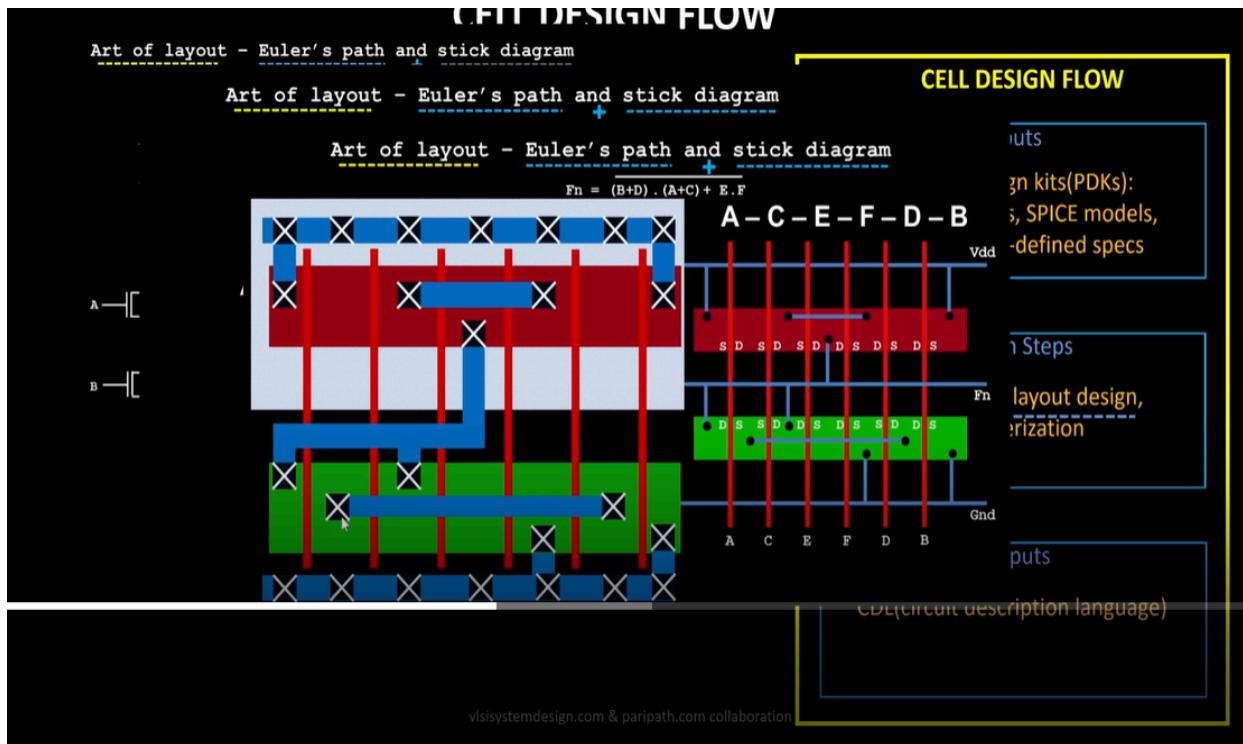
3) Optimize Placement

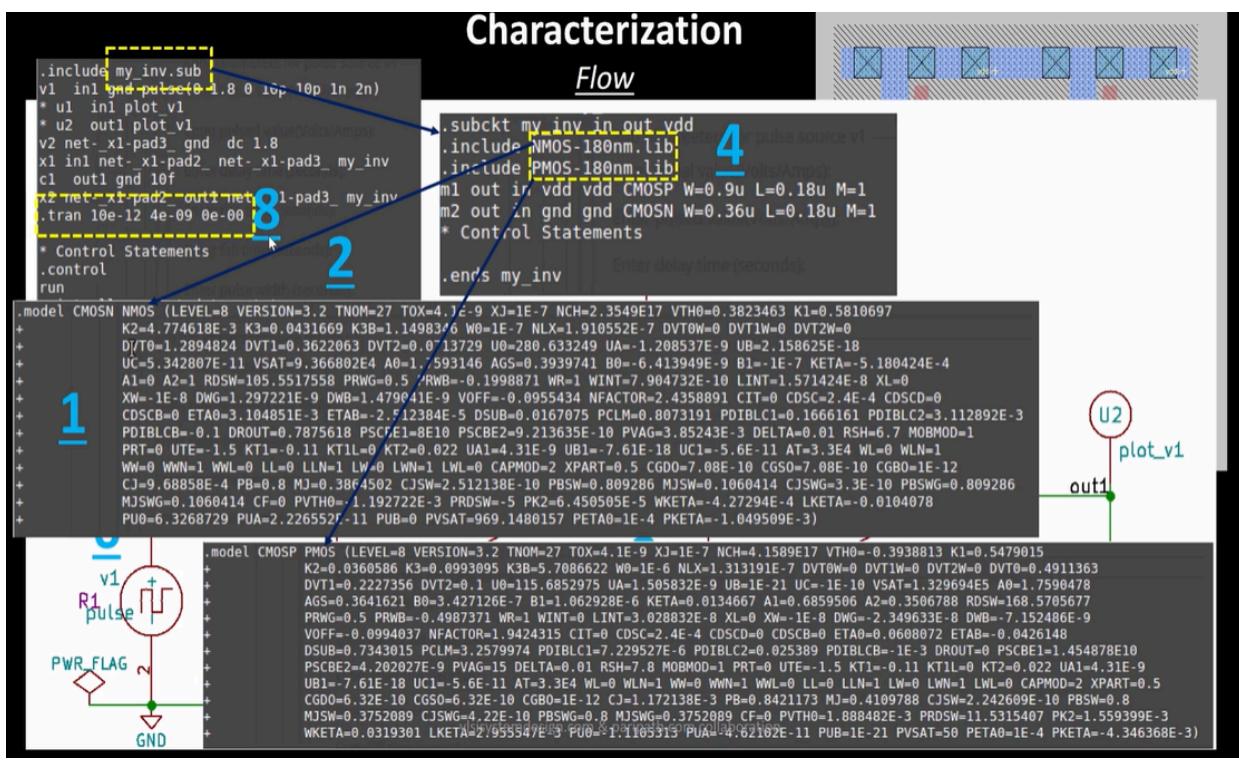
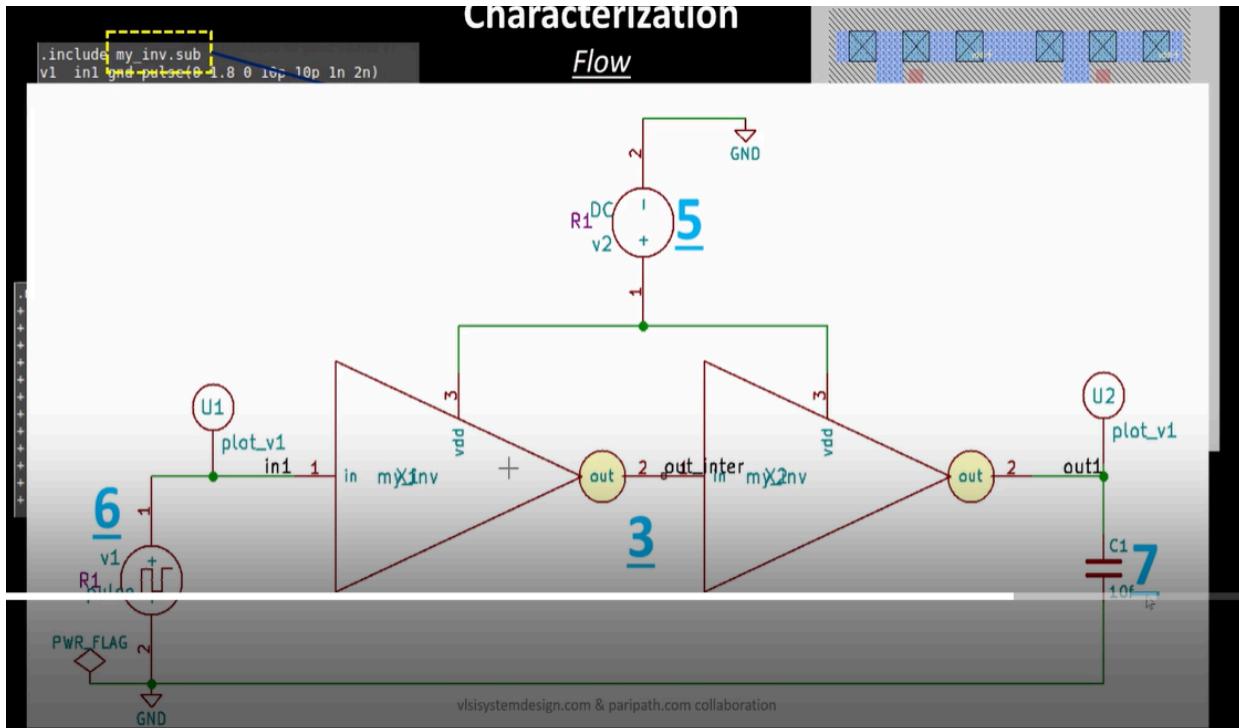






Output: CDL: Circuit description language

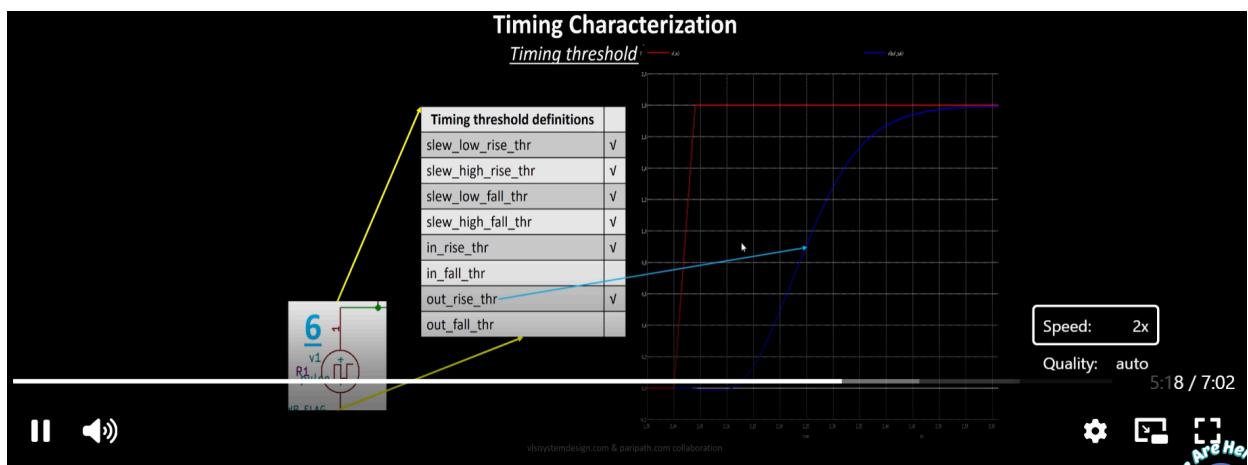




Characterization



vlsisystemdesign.com & paripath.com collaboration



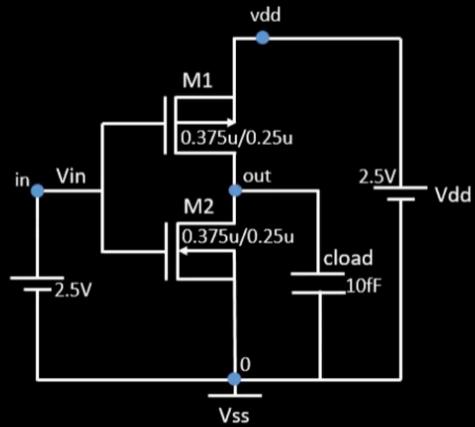
NGSpice

SPICE deck

```
*** MODEL Descriptions ***
*** NETLIST Description ***
M1 out in vdd vdd pmos W=0.375u L=0.25u
M2 out in 0 0 nmos W=0.375u L=0.25u

cload out 0 10f

Vdd vdd 0 2.5
Vin in 0 2.5
*** SIMULATION Commands ***
.op
.dc Vin 0 2.5 0.05
*** .include tsmc_025um_model.mod ***
.lib "tsmc_025um_model.mod" CMOS_MODELS
.end
```

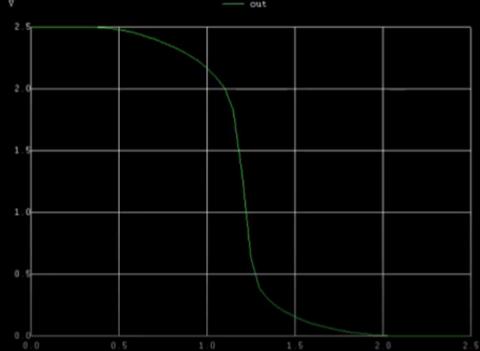
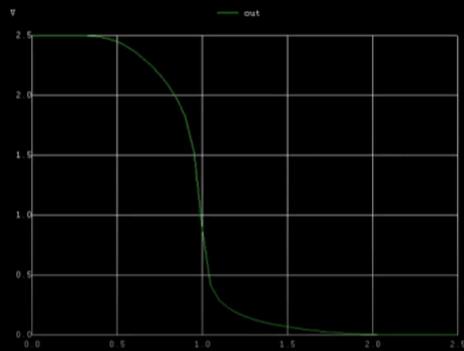


SPICE waveform : $W_n=W_p=0.375\mu$,
 $L_n,p=0.25\mu$ device
 $(W_n/L_n=W_p/L_p = 1.5)$

SPICE waveform : $W_n=0.375$, $W_p=0.9375\mu$,
 $L_n,p=0.25\mu$ device
 $(W_n/L_n=1.5, W_p/L_p = 3.75)$

Static behavior Evaluation : CMOS inverter Robustness

1. Switching Threshold, V_m



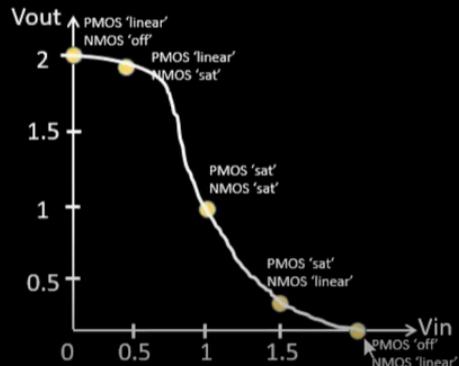
V_m is the point where $V_{in}=V_{out}$

SPICE waveform : $W_n=W_p=0.375\mu$,
 $L_n,p=0.25\mu$ device
($W_n/L_n=W_p/L_p = 1.5$)

SPICE waveform : $W_n=0.375$, $W_p=0.9375\mu$,
 $L_n,p=0.25\mu$ device
($W_n/L_n=1.5$, $W_p/L_p = 3.75$)

Static behavior Evaluation : CMOS inverter Robustness

1. Switching Threshold, V_m



$V_m \sim 0.98v$

V_m is the point where $V_{in} = V_{out}$

$V_m \sim 1.2v$

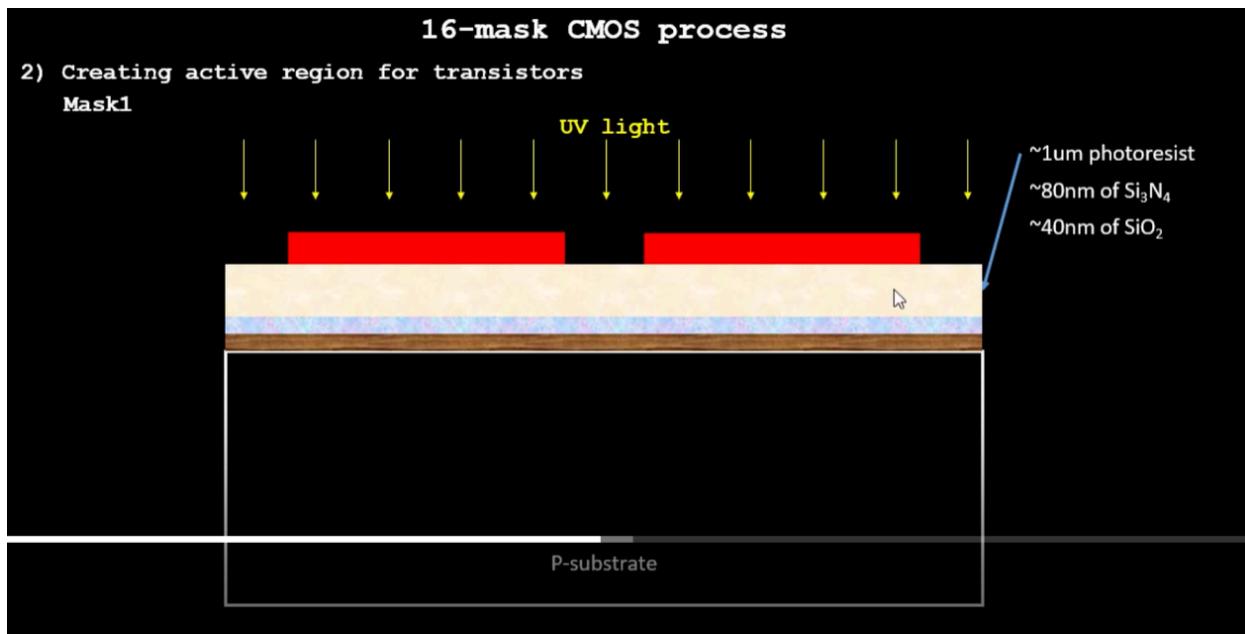
Lithography:

16-mask CMOS process

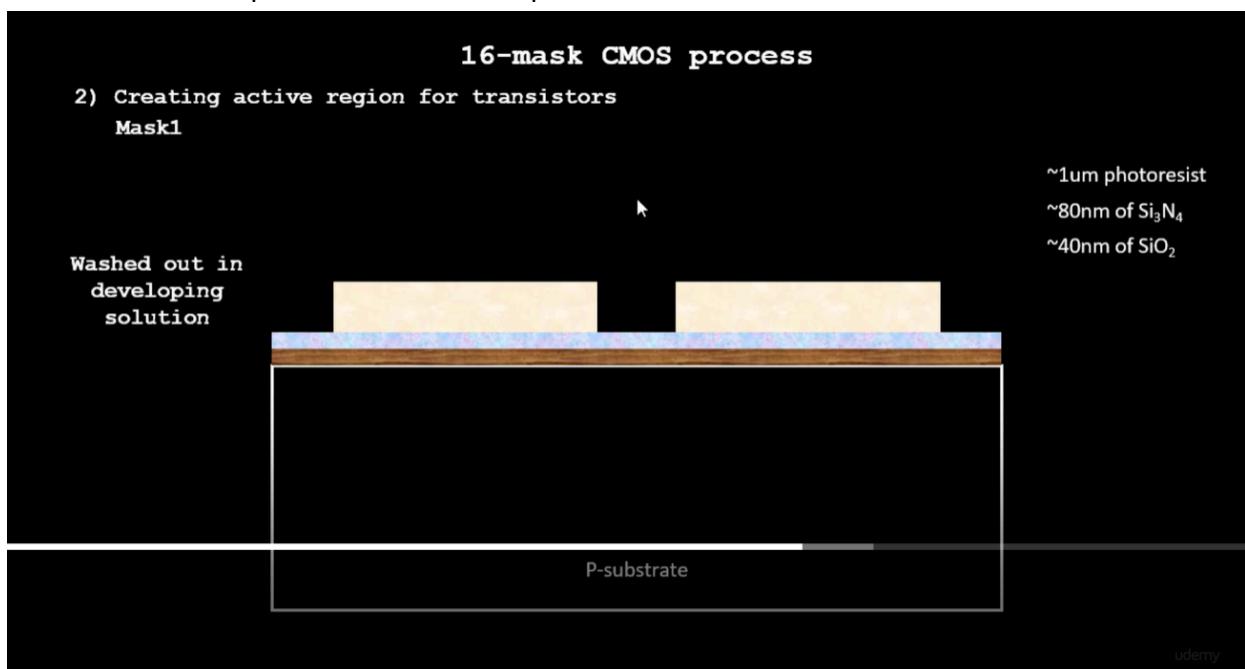
1) Selecting a substrate

P-type, high resistivity ($5\text{--}50$ ohms), doping level (10^{15} cm^{-3}), orientation (100)

Substrate doping should be less than 'well' doping. Coming in further sections



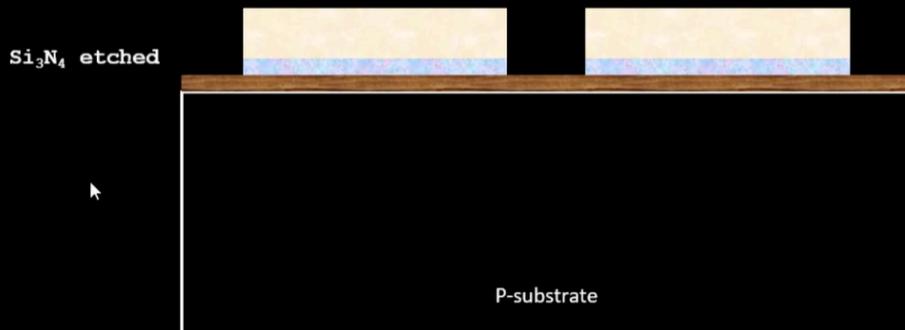
Areas beneath the photoresist mask are protected.



16-mask CMOS process

- 2) Creating active region for transistors
Mask1

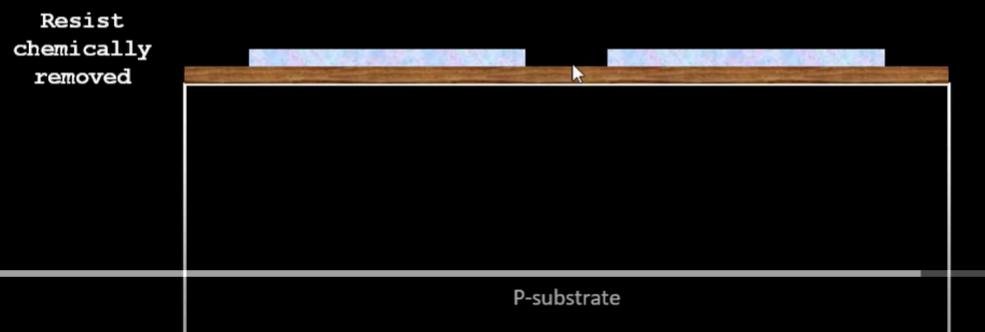
~1μm photoresist
~80nm of Si_3N_4
~40nm of SiO_2



16-mask CMOS process

- 2) Creating active region for transistors
Mask1

~1μm photoresist
~80nm of Si_3N_4
~40nm of SiO_2

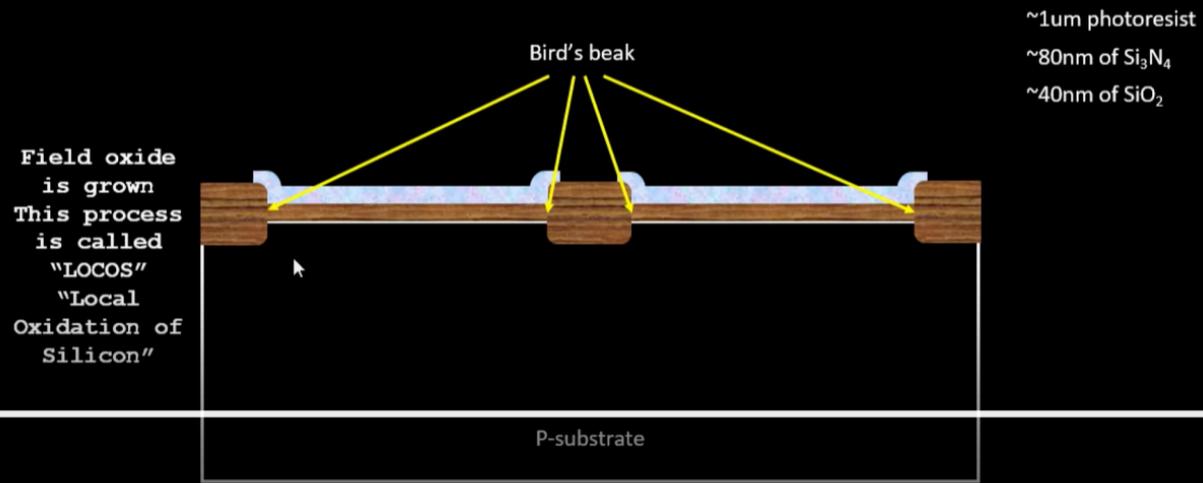


This is then placed in an oxidation furnace.

16-mask CMOS process

2) Creating active region for transistors

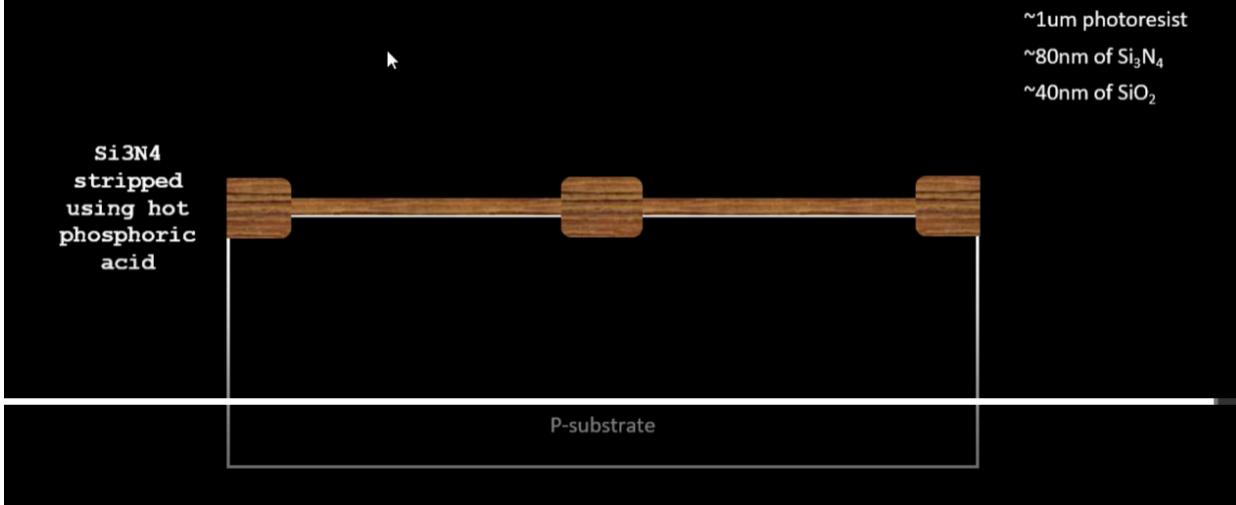
Mask1



16-mask CMOS process

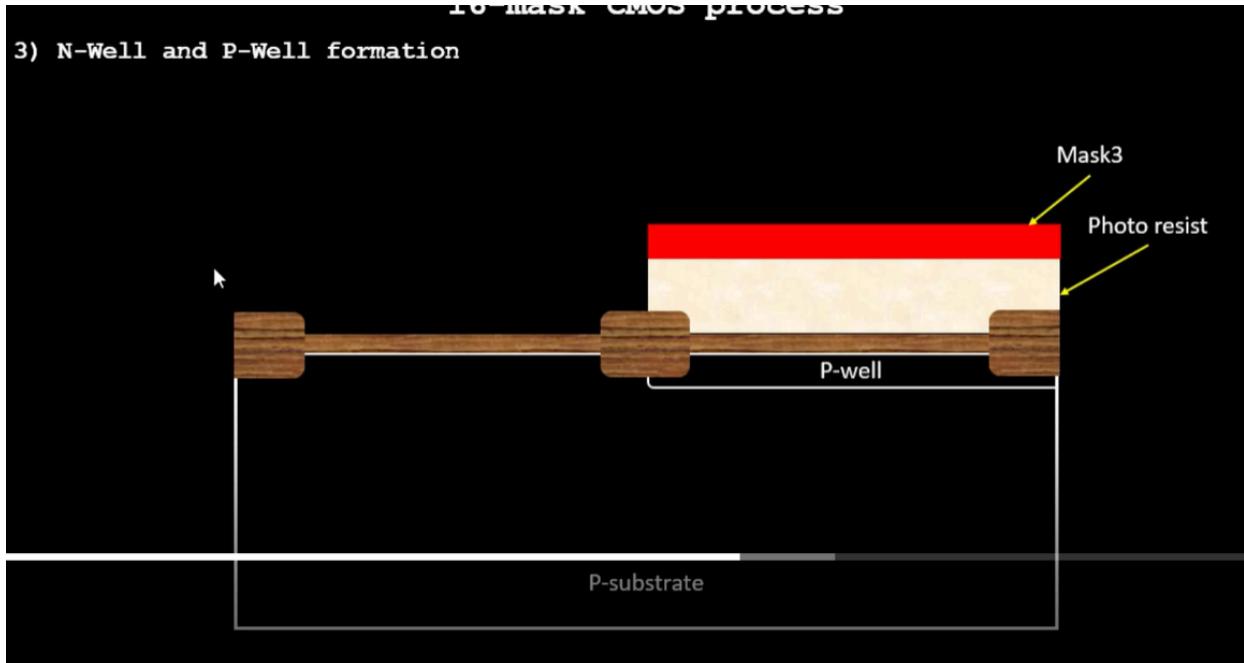
2) Creating active region for transistors

Mask1



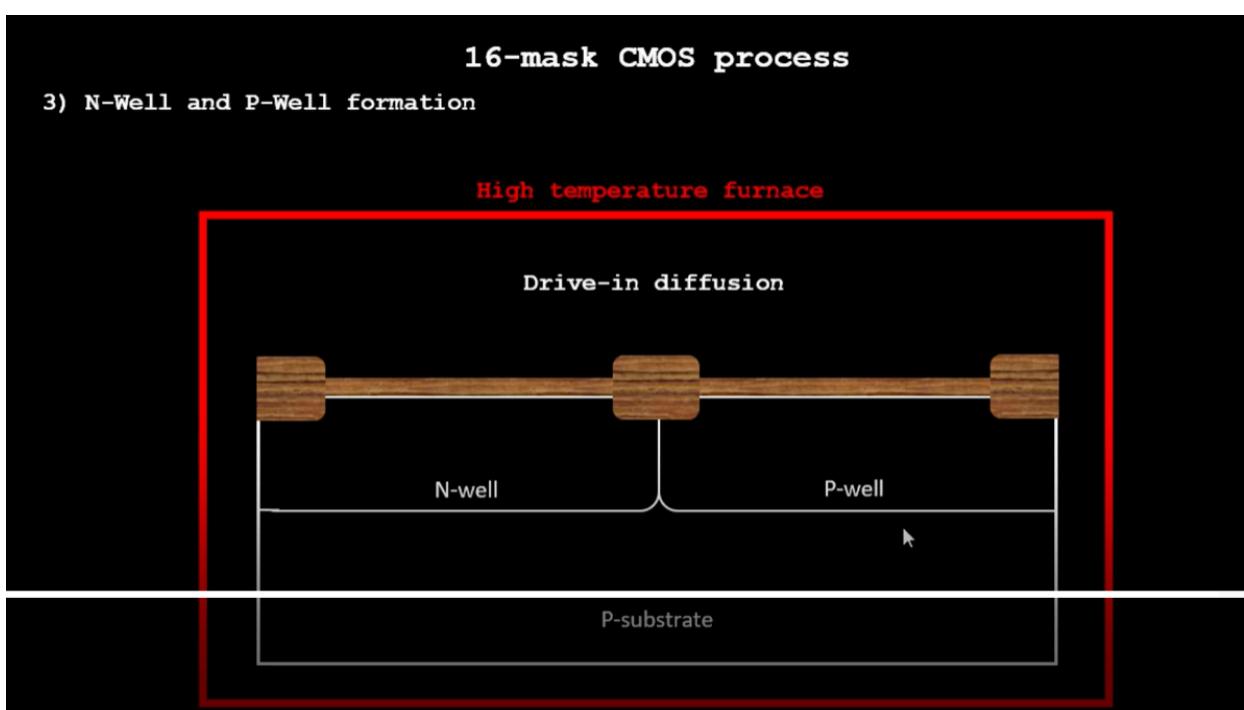
16-mask CMOS process

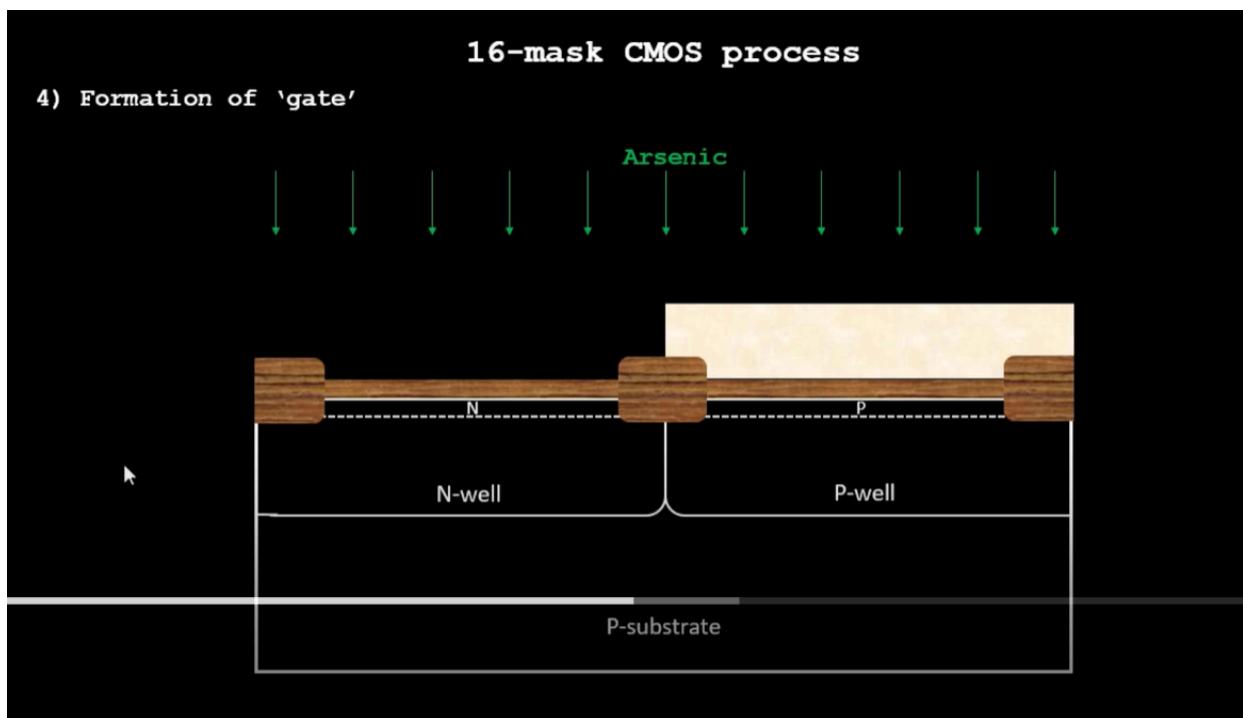
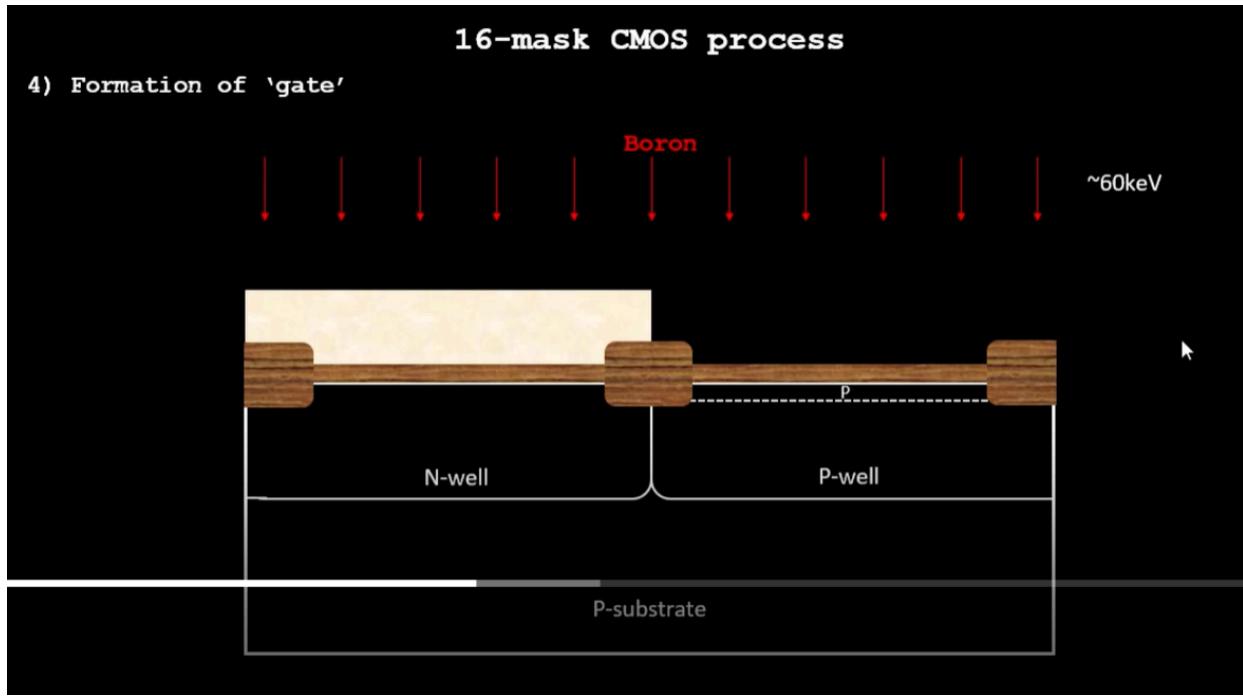
3) N-Well and P-Well formation



16-mask CMOS process

3) N-Well and P-Well formation



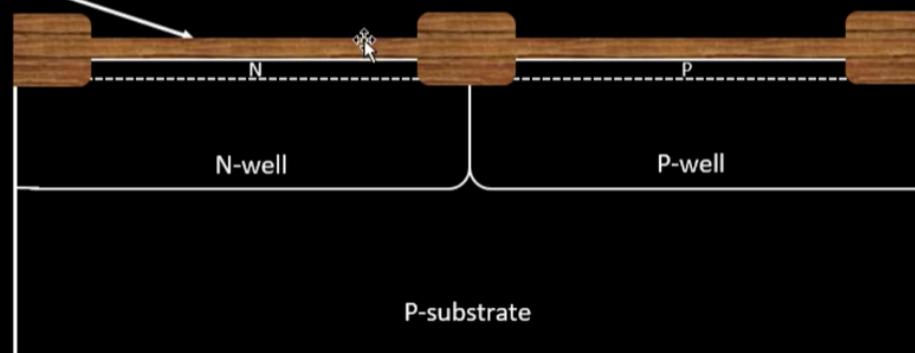


Lots of damage would have been done to the oxide layer due to implantations, we use hydrofluoric acid to remove the extra oxide and regrow new oxide of approx the same thickness

16-mask CMOS process

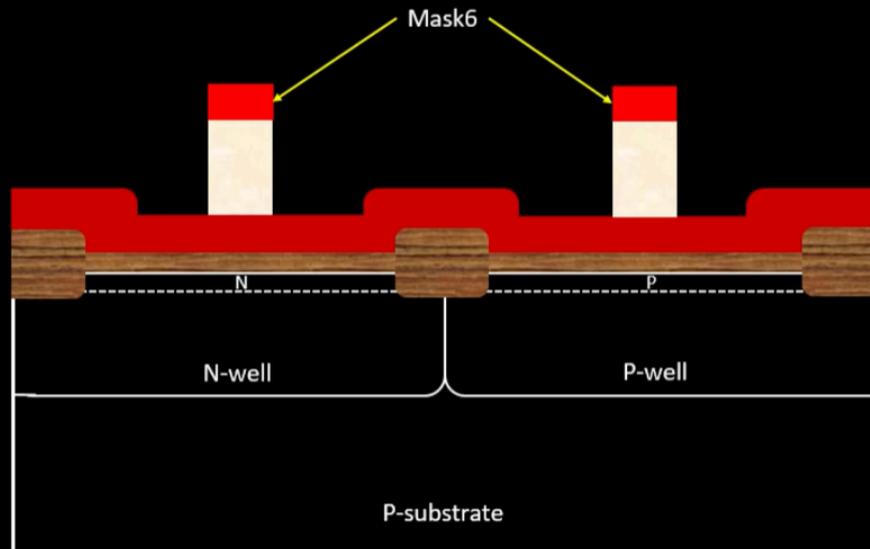
4) Formation of 'gate'

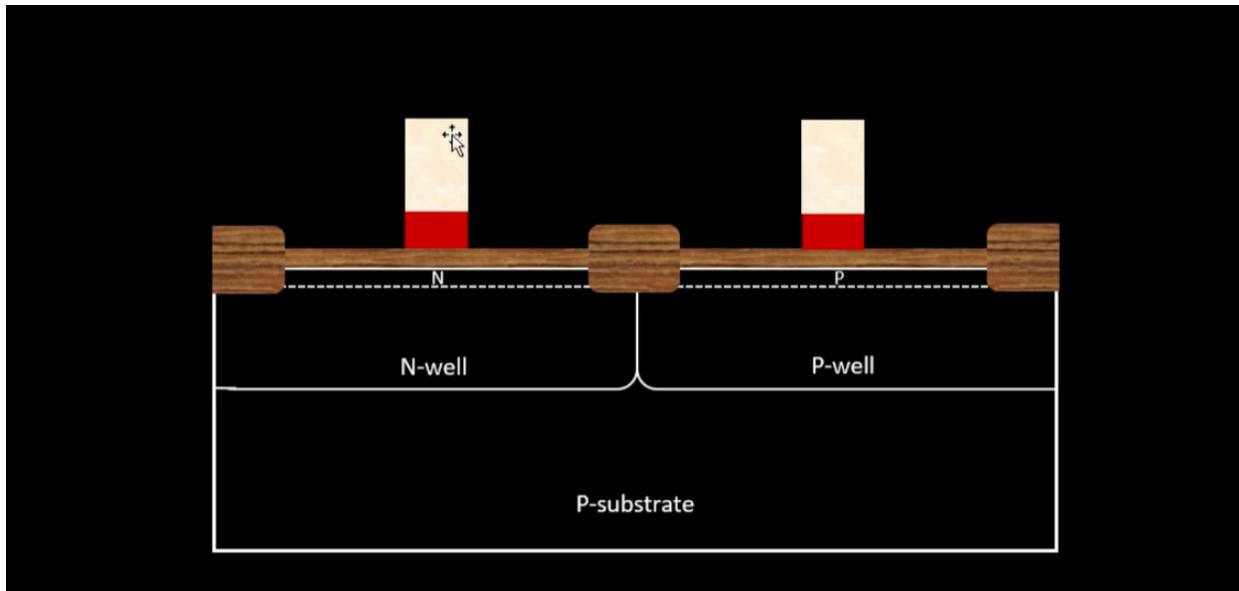
Original oxide etched/stripped using dilute hydrofluoric(HF) solution
Then re-grown again to give high quality oxide (~10nm thin)



16-mask CMOS process

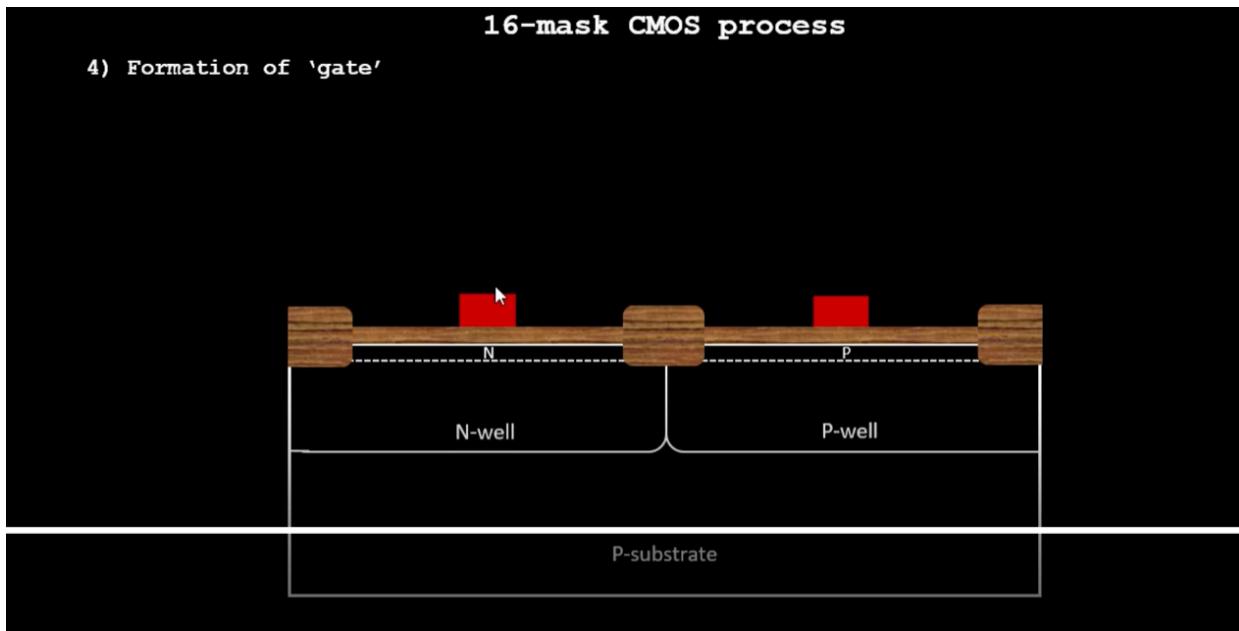
4) Formation of 'gate'

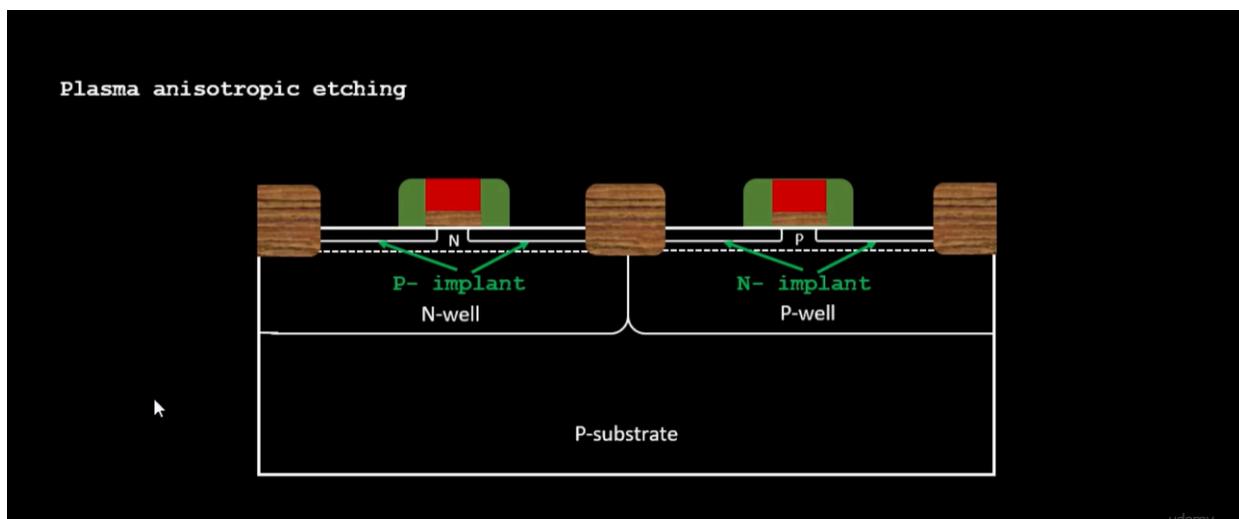
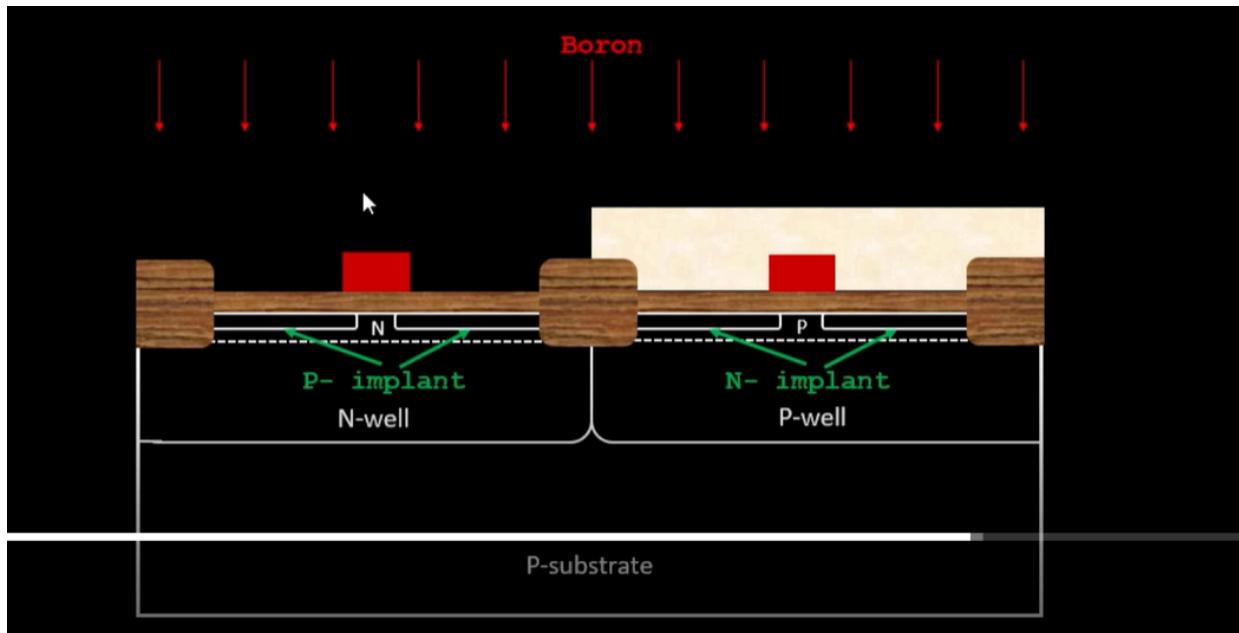




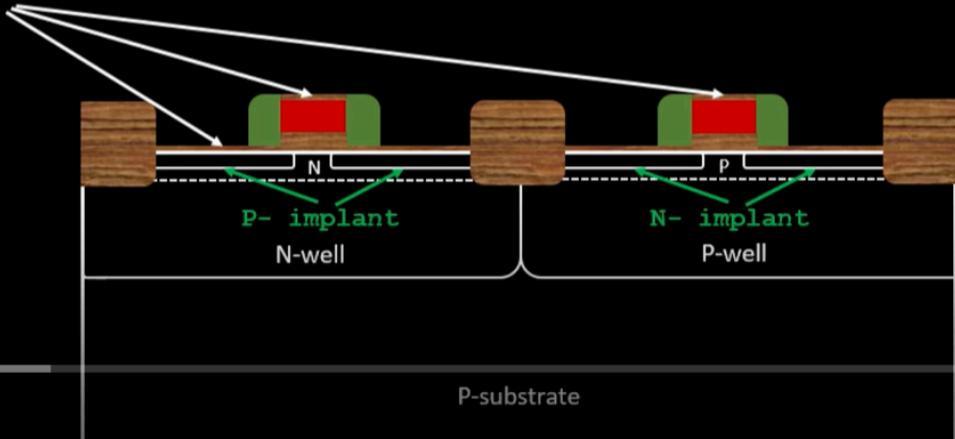
16-mask CMOS process

4) Formation of 'gate'

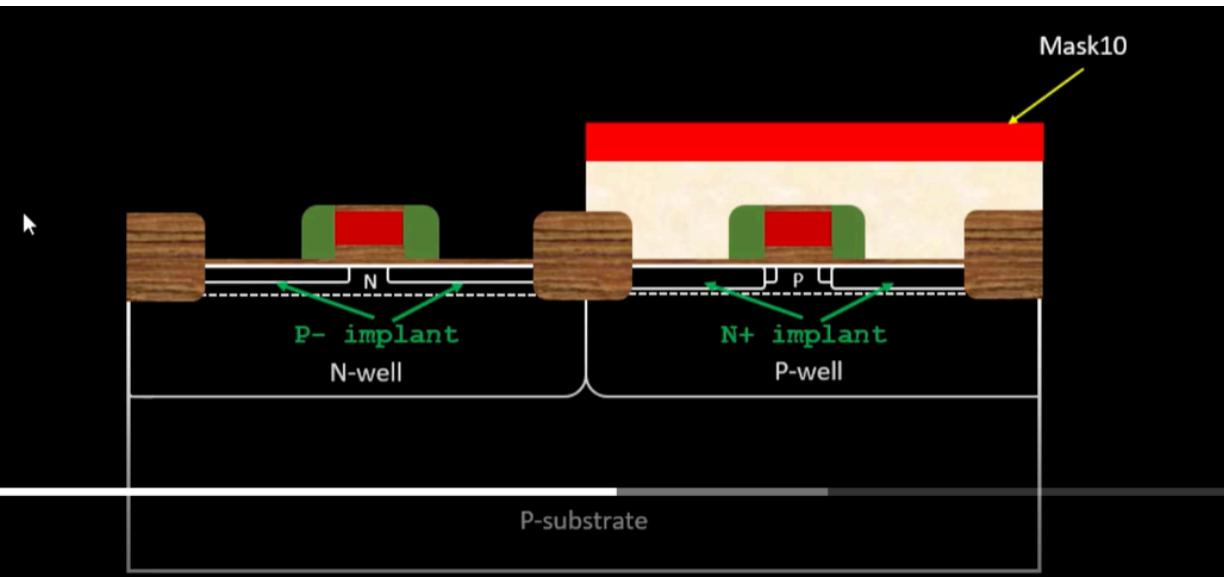




**Thin screen oxide to avoid
channeling during implants**

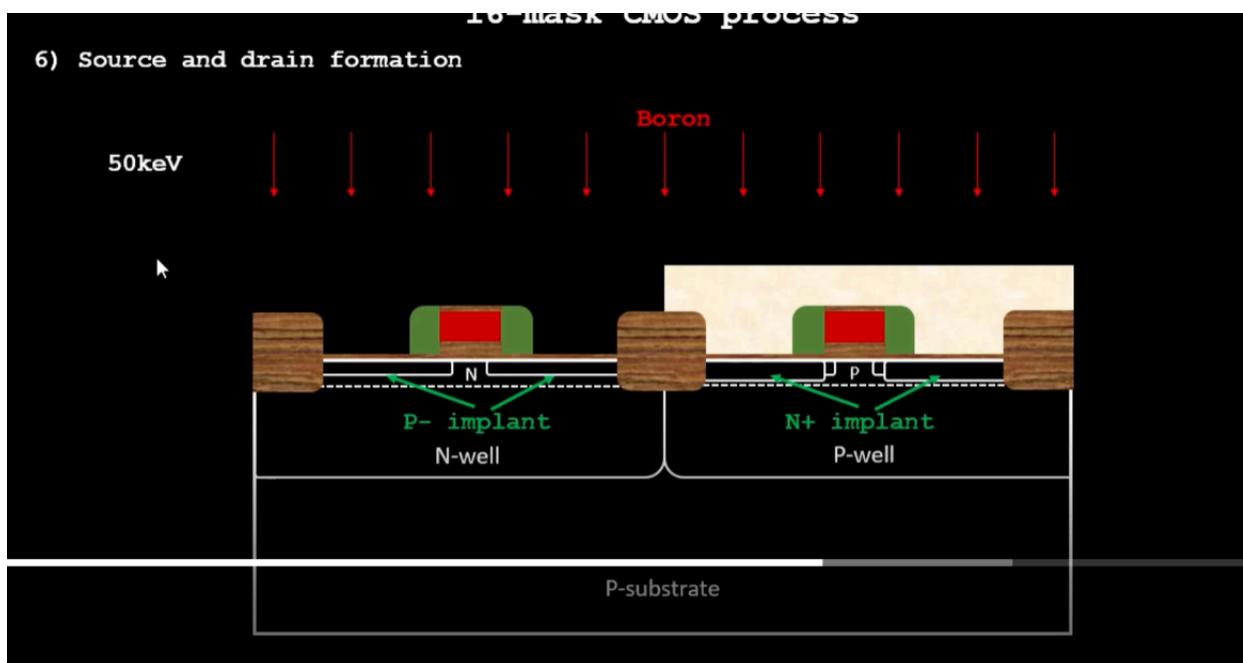


Mask10

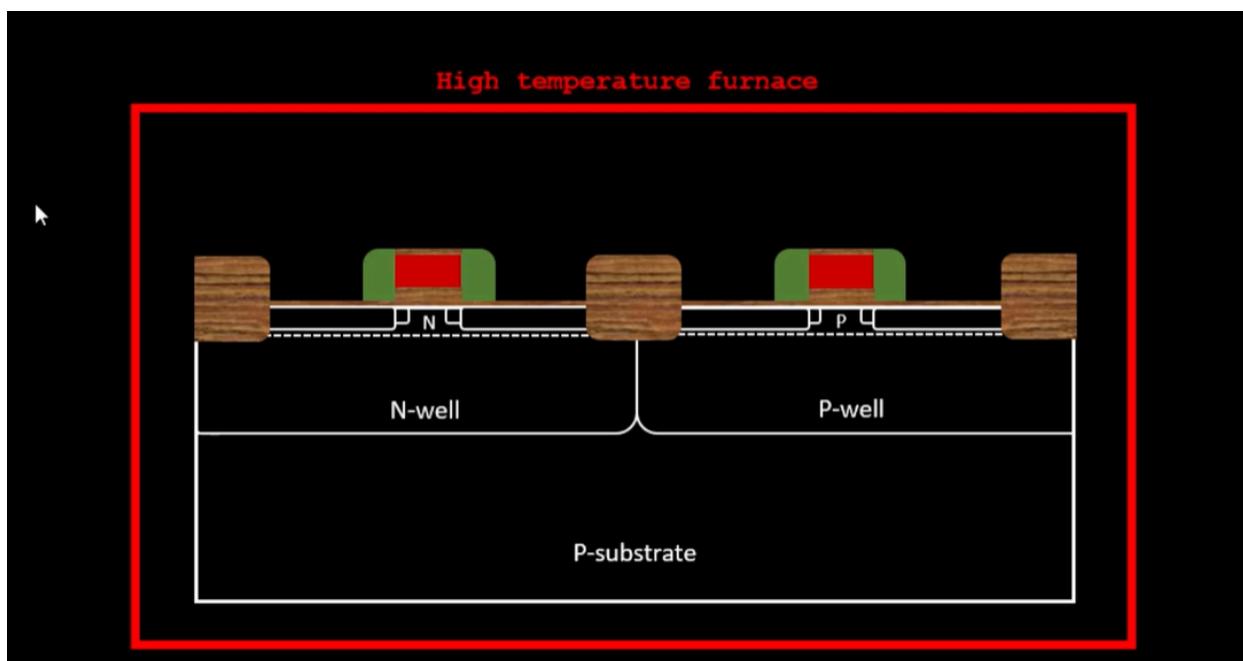


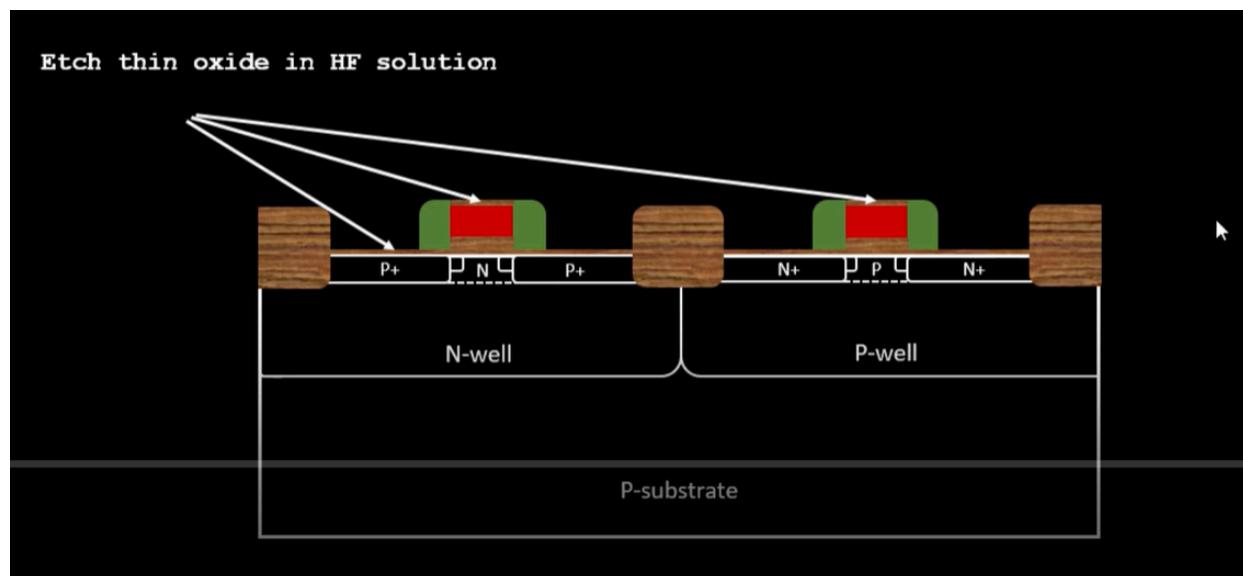
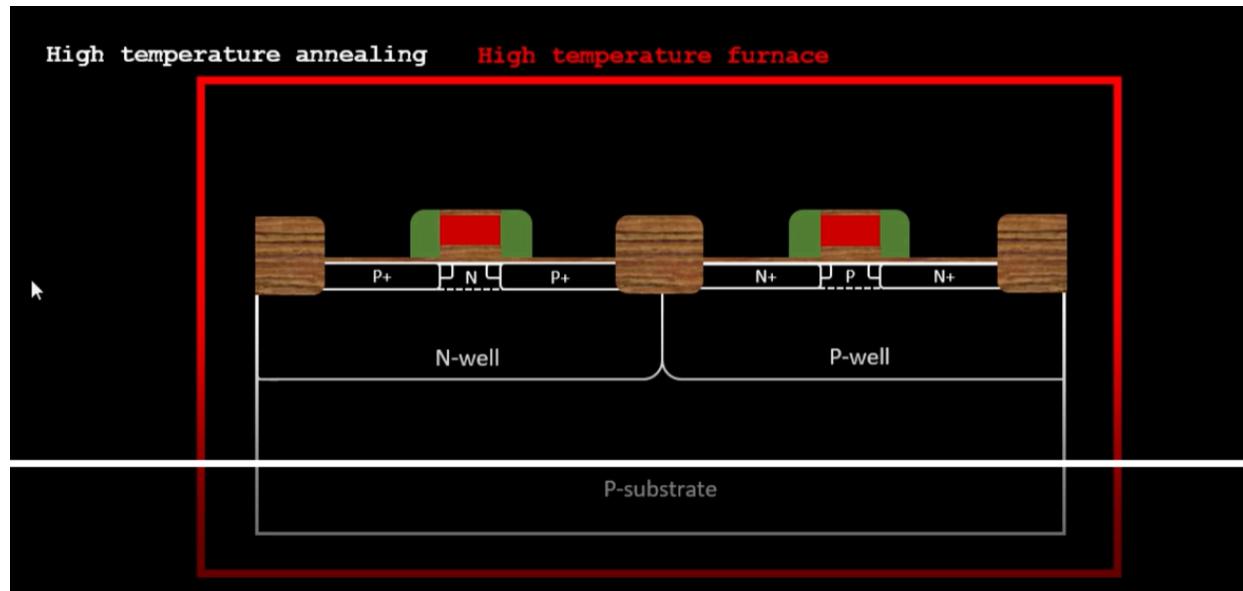
16-mask CMOS process

6) Source and drain formation



High temperature furnace

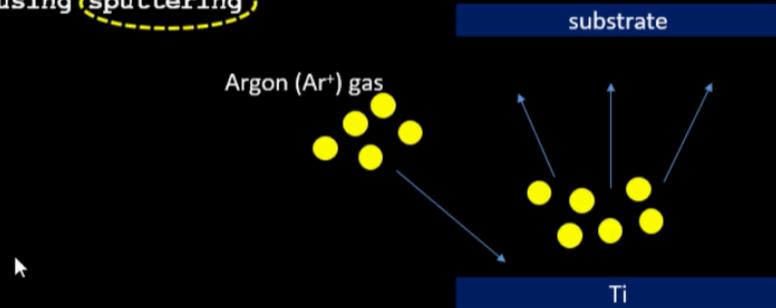




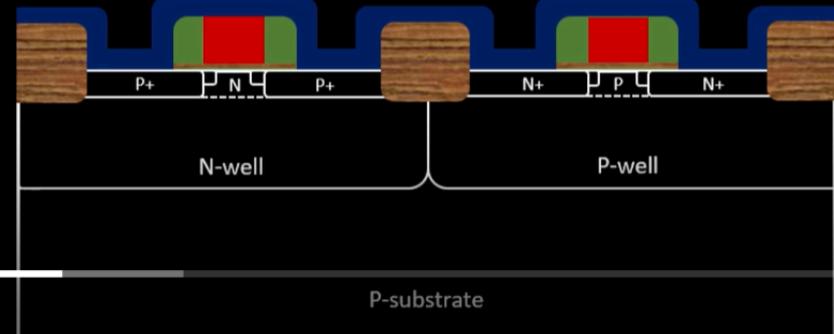
Remove the thin oxides created to avoid short channel effects

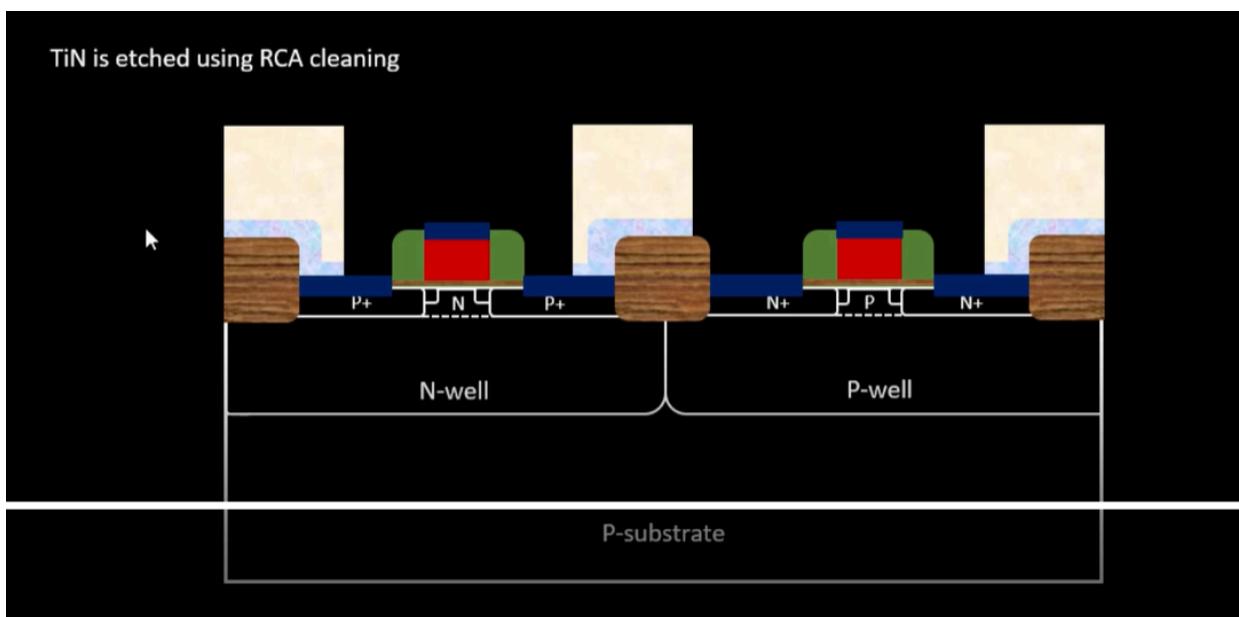
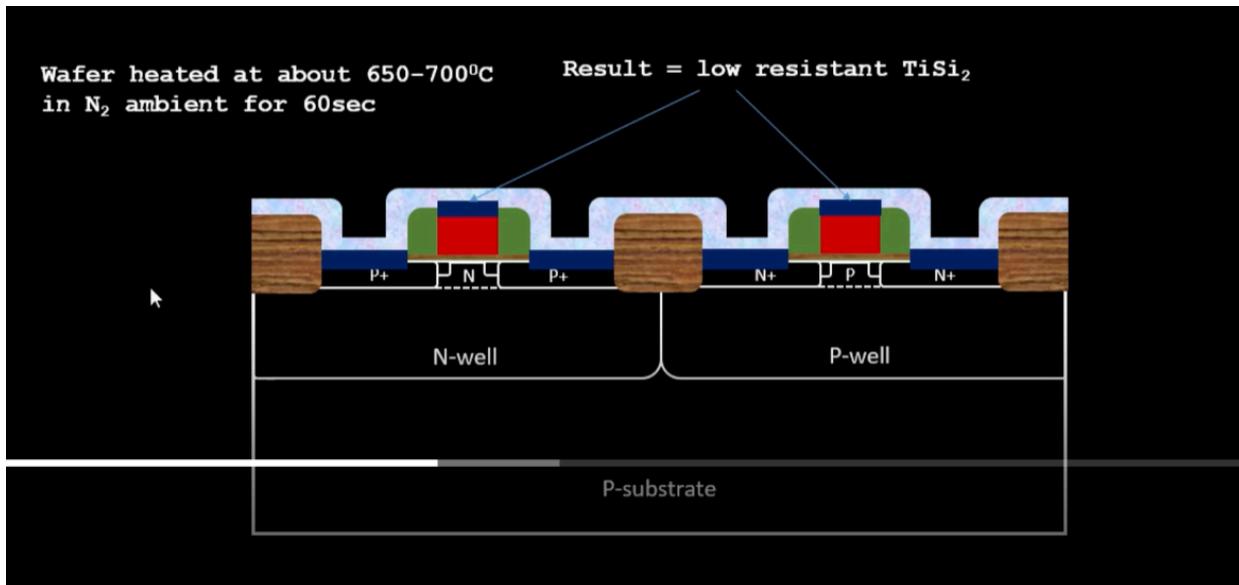
7) Steps to form contacts and interconnects (local)

deposit titanium on wafer surface, using sputtering



deposit titanium on wafer surface, using sputtering

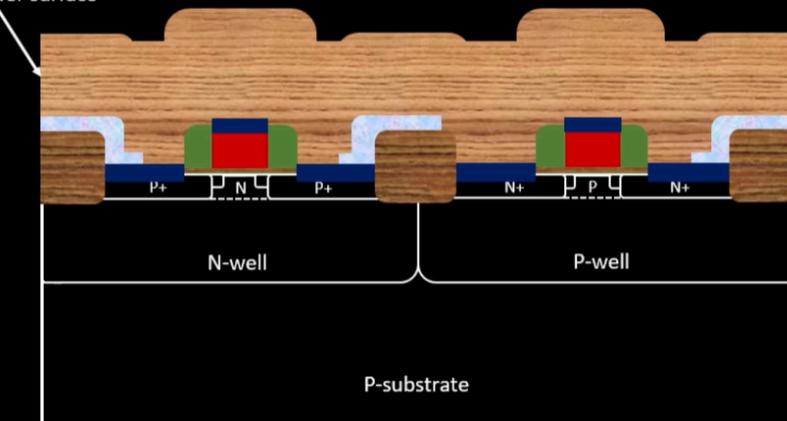




18 mask CMOS process

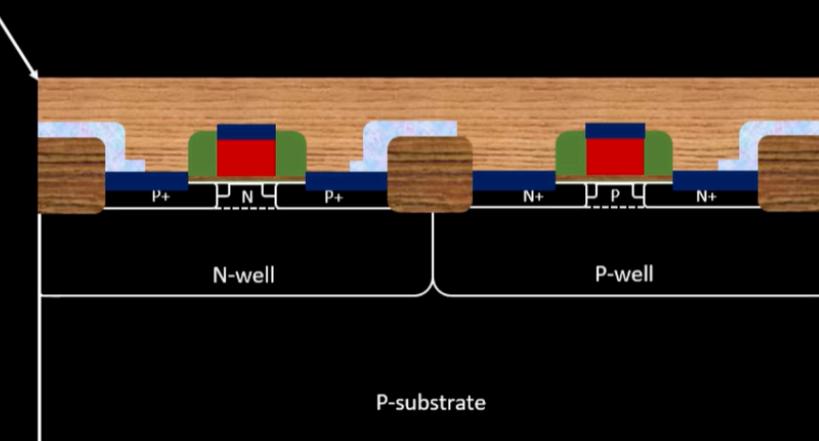
8) Higher level metal formation

1um of SiO_2 doped with phosphorous or boron (known as phosphosilicate glass or borophosphosilicate glass) deposited on wafer surface



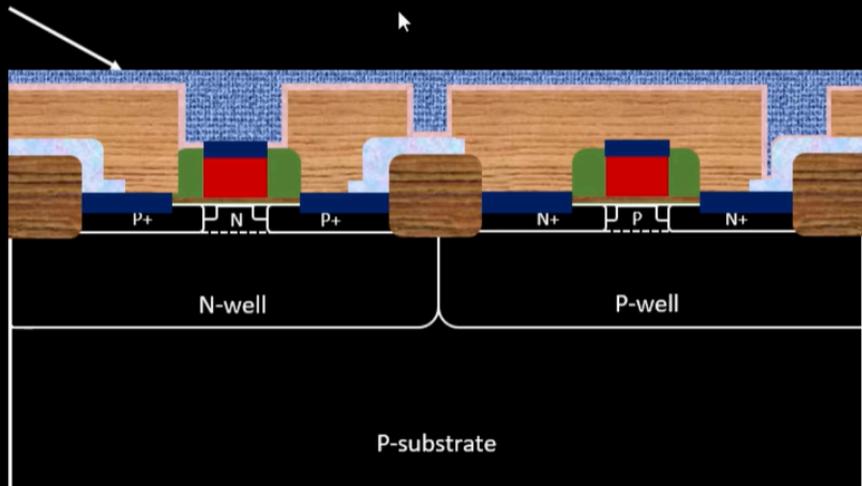
udemy

Chemical mechanical polishing (CMP) technique for planarizing wafer surface

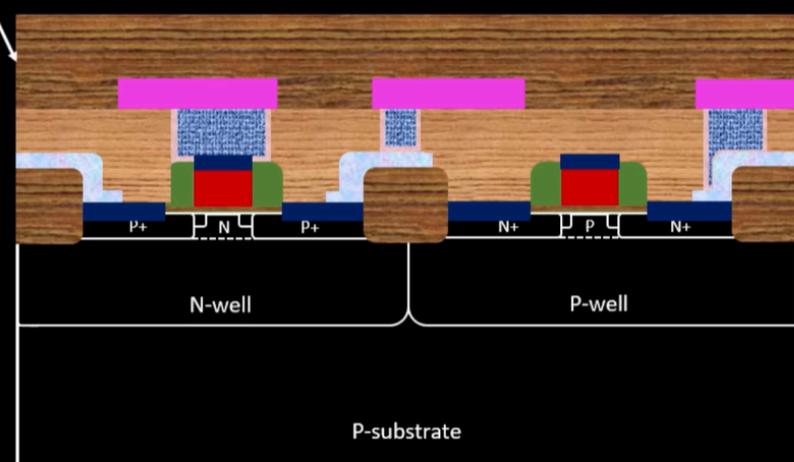


8) Higher level metal formation

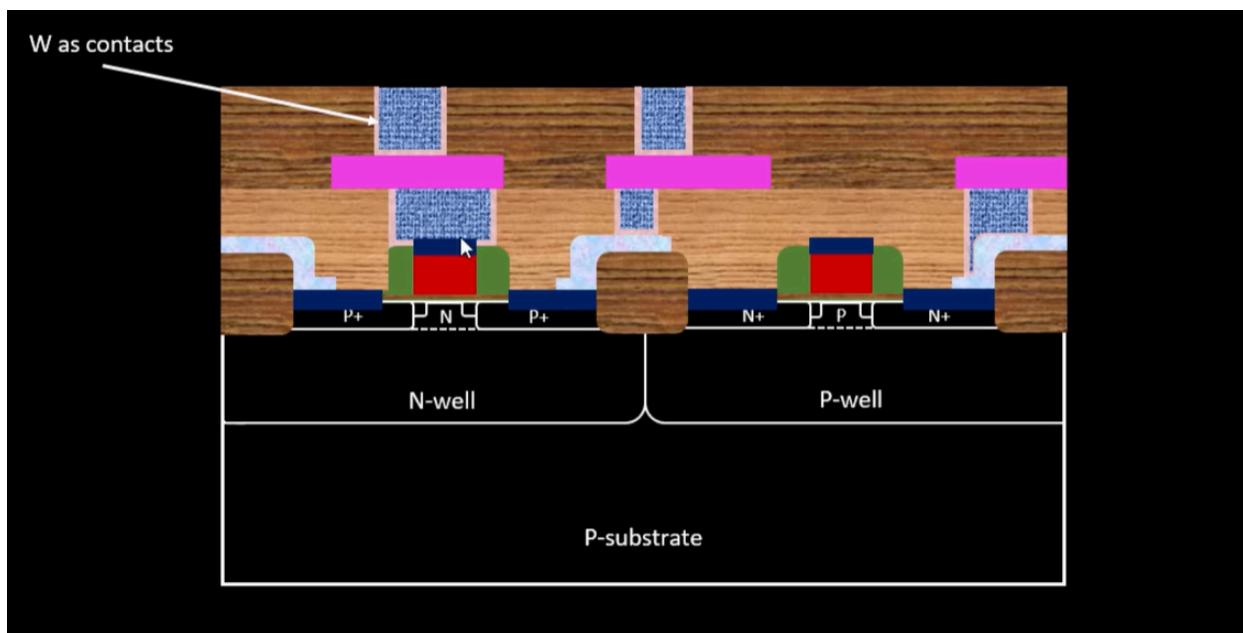
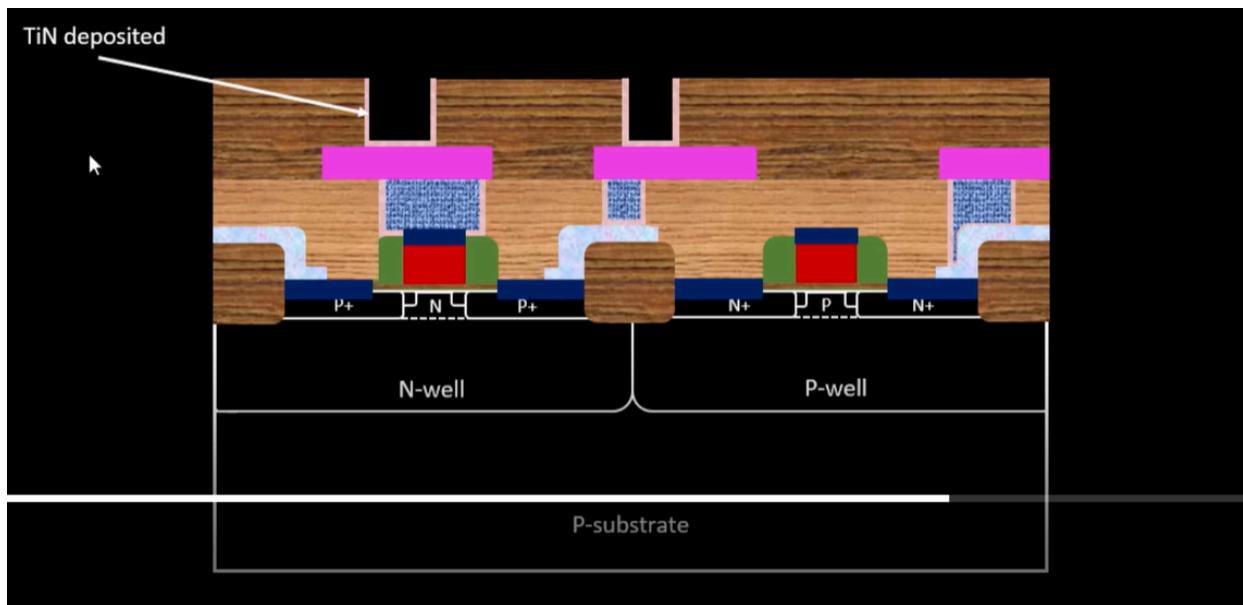
Blanket tungsten (W) layer deposition

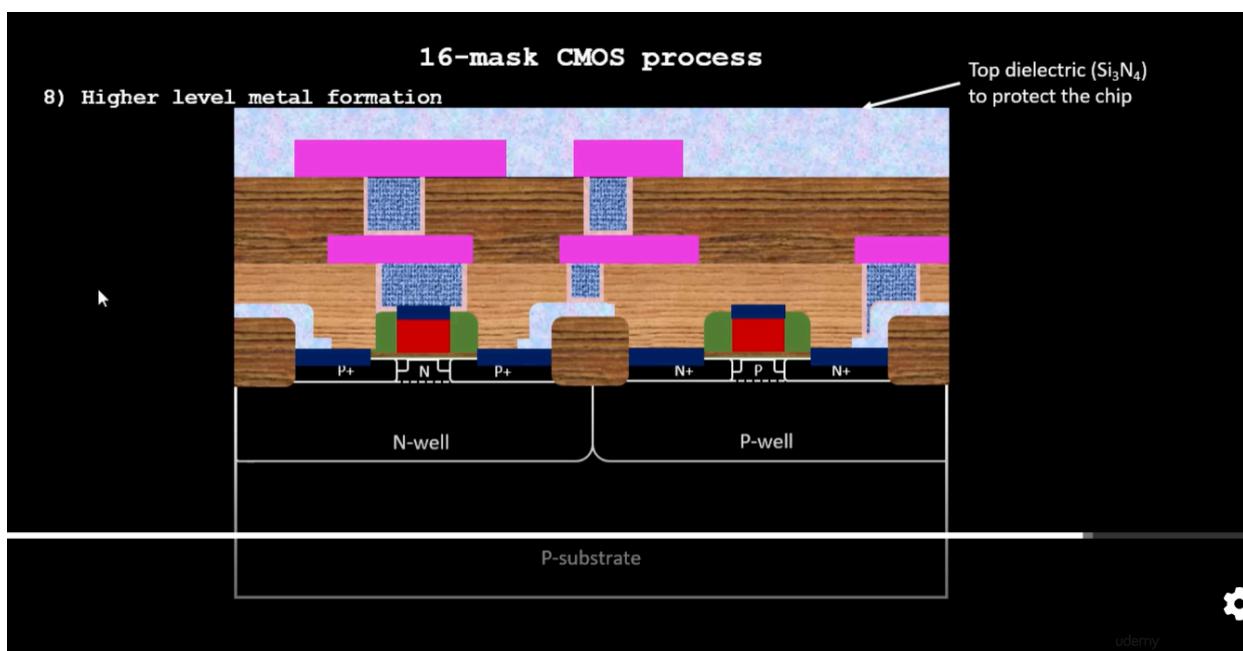
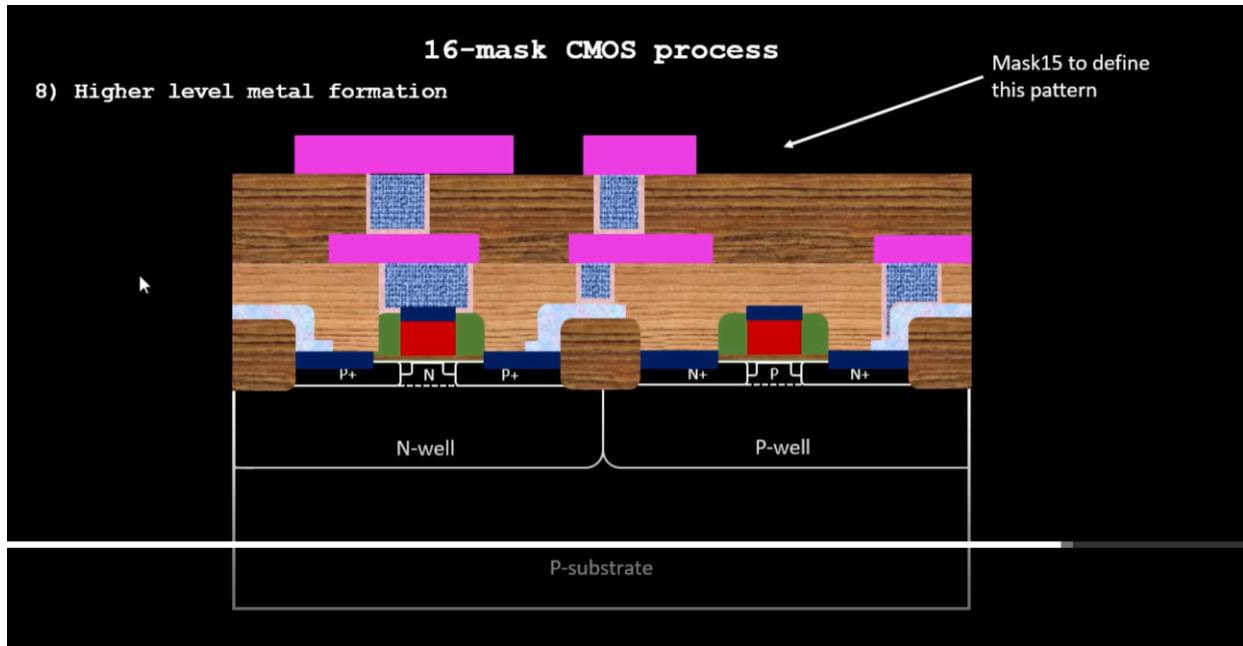


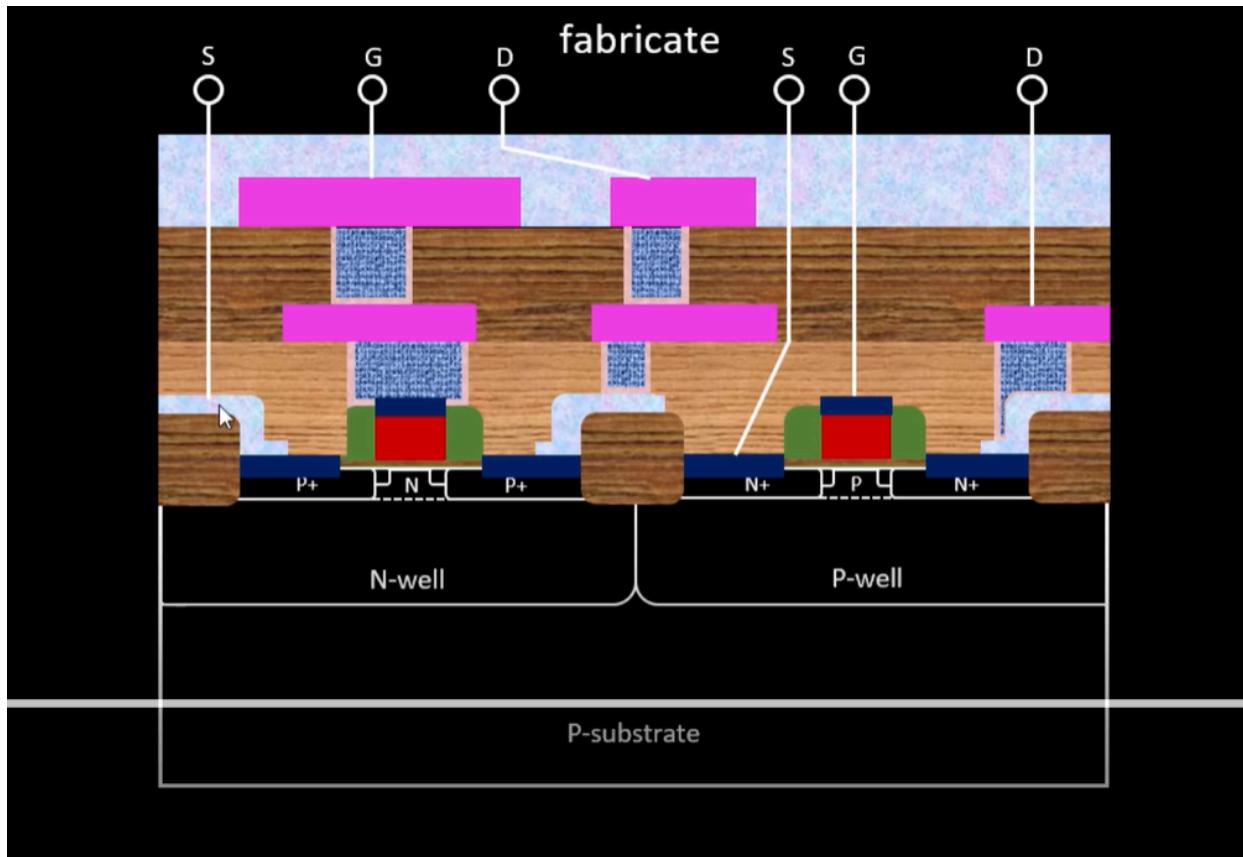
SiO₂ deposited and CMP done



Mask 13 was used to etch the aluminium contacts



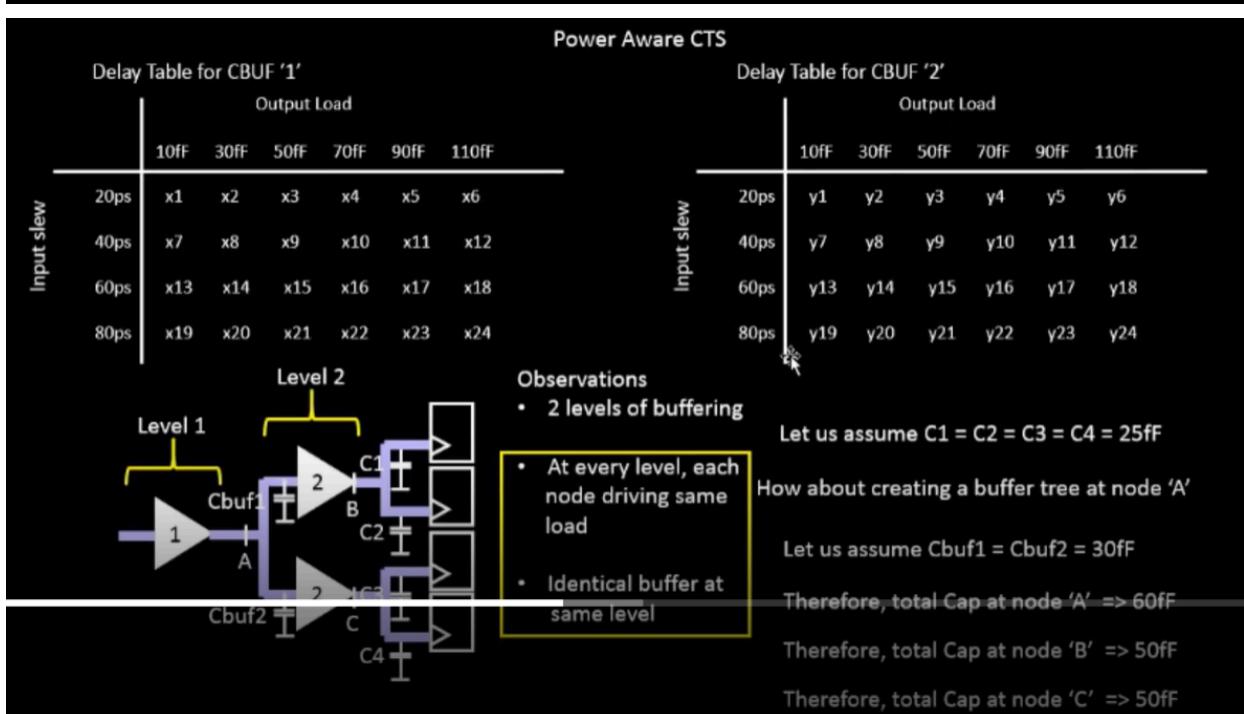
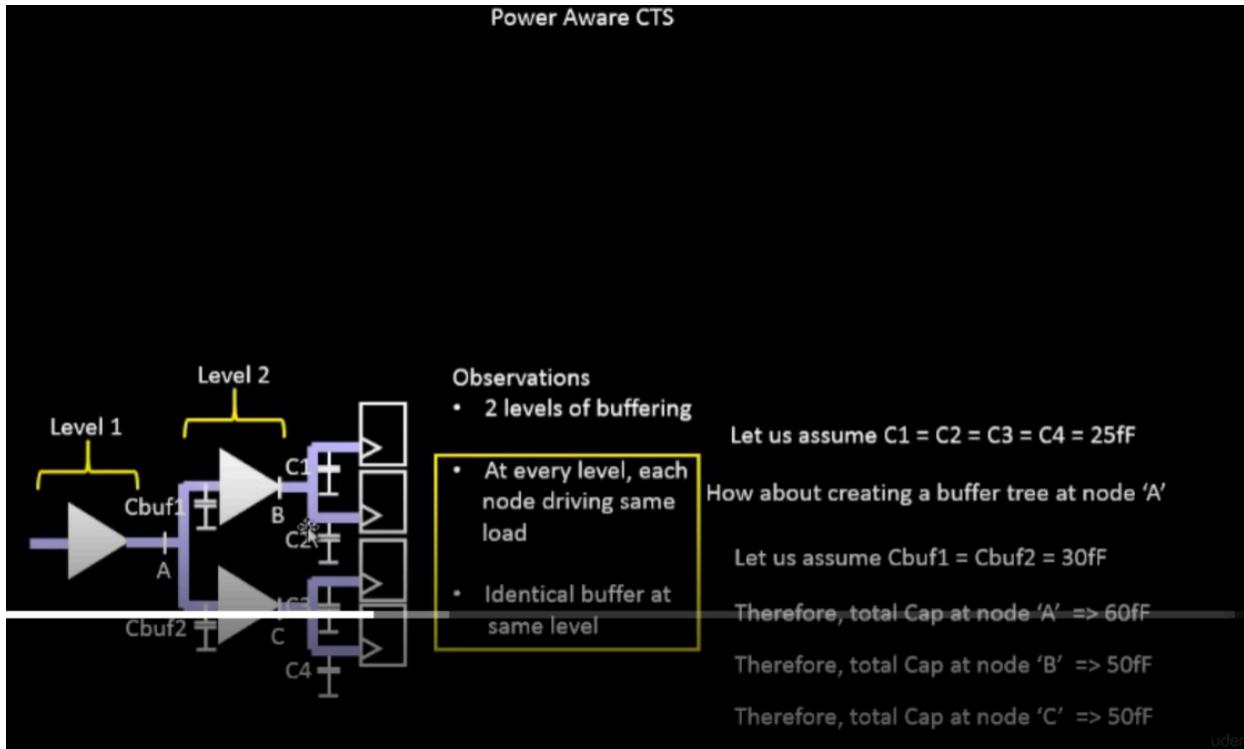




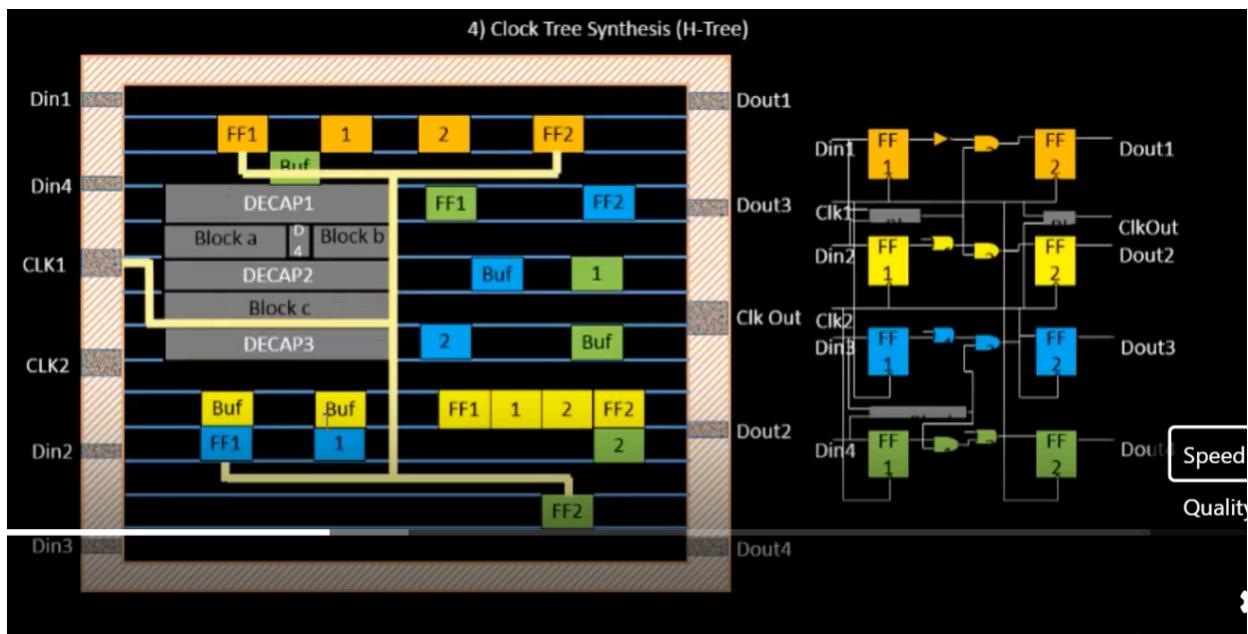
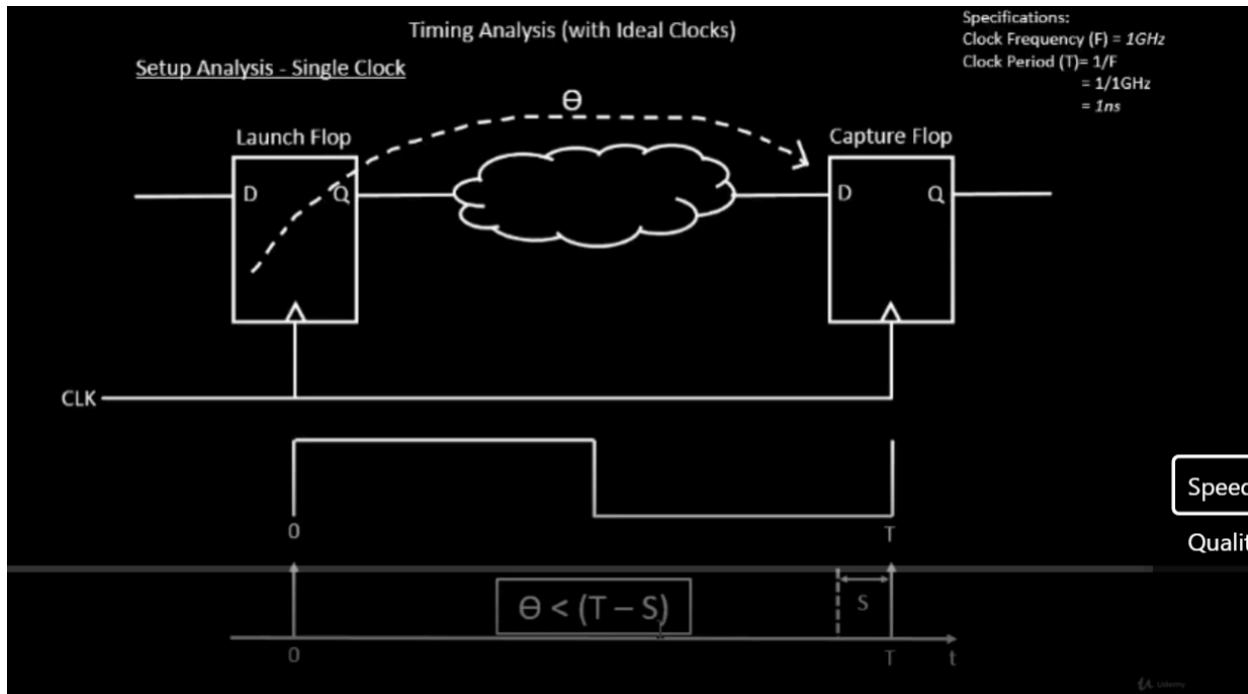
Mask 16 used to create the contact holes as above

Tab 2

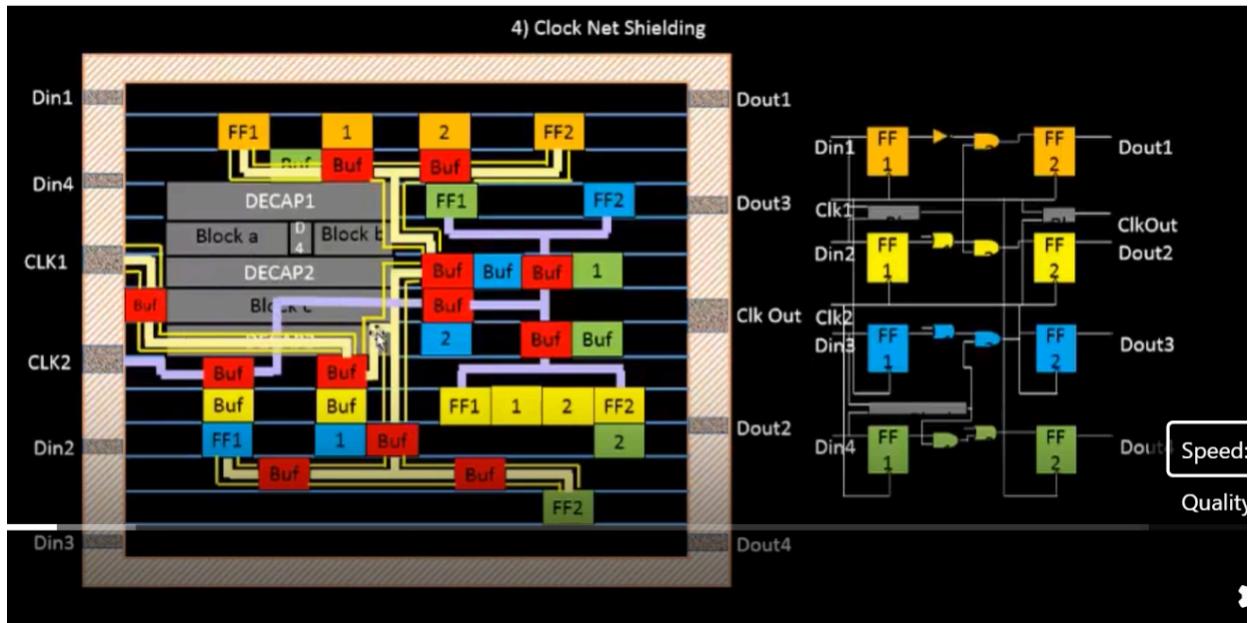
Pre layout timing analysis and importance of a good clock tree:



Delay table varies based on RC time constant while R varies according to device sizing

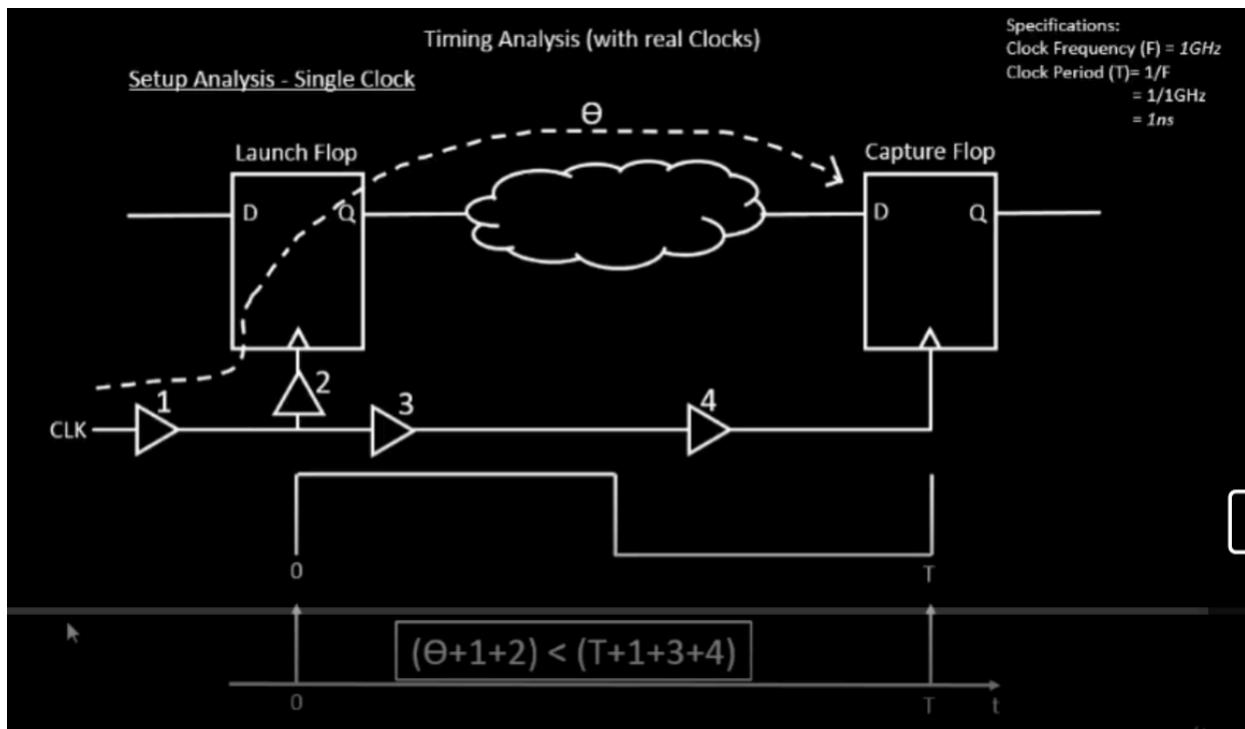


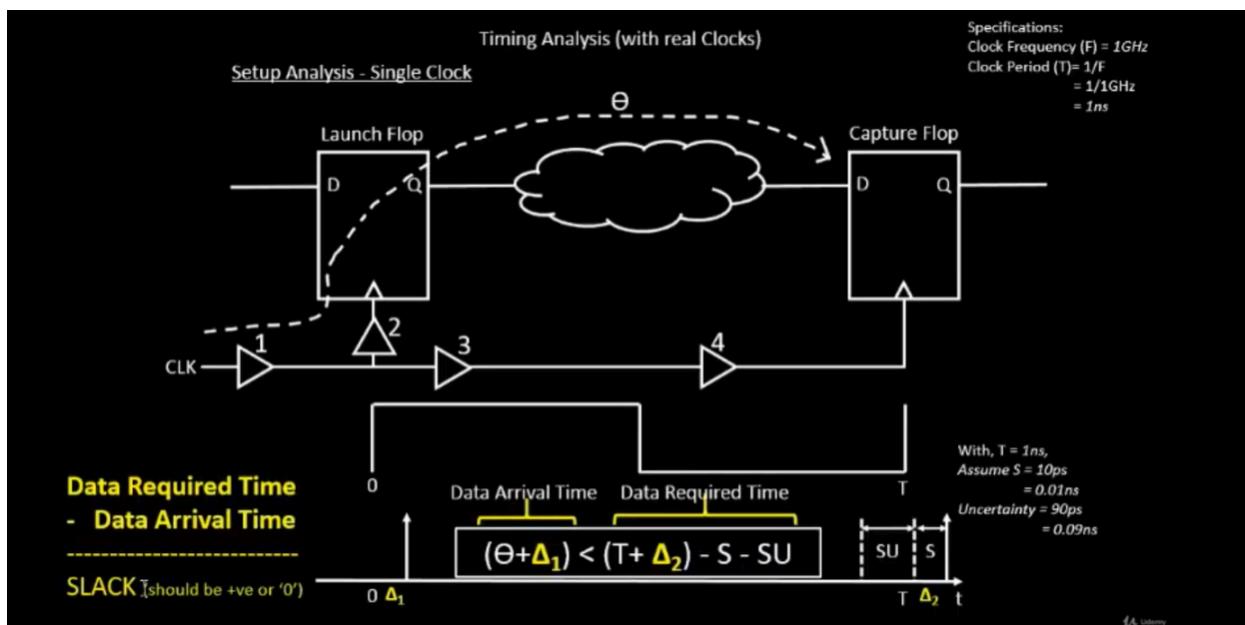
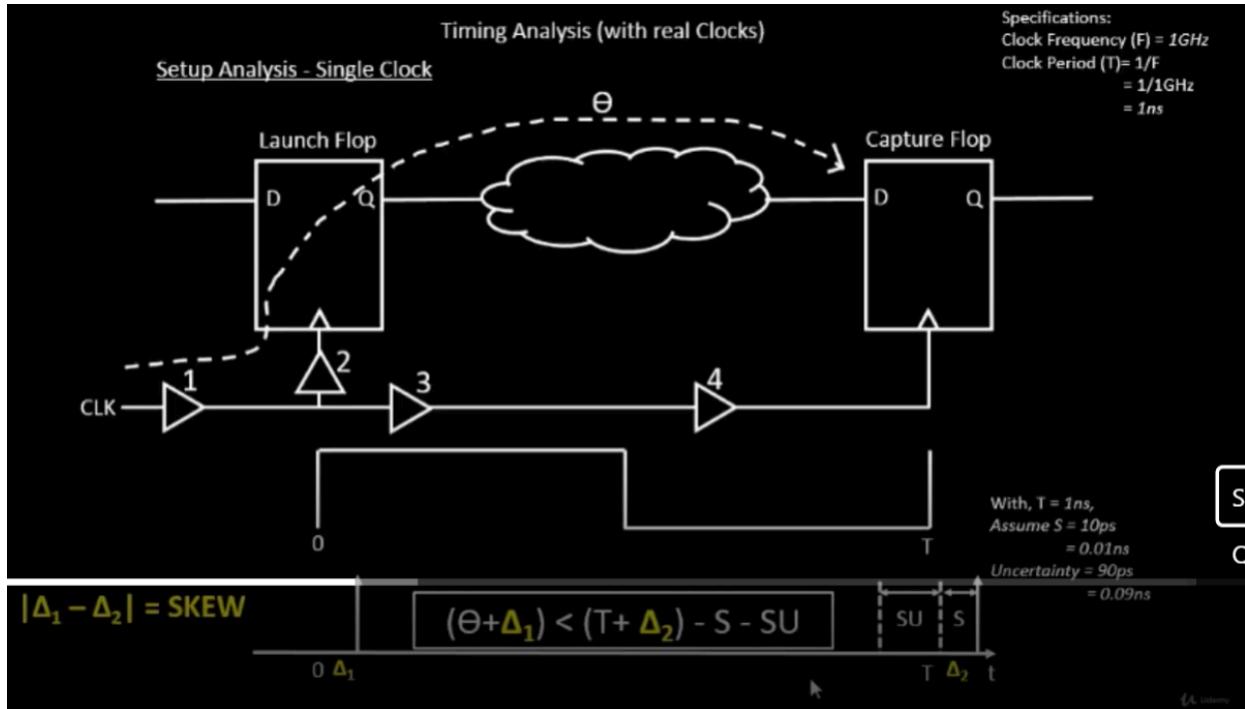
Midpoint strategy for clock tree synthesis for time taken to reach the flop be same for all pths



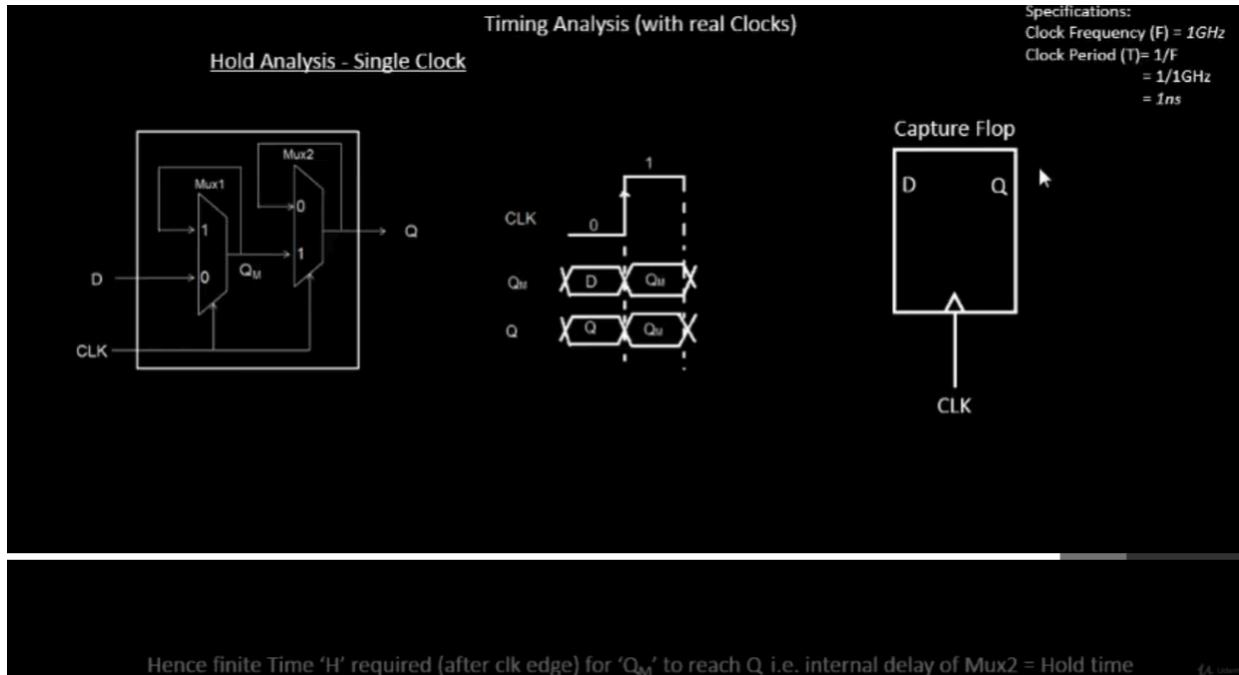
Clock net shielding to avoid crosstalks

Setup and hold time analysis using OPENSTA:

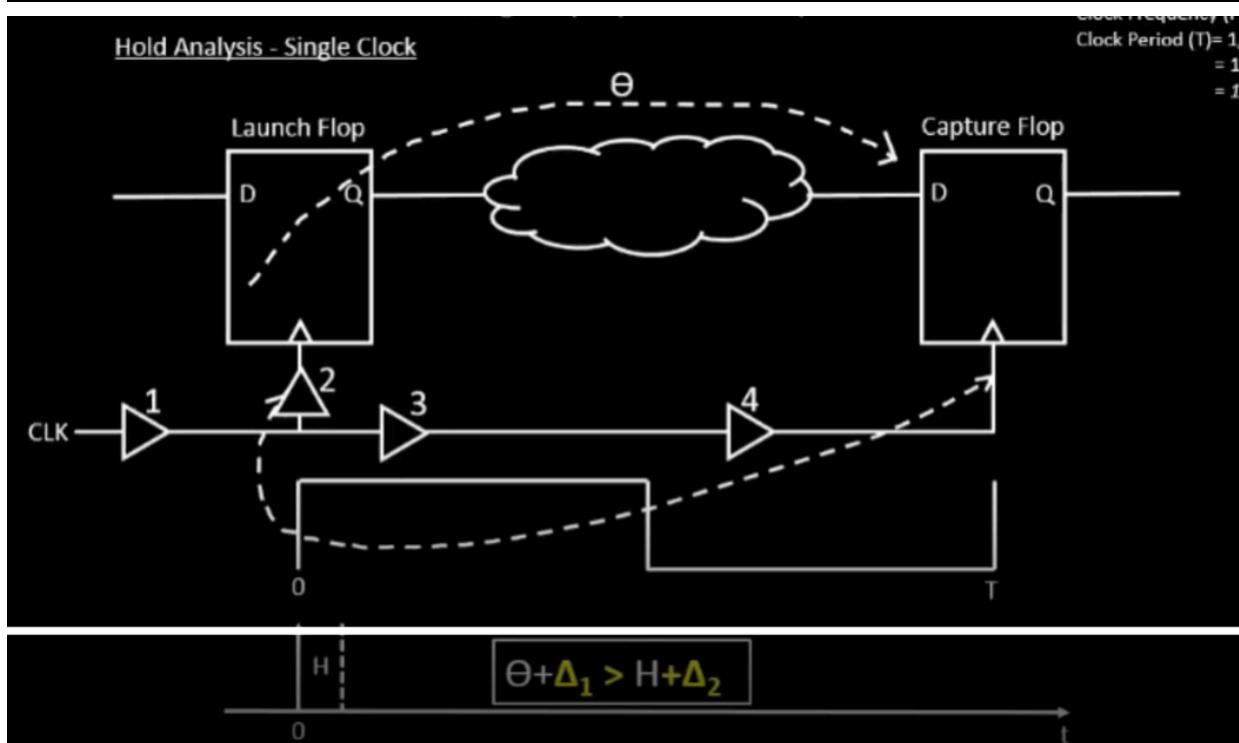


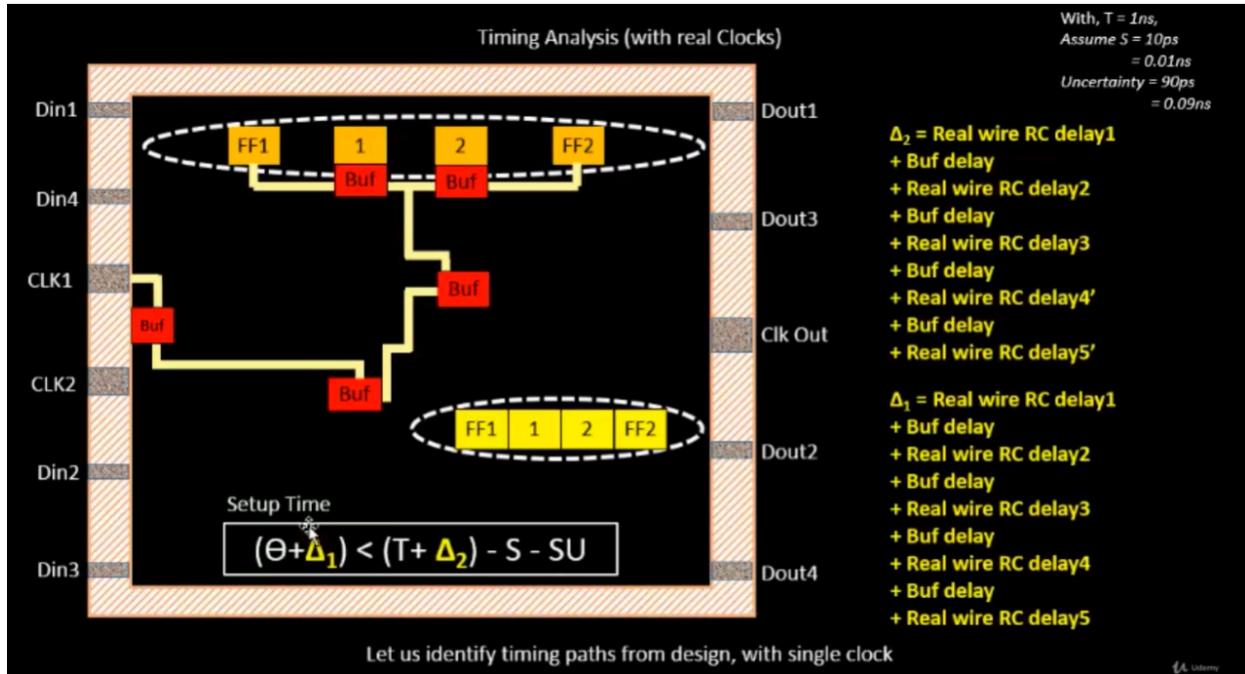


Negative slack - setup violation



Hence finite Time 'H' required (after clk edge) for 'Q_{tt}' to reach Q i.e. internal delay of Mux2 = Hold time





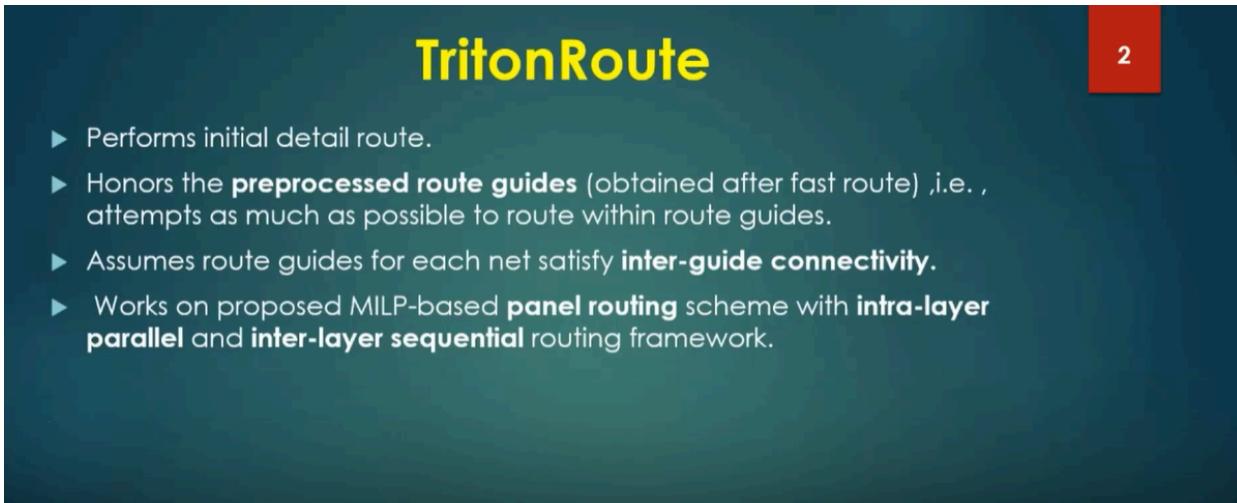
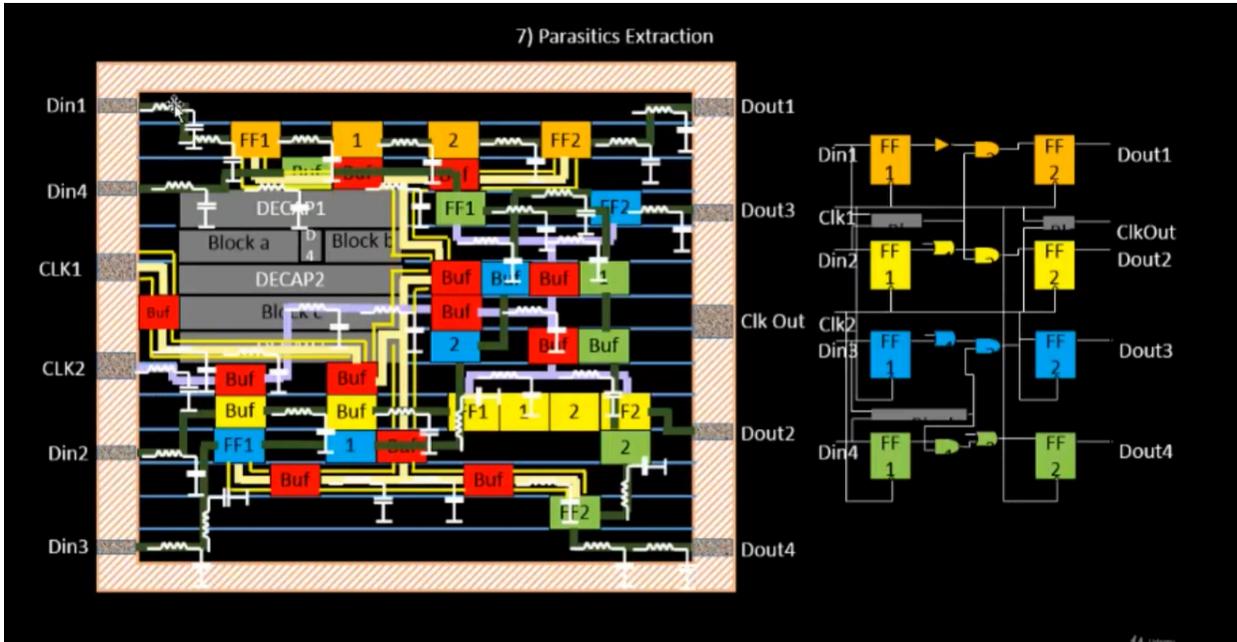
ROUTING



Any routes with single bends are more preferred.

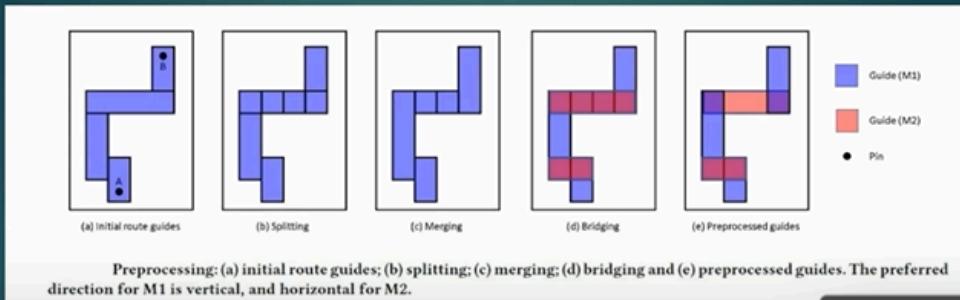
DRC CHECK

Wire width, Wire pitch, wire spacing, signal short



Preprocessed route guides

3



Preprocessing: (a) initial route guides; (b) splitting; (c) merging; (d) bridging and (e) preprocessed guides. The preferred direction for M1 is vertical, and horizontal for M2.

REQUIREMENTS OF PREPROCESSED GUIDES:

- Should have unit width.
- Should be in the preferred direction.

Speed: 2x

Quality: auto

04:04 / 11:34



reH

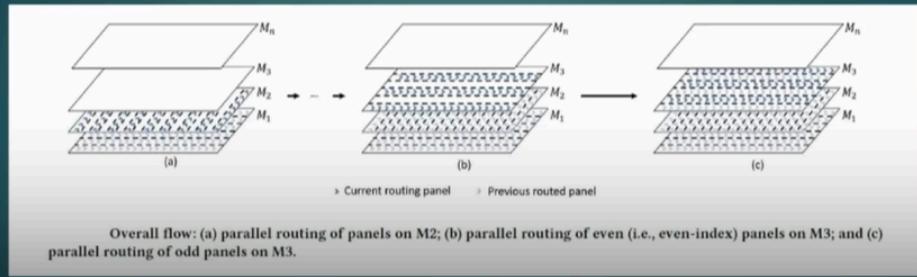
MILP based routing technique

Inter-guide connectivity

4

- ▶ Two guides are connected if:
 - ▶ they are on the same metal layer with touching edges, or
 - ▶ they are on neighboring metal layers with a nonzero vertically overlapped area.
- ▶ Each unconnected terminal (i.e., pin of a standard-cell instance) should have its pin shape overlapped by a route guide.

Intra-layer parallel & Inter-layer sequential panel routing



- Access point and Access point cluster
- Optimization of routing topology- minimum spanning tree

Tab 3

