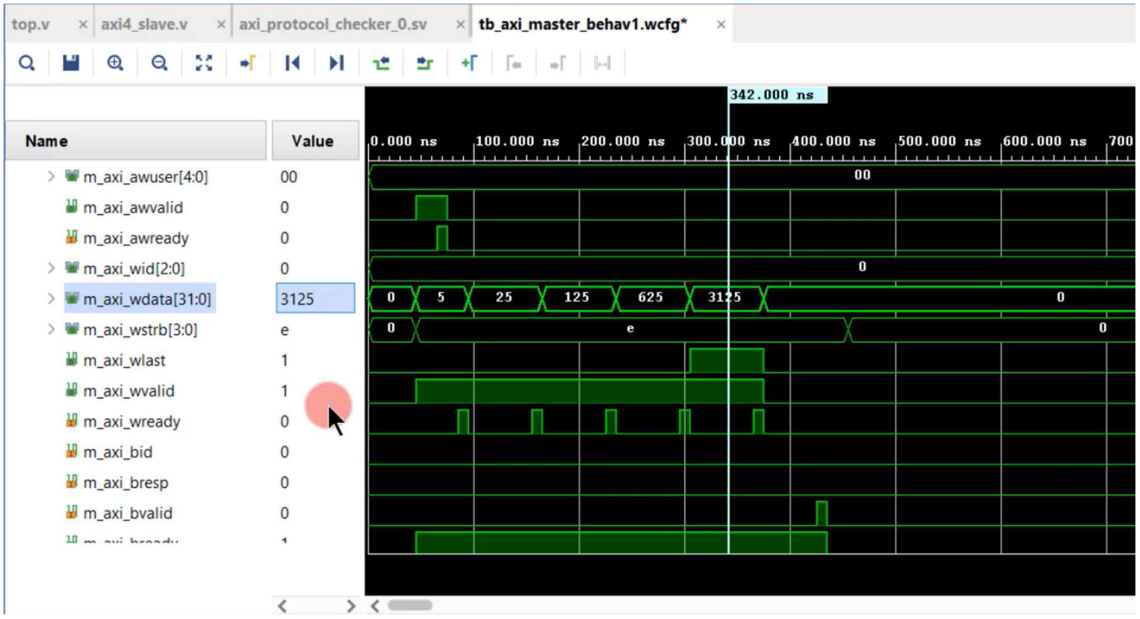
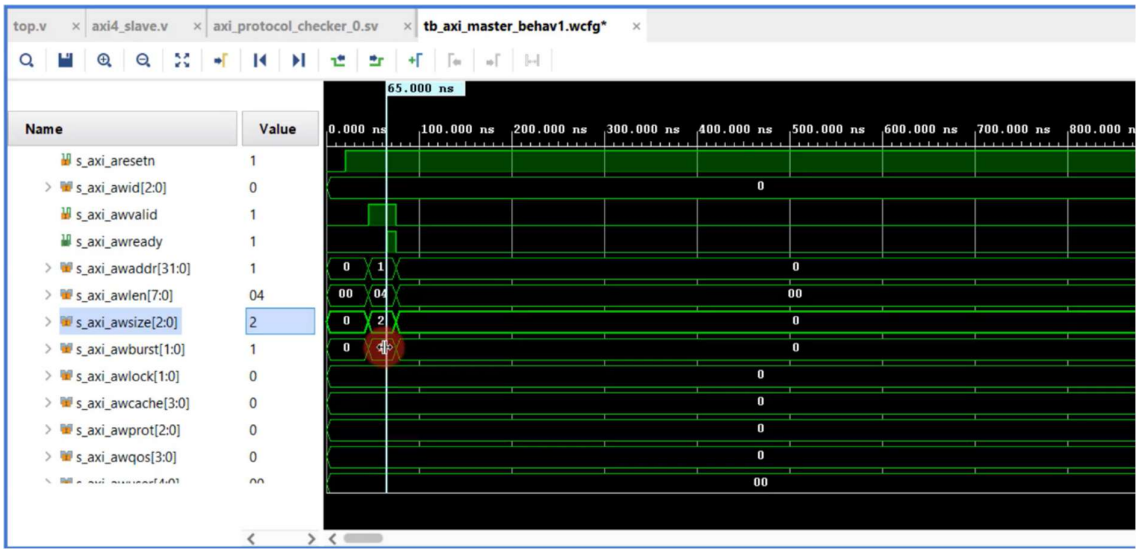
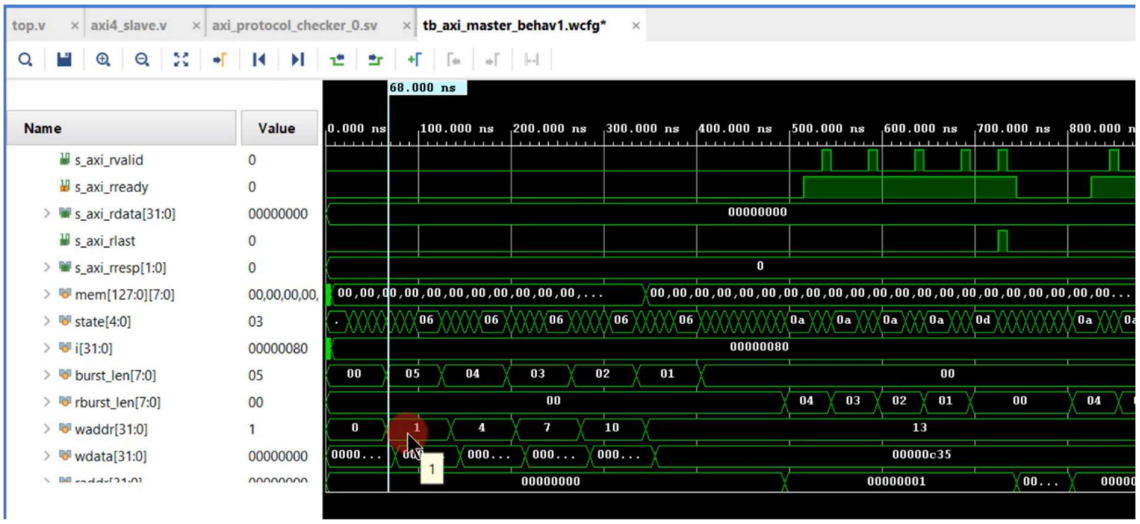
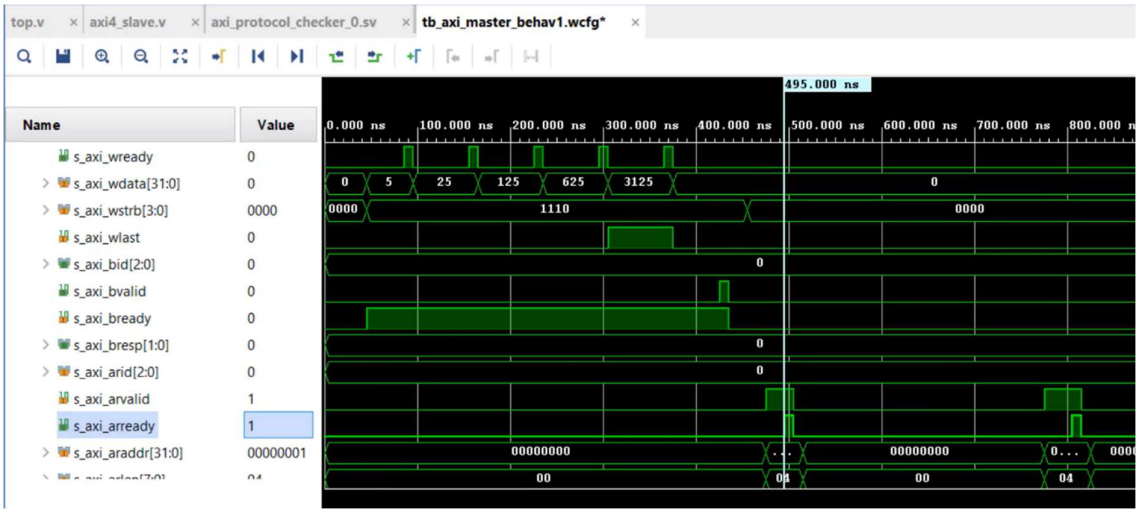


We can see that in we are 5 beats in the write transaction bcz awlen is 4 ,we can see that m_axi_bvalid is 1 from 50 to 450 ns and master receive valid response(m_axi_bvalid becomes high) near 450 ns and m_axi_bresp=0 it means data is successfully written into the salve memory.



Here we can see master has sent the base address to the slave as 1 ,each beat has 4byte data burstlen=5 .

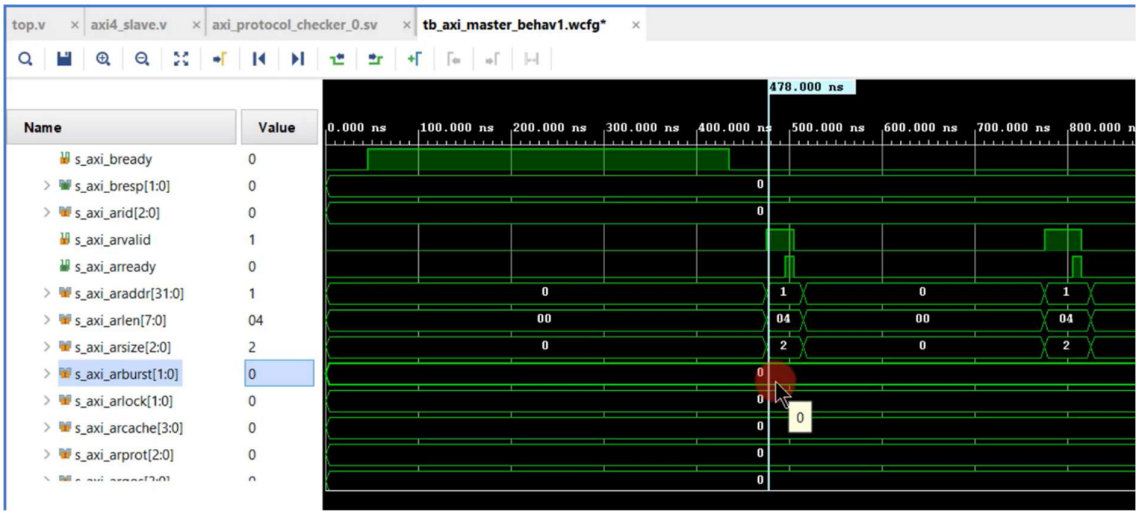




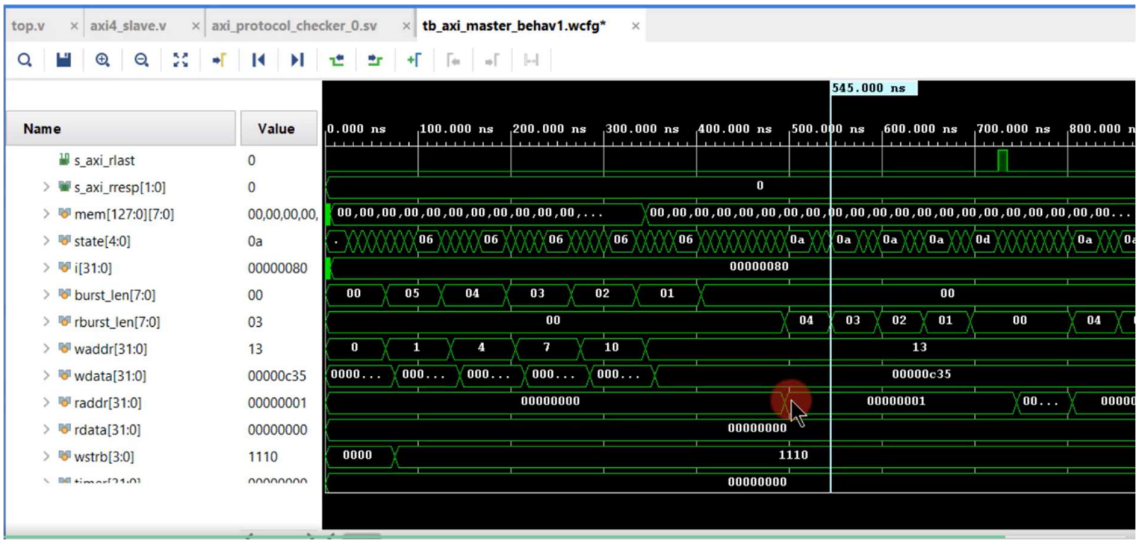
From above waveform images we can conclude that slave has successfully received the data (5,25,125,625,3125). And the value of the address to store the first data is 1 and to store the second data is 4 (it is somewhat confusing here because it looks like it should be 5 but since

Wstrb is 1110 the last beat is neglected hence we write only 3 bytes per beat and our memory can store only 1 byte at 1 location so we need to increment the address by 3).

we can also see near 500ns since s_axi_rvalid becomes high the read operation has started



Here we can see since burst mode is 0 so we are working in fixed burst mode so for every beat read our address is same (that is 1),s_axi_arlen is 4(so master is reading 5 beats from the slave). and after the successfull transmission of the data s_axi_valid goes from 0 to 1 .



we can see our s_axi_rlast becomes 1 after sending all the 5 beats to the master and since we are dealing in the fixed mode the raddr remains constant (1).