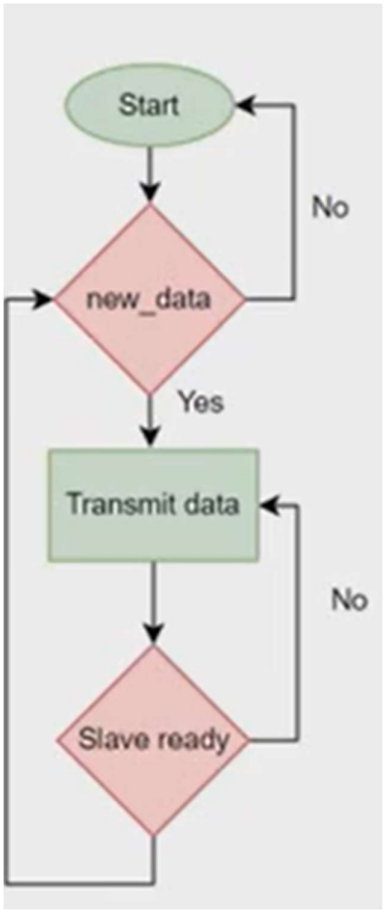
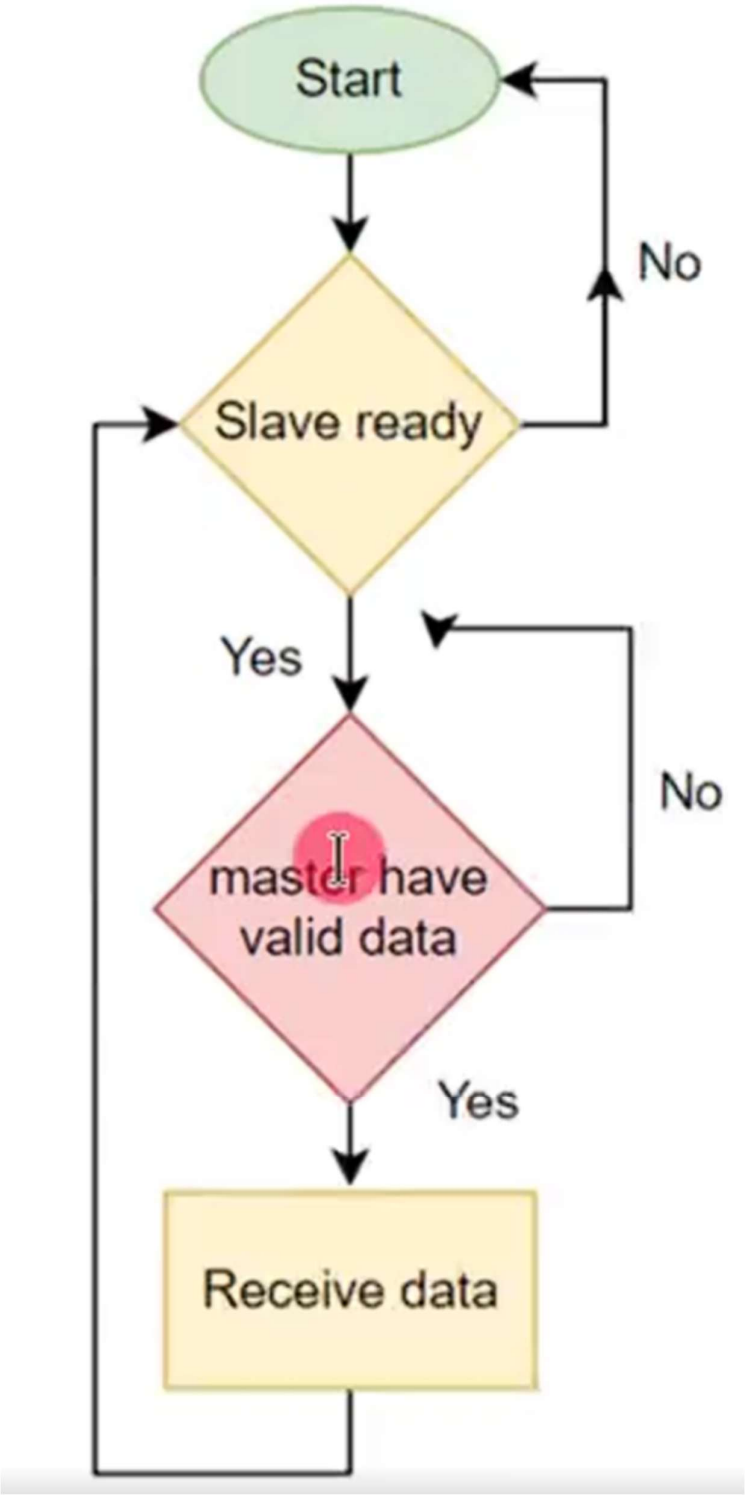
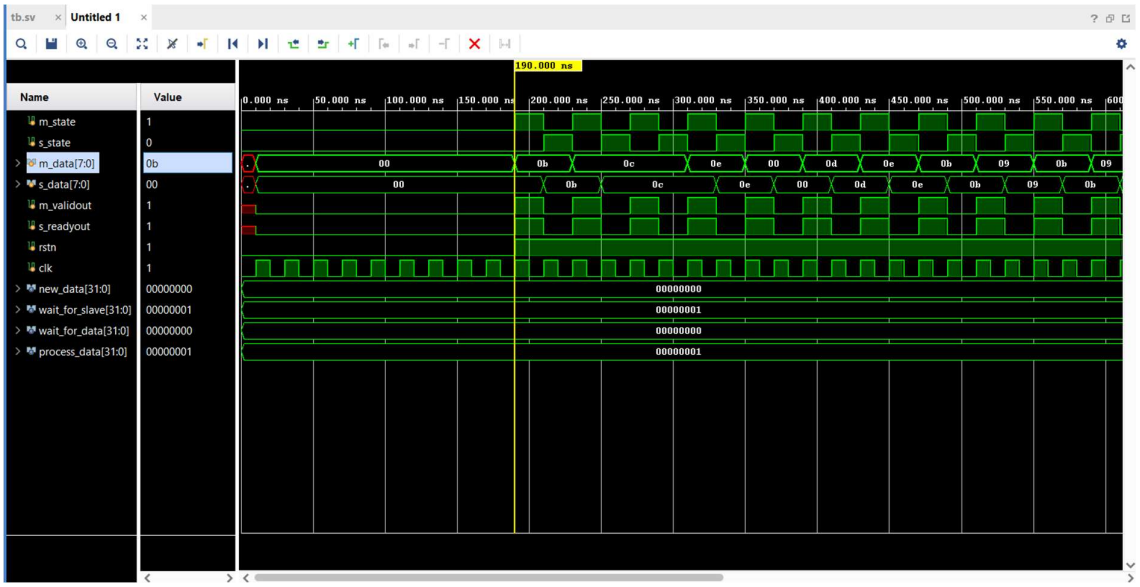


Master state diagram



Slave state diagram



Results:- both master and slave are making validout and ready high simultaneously, in the same clock cycle master sends data to the slave and when both validout and readyout are high simultaneously, in next clock cycle data is written in the slave we can verify this for data 0b in above waveforms