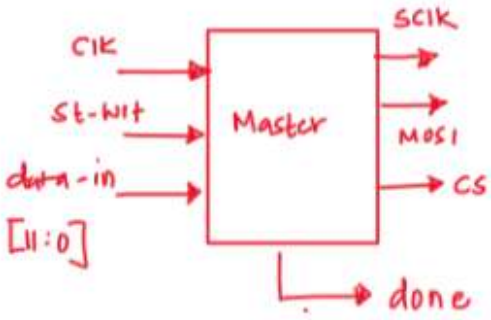
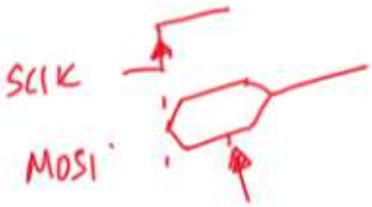
Pin	Signal	Description
1	~CS	Chip Select
2	MOSI	Master-Out-Slave-In
3	(NC)	Not Connected
4	SCLK	Serial Clock
5	GND	Power Supply Ground
6	VCC	Power Supply (3.3V/5V)

Slave (sample data on negative edge)





1.8MSPS → 1.8MHz

1MHz

160MHz

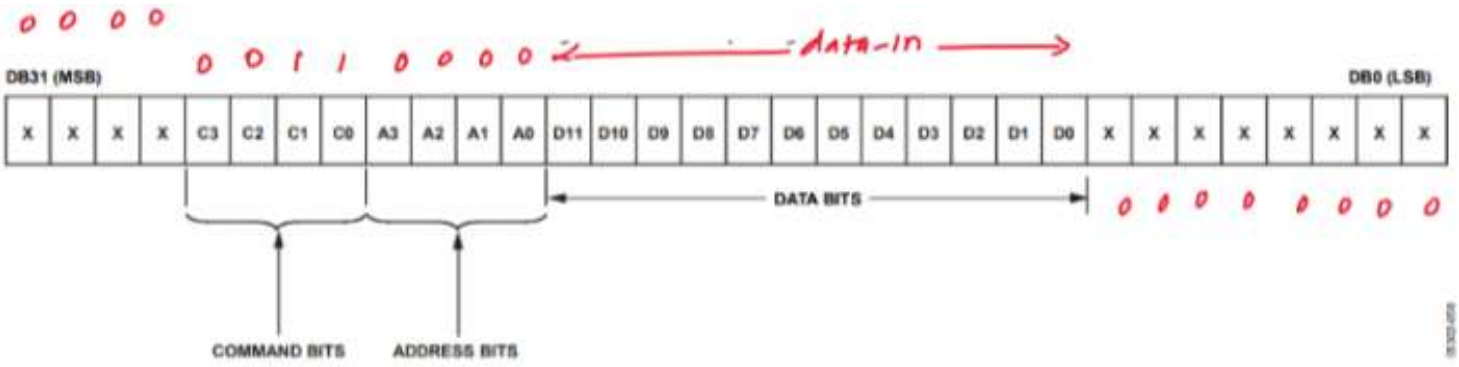


Figure 59. AD5628 Input Register Contents

Table 9. Command Definitions

Command				
C3	C2	C1	C0	Description
0	0	0	0	Write to Input Register n
0	0	0	1	Update DAC Register n
0	0	1	0	Write to Input Register n, update all (software $\overline{LDAC}$)
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up DAC
0	1	0	1	Load clear code register
0	1	1	0	Load $\overline{LDAC}$ register
0	1	1	1	Reset (power-on reset)
1	0	0	0	Set up internal REF register
1	0	0	1	Reserved
–	–	–	–	Reserved
1	1	1	1	Reserved

Table 10. Address Commands

Address (n)				
A3	A2	A1	A0	Selected DAC Channel
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	1	1	1	All DACs

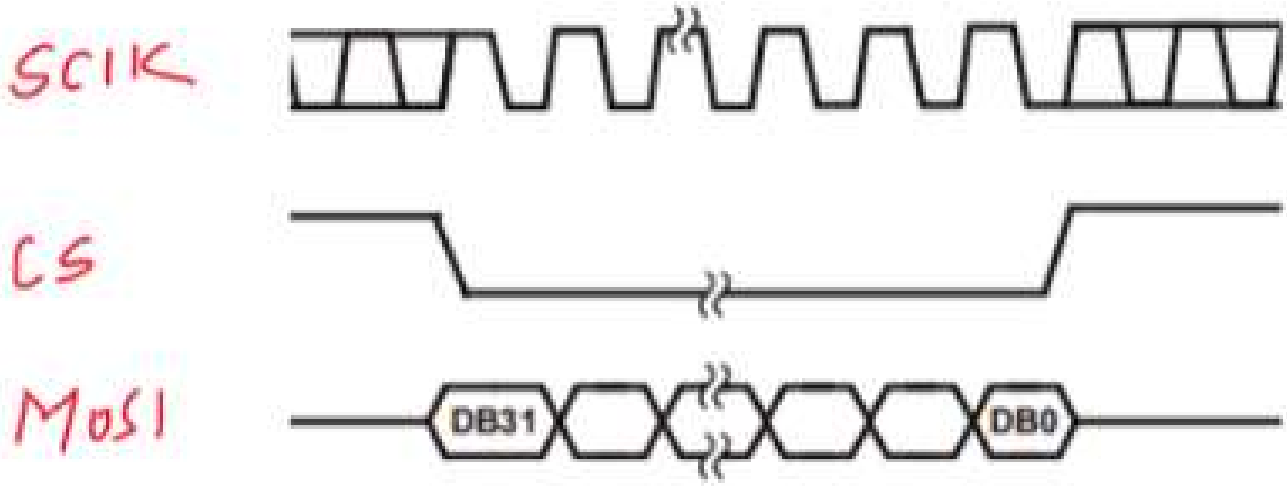
INTERNAL REFERENCE REGISTER

The on-board reference is off at power-up by default. This allows the use of an external reference if the application requires it. The on-board reference can be turned on or off by a user-programmable internal REF register by setting Bit DB0 high or low (see Table 11). Command 1000 is reserved for setting the internal REF register (see Table 9). Table 13 shows how the state of the bits in the input shift register corresponds to the mode of operation of the device.

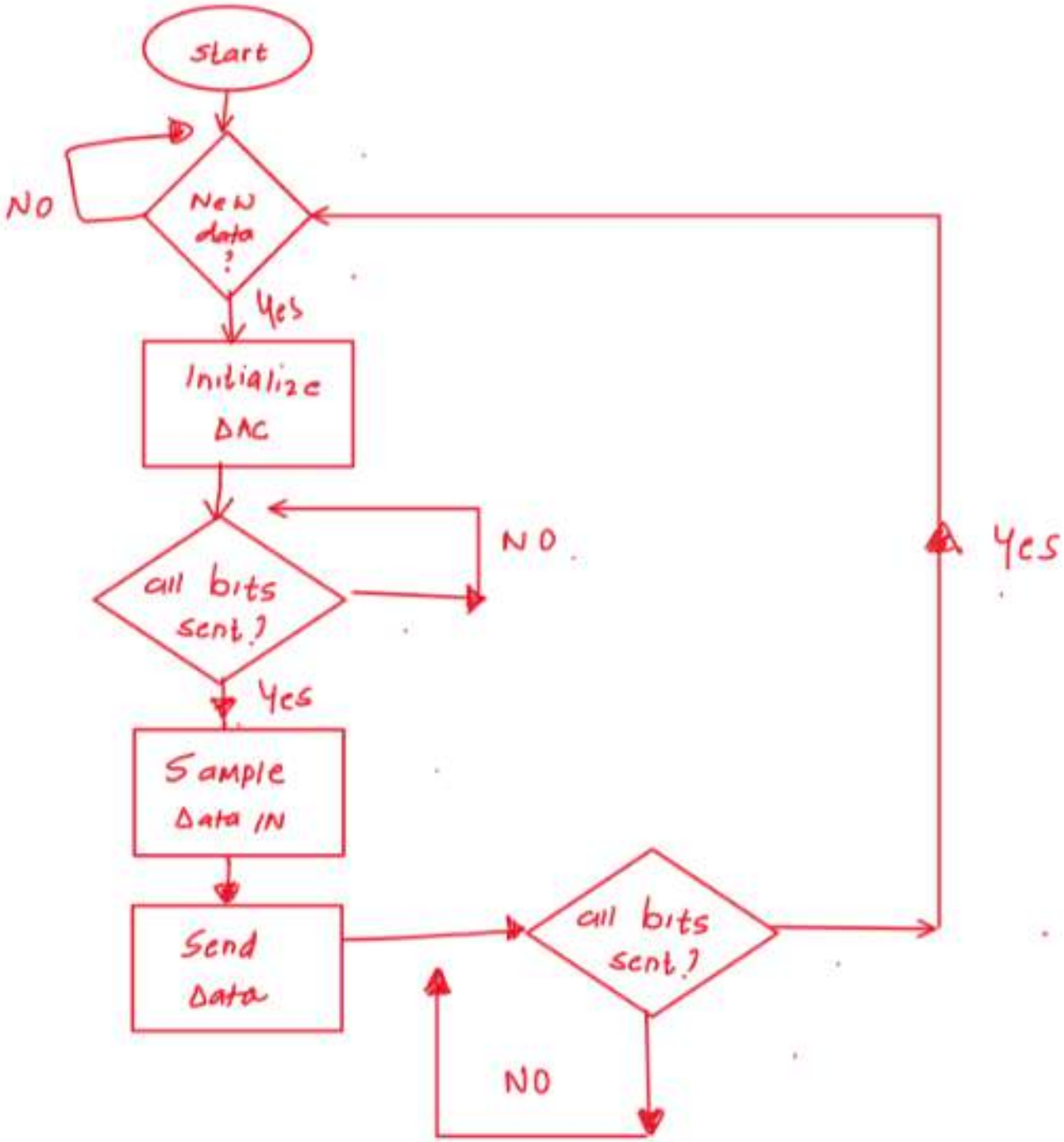
setup – $32'h08000001$

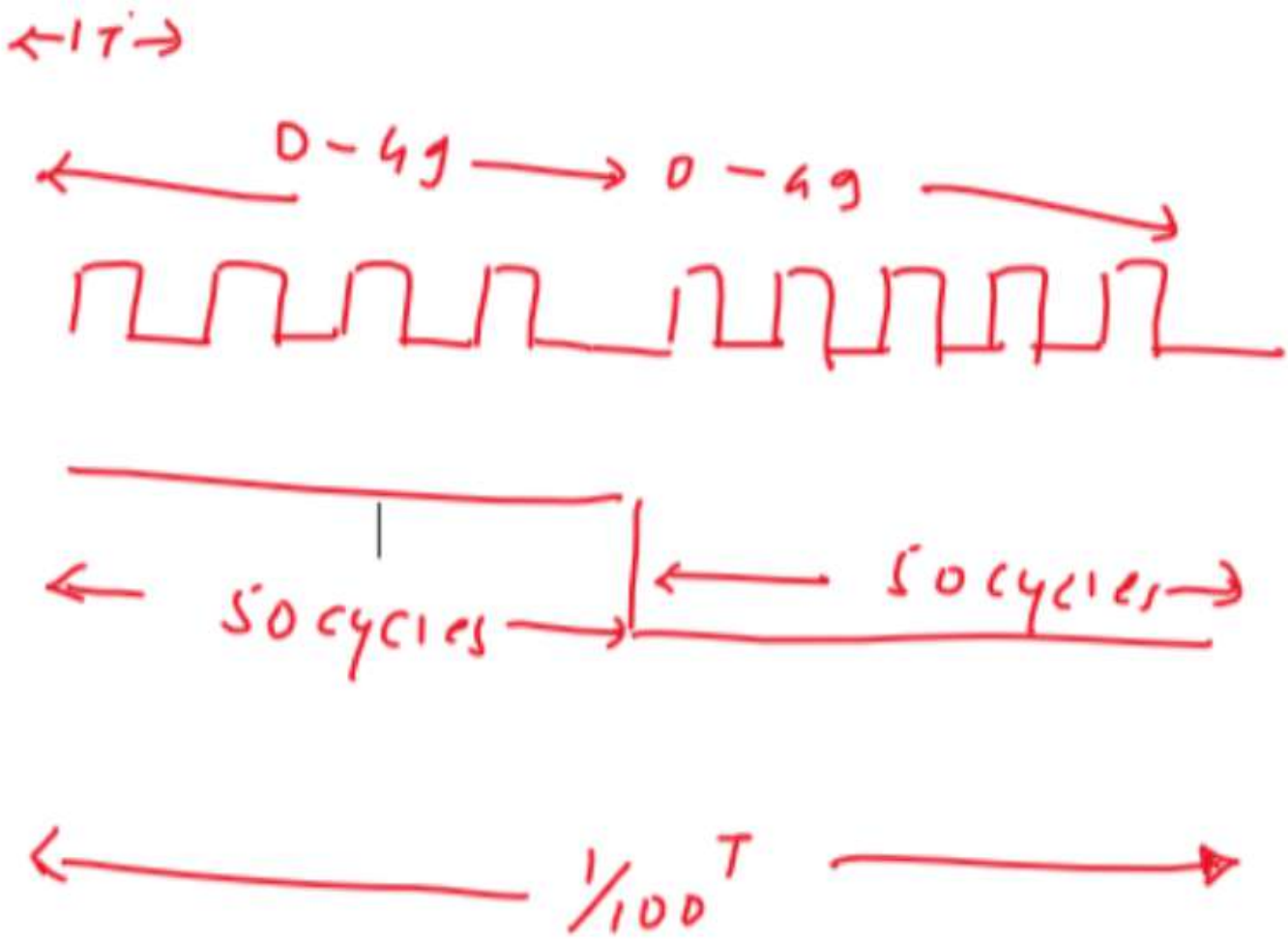
Table 12. 32-Bit Input Shift Register Contents for Reference Set-Up Command

MSB										LSB
DB31 to DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23**	**DB22**	**DB21**	**DB20**	**DB19 to DB1**	**DB0**
X	1	0	0	0	X	X	X	X	X	1/0
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)—don't cares				Don't cares	Internal REF register



VALID WRITE SEQUENCE, OUTPUT UPDATES ON THE 32ND FALLING EDGE


Start
New data ?
NO
Yes
Initialize DAC
all bits sent?
NO
Yes
Sample Data IN
Send Data
all bits sent?
NO
Yes


1T
0-4g
0-4g
50 cycles
50 cycles
1/100 T