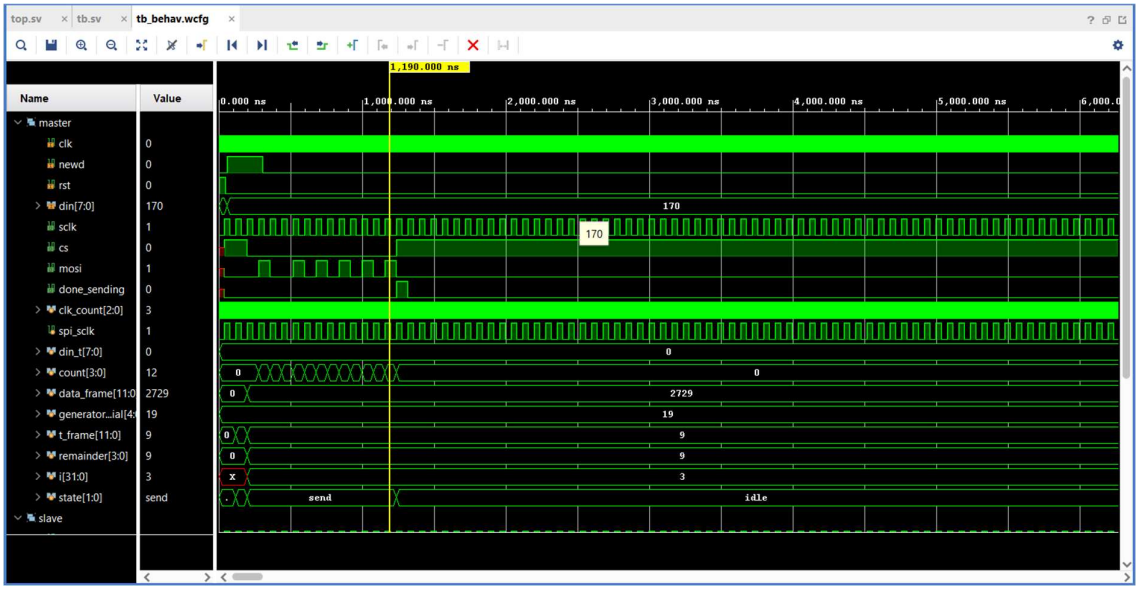
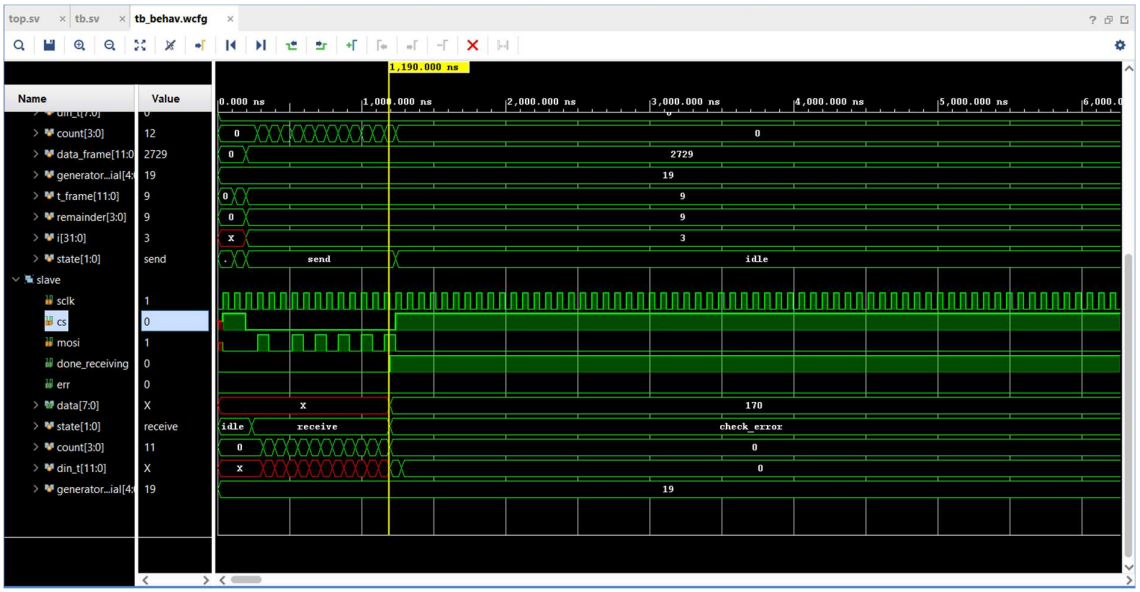
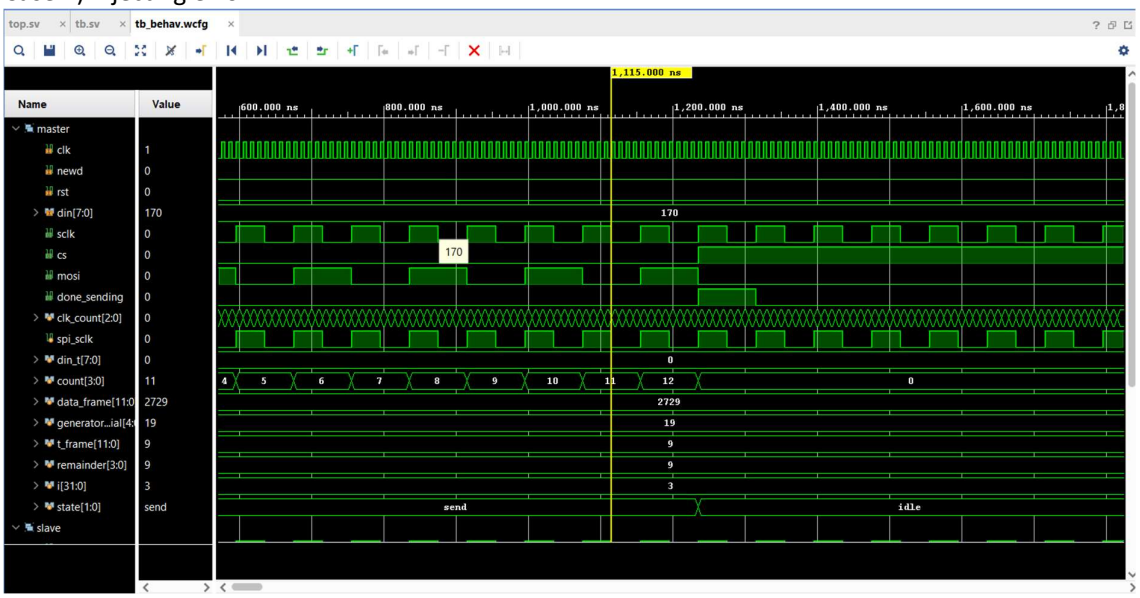
Case 1) non-erronious

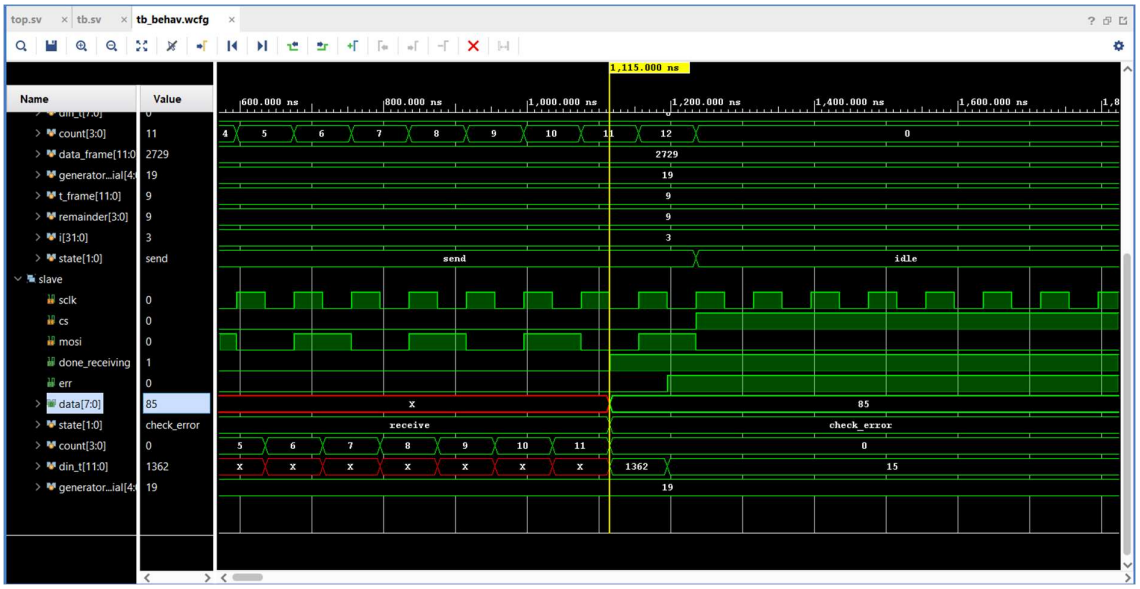




In this case I have not injected any error and I am transmitting data 170 from the master to the slave and my generator polynomial is 5’b10011 so iam transferring 2729 (in decimal) as data frame to the slave and we can see in the waveforms that slave has correctly received the data and err remains 0.

Case 2) injecting error





in this case I have done some change in the master logic

```
case(state)
      idle:begin
       if(newd)
         begin
           cs<=0;
           state<=add_crc;
           t_frame<={din,4'b0000};
```

end

I have made cs=0 just after receiving newd high on the posedge clk so slave will start receiving the data from the next negedge slave but master has not started sending data frame yet because on next posedge master will compute data_frame that it needs to send and then after it will send data to the slave so we can see that we get err=1,and slave has received the data=85,while master has sent data 170.