S.B. Roll No.....

DIGITAL ELECTONICS

3rd Exam/0620/0262/ECE/ETV/ECE(II)/CSE/CSc/EEE/Nov'17

Duration: 3Hrs. **M.Marks:75**

SECTION-A

Q1. Do as directed. **1.5x10=15**

a. A _____signal varies continuously with time.
b. The radix of octal number is_____.
c. 1's complement of 111101 is_____.
d. The number of states in Decade counter is _____.
e. The Boolean expression for OR gate is _____
f. In logic addition A+A=2A (T/F)
g. NOR and NAND gate can realize any logic function. (T/F)
h. ASCII stands for _____.
i. SIPO Stands for _____.
j. SSI stands for _____.

SECTION-B

Q2. Attempt any six questions. **6x5=30**

i. What is multiplexer? Draw the logic diagram of 4:1 multiplexer.
ii. A seven bit Hamming code is received as 1011111. Check if it is correct. If not, find the correct code if even parity is used.
iii. Draw the symbol and truth table for XOR gate and NAND gate?
iv. Draw and explain full adder circuit.
v. Differentiate between Analog and Digital signals.
vi. Define Propagation delay, Bit rate and Power dissipation.
vii. Write a note on shift register?
viii. Convert the following
i) $(110101)_2 = (\ )_{10}$ ii) $(5CB8)_{16} = (\ )_2$

SECTION-C

Q3. Attempt any three questions. **3x10=30**

a. Simplify four variable functions using K- map and implement the circuit
$F = \sum m (0, 4, 12, 8, 9, 13, 7, 15)$
b. Draw and explain working of JK flip flop.
c. Explain the operation of Decade counter.
d. Explain following.
i. Seven segment display
ii. Universal gate

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DIGITAL ELECTRONICS

3RD Exam/ECE/ECE-II/ETV/CSE/COMP/IT/EEE/0620/Nov'18

Duration: 3Hrs. **M.Marks:75**

SECTION-A

Q1. Fill in the blanks. **15x1=15**

a. In a digital system, digital signal requires _____ channel bandwidth.
b. Collection of 4 bits is called _____.
c. Radix of octal number is _____.
d. BCD numbers express each decimal digit as a _____.
e. TTL stands for _____.
f. An inverter is also known an _____.
g. The XOR gate is sometimes referred to as _____.
h. LSI & VLSI devices use _____ technology.
i. A multiplexer changes _____data into _____ data.
j. To overcome race around condition _____type of flip flop is used.
k. A ripple counter is _____ sequential circuit.
l. IC 74194 is _____ shift register.
m. The fastest A/D Converter is _____.
n. Draw symbol of XNOR.
o. The 2's complement of 11001000 is _____.

SECTION-B

Q2. Attempt any six questions. **6x5=30**

i. Convert each binary number to decimal
a) $(110011.11)_2$ b) $(101010.01)_2$ c) $(1000001.11)_2$
ii. Explain ASCII code and convert a binary 1001011 to gray code.
iii. What are the different error detection and correction codes?
iv. Discuss the characteristics of TTL Logic Family.
v. Explain the laws related to Boolean algebra.
vi. Explain De Morgan's theorems.
vii. Difference between Combinational and Sequential Circuit.
viii. Design 4 bit ring counter.

SECTION-C

Note: Attempt any three questions. **3x10=30**

Q3. Explain the universal property of NAND & NOR Gate.

Q4. Draw the Karnaugh Map for the following of four variables
i. F(A,B,C,D)=∑m(0,1,2,3,4,5,10,11)
ii. F(A,B,C,D)=∑m(2,3,6,7,10,11,14,15)

Q5. Write a short note on the following. **(any two)**
a) Half Adder b) DEMUX c) Dual slope A/D Converter.

Q6. Explain the working principle of JK Master/ Slave flip flop and its truth table.

Q7. Explain Serial to Parallel Shift Register.

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DIGITAL ELECTRONICS

3RD Exam/ECE/ETV/ECEII/Comp/CSc/EEE/0620/May'17

Duration: 3Hrs **M.Marks:75**

SECTION- A

Q1. Do as directed: **15x1=15**

a. The numbers of levels in a digital system are _____.
b. 1011 is a valid BCD number. (T/F)
c. Binary code of gray code 1011_{gray} is_____.
d. The expression A.B represents _____gate.
e. The clear signal is same as reset signal.(T/F)
f. The fastest ADC is _____.
g. The maximum count in a 4-bit ripple counter is _____.
h. To convert a JK flip-flop into T flip-flop, the inputs J=K=_____.
i. The condition S=R=1 is called as _____condition.
j. The complement of Boolean algebra AB. (BC+AC) is _____.
k. The radix of octal number is _____.
l. The parity is used for error detection and correction. (T/F)
m. _____logic family has maximum fan-out.
n. ASCII is a _____code.
o. A universal shift register can shift register left or right. (T/F)

SECTION- B

Q2: Attempt any six questions. **6x5=30**

i. Draw symbol and truth table of NOT, NAND and OR gate.
ii. Convert the following: **A)** 62_{16} X 36_{16} **B)** $341_8 = (?)_{10}$
iii. Define noise margin, propagation delay and fan-out.
iv. Compare all logic families and their characteristics.
v. Explain the operation of JK flip-flop using NAND gate.
vi. Explain dual slope A/D converter.
vii. Why universal shift registers are called universal? Explain.
viii. Draw and implement half adder.
ix. What are the applications of digital signal?

SECTION-C

Attempt any three questions **(3x10=30)**

Q3. Simplify the given K-map and draw logic circuit using gates. F(A,B,C,D)= ∑(0,3,6,7,9,13,14,15)

Q4. Explain the working of 3-bit asynchronous counter.

Q5. Draw and explain BCD to decimal decoder. Give its applications also.

Q6. Write Short note on any two:

(a) 4-bit adder
(b) D/A converter
(c) Buffer register
(d) Latch and flip-flop

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DIGITAL ELECTRONICS

3rd Exam/ECE/ETV/ECE-II/Comp/IT/CSc/EEE/0620/May'18

Duration: 3Hrs. **M.Marks:75**

SECTION-A

Q1. Do as directed. **10x1.5=15**

a. Radix of Hexadecimal number is _____.
b. ASCII code is ____ bit code.
c. IC 7402 is _____ gate.
d. BCD stands for_____.
e. The expression A+B represents _____ gate.
f. 1011 is a valid BCD number. (T/F)
g. 2's compliment of 1101 is _____.
h. CMOS stands for _____.
i. 8:1 Multiplexer has _____ number of select lines.
j. SSI stands for_____.

SECTION-B

Q2. Attempt any five questions. **5x6=30**

i. What are advantages of digital signal?
ii. Draw and explain Half Adder.
iii. Explain the working of 3 bit asynchronous counter.
iv. Explain Universal gates with diagrams.
v. Define noise margin, propagation delay and fan-out.
vi. Describe Ring counter with timing diagram.
vii. Explain the function of JK flip flop?
viii. Explain dual scope A/D converter.

SECTION-C

Q3. Attempt any three questions. **3x10=30**

a. Draw symbol and truth table of various logic gates.
b. Simplify the given K-map and draw logic circuit using gates:
   $F(A,B,C,D)= \sum(0,3,6,7,9,13,14,15)$
c. Draw and explain BCD to decimal decoder. Give its applications also.
d. Describe the operation of Universal Shift Register.
e. Draw and explain the Full Subtractor.

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DIGITAL ELECTRONICS
3rd Exam/ECE/CSE/IT/0195/Nov'19
(FOR 2018 BATCH)

Duration: 3Hrs. **M.Marks:75**

SECTION-A

Q1. Do as directed. **15x1=15**

a. 1's complement of 1001 is_____.
b. Radix of a binary number is _____.
c. The expression **A.B** represent _____ gate.
d. ASCII is _____ bit code.
e. _____signal varies continuously with time.
f. A+A=_____
g. A Combinational Circuit does not have _____
h. Race around condition can be avoided by using Master Slave JK Flip Flop.(T/F)
i. A demultiplexer is a circuit with many inputs but only one output. (T/F)
j. NAND and NOR gate can realize any logic function (T/F).
k. SSI stands for _____
l. BCD stands for _____
m. CMOS stands for _____
n. SIPO stands for _____
o. Draw symbol of XOR gate

SECTION-B

Q2. Attempt any six questions. **6x5=30**

a. Draw and explain the circuit for Full Adder.
b. Differentiate between analog and digital signal.
c. Define Multiplexer. Explain 4:1 mux with the help of a diagram.
d. Define shift register. Explain its types.
e. Explain the universal property of NAND Gate
f. Define Propagation delay and power dissipation
g. Convert: - 1. $(25)_{10} = (?)_2$ 2. $(B3F5)_{16} = (?)_{10}$
h. Differentiate between combinational and sequential circuit
i. Describe the working of seven segment display.

SECTION-C

Q3. Attempt any three questions. **3x10=30**

i. Exaplain contruction and working of SR flip flop.
ii. Define counter and explain the working of decade counter
iii. Define Logic Gate. Explain its various types along with symbols and truth tables.
iv. Simplify the function using K-map and implement the Circuit.
F=Σm (0, 4, 12, 8, 9, 13, 7, 15)
v. Write short notes on the following. a) ASCII Code b) Parity

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DIGITAL ELECTRONICS

3rd Exam/ECE/ETV/ECE-II/CSE/Comp/IT/EEE/0620/May'19

Duration: 3Hrs. **M.Marks:75**

SECTION-A

Q1. Fill in the blanks. **15x1=15**

a. Two's compliment of 110101 is_____.
b. Hexadecimal system uses digits from_____.
c. Hamming code is a one type of _____ code.
d. BCD stands for _____.
e. Boolean rule (A+B) (A+C)=_____
f. Half adder is also known as _____.
g. Flip flop is not a _____ circuit.
h. Race around condition do not occur in _____FF.
i. Data is said to be in serial form if the bits are available _____
j. Analog to digital conversion is _____ complex than digital to analog conversion.
k. LCD consumes _____ power than LED display.
l. RAM stands for_____.
m. A _____ signal varies continuously with time.
n. For decade counter no. of Flip-Flop required will be_____.
o. A NAND gate acts as a _____ OR gate.

SECTION-B

Q2. Attempt any five questions. **5x6=30**

i. Explain the Laws related to Boolean algebra.
ii. What do you mean by BCD codes? Explain.
iii. Explain operation of seven segment display.
iv. Explain various characteristics of standard TTL family.
v. Explain RAM and ROM.
vi. Differentiate between a multiplexer and a Demultiplexer.
vii. Write down the application of A/D and D/A converter.
viii. Explain briefly the functioning of a serial in parallel out shift register.

SECTION-C

Q3. Attempt any three questions. **3x10=30**

a. Explain the working and construction of dual slope ADC.
b. Discuss the OR, AND, NOT, NAND, NOR gates with their symbols and truth tables.
c. What is latch? Explain working principle of J-K master/slave flip flop and draw its truth table.
d. Write short note on the following. **(any two)** i) Hamming Code ii)Parity iii) Ring counter
e. Minimize and realize following logic functions using K-map
   f (A,B,C,D) = ∑m (0,1,2,5,8,9,10)

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DIGITAL ELECTRONICS

3rd Exam/ECE/ETV/ECE-II/CSE/EEE/0620/SEP'2020

Duration: 1.15 Hrs. **M.Marks:25**

SECTION-A

Q1. Attempt any three questions. **3x5=15**

a. Convert the following: i) $85.63_{10}=X_2$ ii) $300.45_{10}= (?)_8$
b. Draw symbol and truth table of NAND gate.
c. Define noise margin, propagation delay and figure of merit.
d. List the difference between analog and a digital signal.
e. Draw and explain asynchronous Mod-5 counter.
f. What are shift registers? Give its types.
g. Draw and explain 2:1 Multiplexer
h. Draw and implement half adder.
i. What are the applications of shift registers?

SECTION-B

Q2. Attempt any one question. **1x10=10**

i. Simplify the following K-map and draw logic circuit using gates.
F (A,B,C,D)= ∑(1,5,7,8,9,10, 11,14 ,15)
ii. Explain the working and construction of a successive approximation type of ADC.
iii. Draw and give truth table of JK flip-flop. What is race around condition in JK flip-flop? How it can be avoided.
iv. Write Short note on the following. a) decoder b) combination circuit c) parity

S. B. Roll. No……

DIGITAL ELECTRONICS

3rd Exam/ECE/ETV/ECE-II/Comp/CSE/EEE/IT/0620/Jun'2021

Duration: 1.15Hrs. **M.Marks:25**

SECTION-A

Q1. Attempt any three questions. **3x5=15**

i. What are the advantages of Digital signals?
ii. Describe NAND gate as universal gate.
iii. Describe Ring counter.
iv. Differentiate Weighted and non-weighted codes.
v. Draw symbol and truth table of NOT, AND and NOR gate.
vi. List the difference between combinational and a sequential circuits.
vii. What are shift registers? Give its types.

SECTION-B

Q2. Attempt any one question. **1x10=10**

a. Simplify the following K-map and draw logic circuit using gates. F (A,B,C,D)= ∑m(0,4,12,8,9,13,7,15)
b. Explain the working and construction of a dual slope type of ADC.
c. Draw and give truth table of JK flip-flop. What is race around condition in JK flip-flop? How it can be avoided.
d. Explain the working of 3-bit asynchronous counter.

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DIGITAL ELECTRONICS
3rd Exam/ECE/IT/CSE/0195/Jun'2022
(For 2018 Batch Onwards)

Duration: 3Hrs. **M.Marks:75**

SECTION-A

Q1. Do as directed. **15x1=15**

a. The no. of bits in a nibble is _____.
b. Octal system uses digits from_____.
c. Decimal 8 in excess-3 code is _____.
d. A+ (B.C) = _____.
e. BCD stands for_____.
f. _____ changes serial data into parallel data.
g. A Half adder adds _____ bits.
h. _____ And _____ are UNIVERSAL gates.
i. A flip flop is memory element.(T/F)
j. EPROM is available in all technologies.(T/F)
k. ASCII stands for_____.
l. 4:1 Multiplexer has _____ number of select lines.
m. Race around condition can be avoided by using Master Slave JK flip flop .(T/F)
n. PIPO stands for _____.
o. LED stands for_____.

SECTION-B

Q2. Attempt any six questions. **6x5=30**

i. Differentiate between Analog and Digital signals?
ii. Draw and explain the circuit for half subtractor?
iii. Define SSI, MSI, LSI, VLSI and ULSI?
iv. What is a T flip flop? Show its symbol and draw truth table for negative edge triggered T flip flop?
v. Draw logic circuit of 4:1 multiplexer and explain its working?
vi. Differentiate between asynchronous and synchronous counters?
vii. Explain the working of decade counter?
viii. Draw the circuit of parallel in- parallel out shift register and explain its working?

SECTION-C

Q3. Attempt any three questions. **3x10=30**

a. Explain working and construction of JK flip flop. How Race around condition can be avoided by using Master Slave JK flip flop?
b. Define logic gate? Explain various logic gates along with symbols and truth tables?
c. Minimize and implement in SOP form
F (A, B, C, D) = ∑m (1, 2, 3, 6, 8, 12, 14, 15)
d. Draw and explain the circuit for half adder and full adder?
e. Explain the following i) Universal shift registers ii) seven segment display