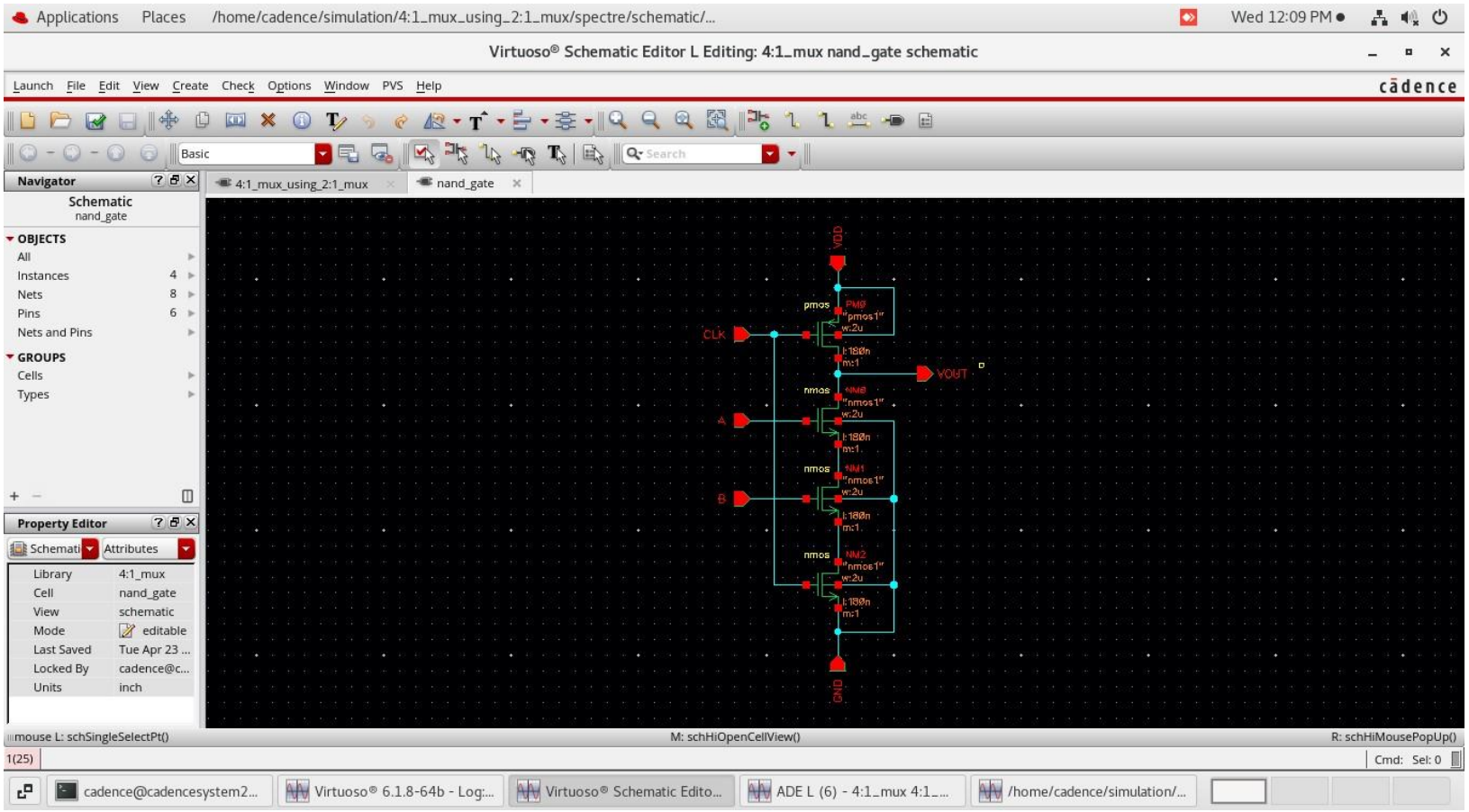
PROBLEM STATEMENT: 4:1 MUX USING DYNAMIC CMOS LOGIC

DESIGN AND IMPLEMENTATION:

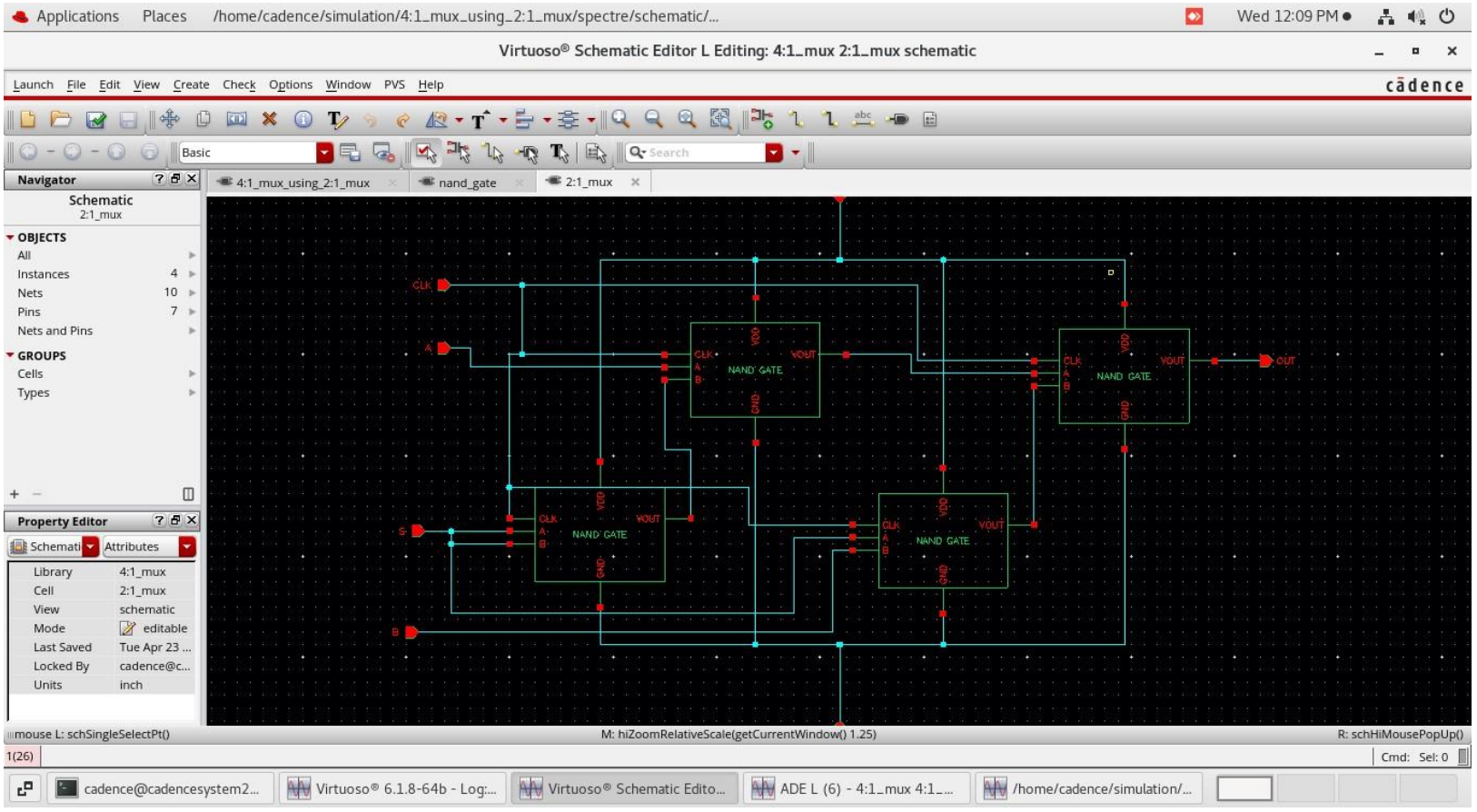
To implement 4:1 mux, first a NAND gate is created using dynamic CMOS logic. It requires 1 PMOS device placed at the top (with its source and body terminals connected to VDD) and and 3 NMOS devices placed in continuation (with source of the last NMOS and all body terminals grounded). The PMOS at the top and NMOS below form the basic structure for dynamic CMOS logic. Both of these are powered by a clock signal. When clock is 0, the circuit is in precharge phase. When clock is 1, the circuit is in evaluate phase which means it functions as a normal NAND gate. Hence it can be considered as a clock enabled nand gate. In the middle the pull down network (2 NMOS in this case) with the inputs (A,B) is placed. The output is obtained at the drain of the PMOS. A symbol is

created for this standard cell on Cadence tool for its further use. The schematic for this is shown below.

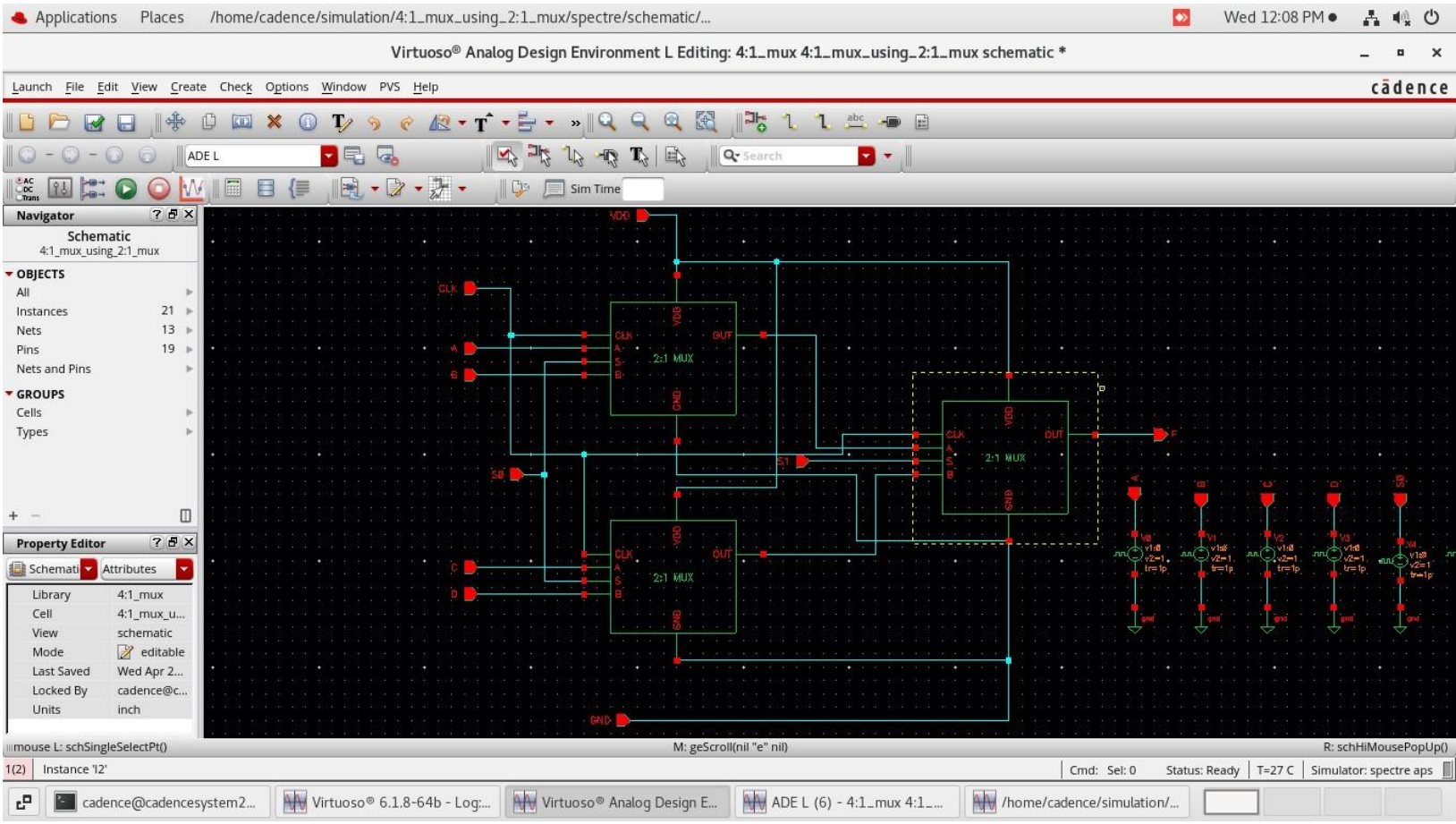


This NAND gate is imported as a symbol and used as a universal gate to create a 2:1 mux. The connections between all the pins are made appropriately. The extra clock pins of all the NAND gate symbols are connected together and kept separate from other connections. A symbol is created for this with an extra clock terminal. There are mainly 2 inputs A and B, 1 select line, a clock to control the functionality and 1 output pin. There is also a

VDD pin on top and ground at the bottom. The schematic below shows all the connections clearly.



2:1 mux symbol is imported to create the final circuit which is the 4:1 mux. All clock terminals are again connected together and kept separate from other pins. Rest of the connections are made as shown in the schematic below. Now there are 4 main inputs A,B,C,D, 2 select lines S1 and S0 and 1 output along with VDD and ground terminals. The clock signal controls the functionality of the circuit (evaluate phase for 4:1 mux operation) as stated earlier.

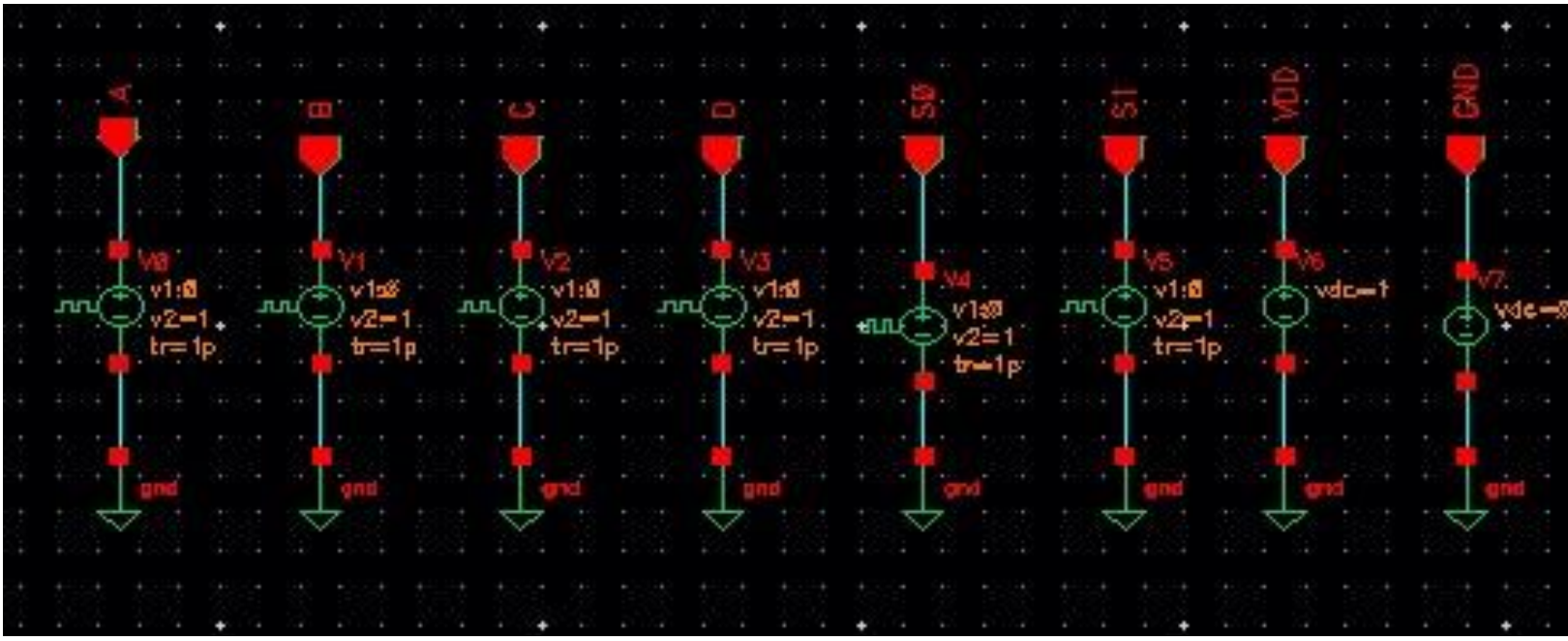


SPECIFICATIONS AND INPUT PARAMETERS:

The gpdk180 library on cadence tool is used for the entire implementation. For the NMOS and PMOS specifications, the default values are used.

Clock signal value is taken as constant 1 (evaluate phase) to show functionality of the circuit. Vdc from analoglib is used for this. VDD is also connected to Vdc. Other inputs : A,B,C,D,S0,S1 are connected to Vpulse (from analoglib)

with different pulse widths to show the output waveform for each testcase.



Vpulse: Voltage 1: 0 V, Voltage 2: 1V, Delay time: 0s, Rise time=1ps, Fall time=1ps

A: Period=80ns, Pulse width=40ns

B: Period=40ns, Pulse width=20ns

C: Period=20ns, Pulse width=10ns

D: Period=10ns, Pulse width=5ns

S0: Period=80ns, Pulse width=40ns

S1: Period=40ns, Pulse width=20ns

Vdc:

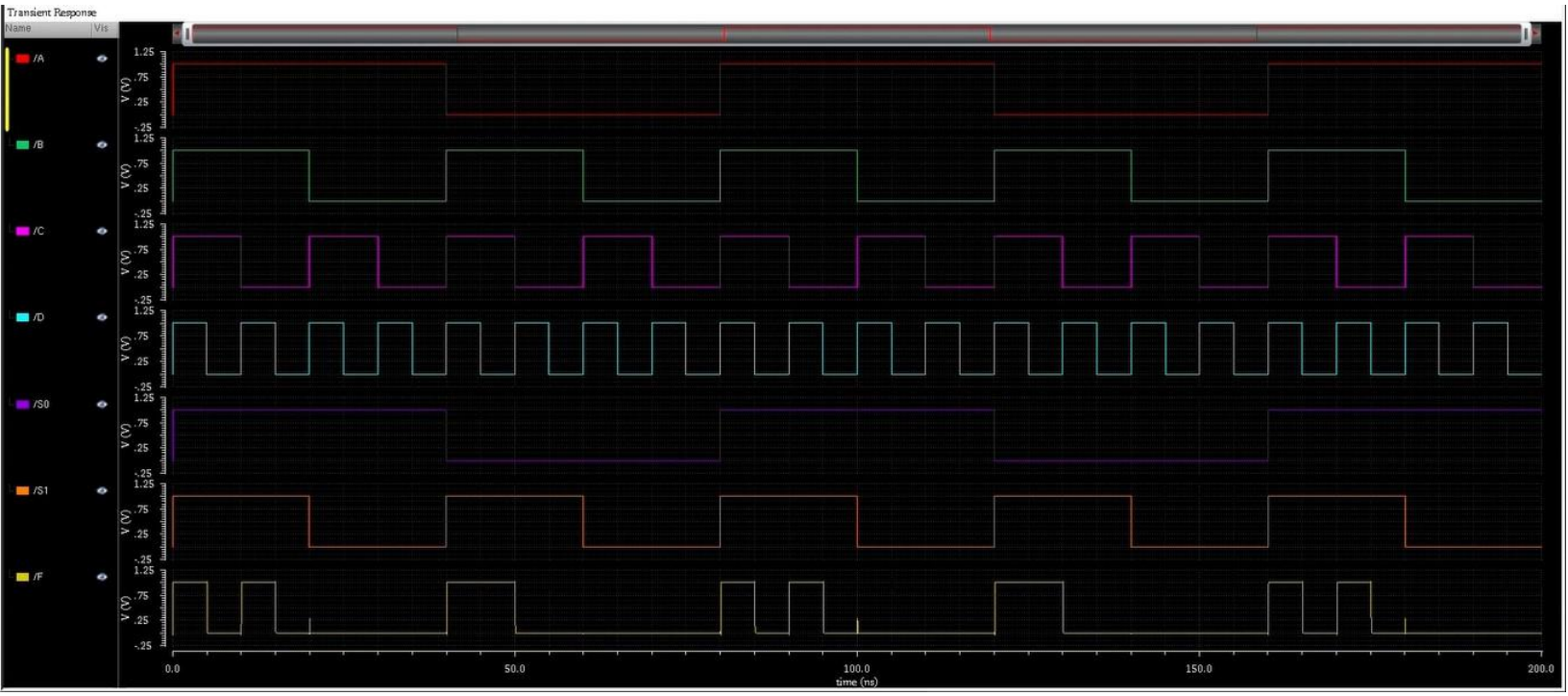
CLK: DC voltage=1V

VDD: DC voltage=1V

GND: DC voltage=0V

OUTPUT:

Transient analysis is done by selecting the pins: A,B,C,D,S0,S1 and F(output pin). Stop time is set as 200ns. Truth table for 4:1 mux can be verified from the output waveforms.



CLK	S0	S1	F
1	0	0	A
1	0	1	C
1	1	0	B
1	1	1	D