# The Simplest CPU Arch Possible(SCAP)

## 1:System specs

### 1.0:Registers

The simples CPU architecture possible(SCAP for short) has the following registers:

| BIN | HEX | NAME | BITS | Init Val |
|---|---|---|---|---|
| **00** | 0x0 | A | 8 | 0x00 |
| **01** | 0x1 | B | 8 | 0x00 |
| **inaccessable** | inaccessable | PC | 16 | 0x0000 |
| **10(upper) and 11(lower)** | 0x2(upper) and 0x3(lower) | SP | 16 | 0x00FF |
| **inaccessable** | inaccessable | FLAGS | 2 | 0b00 |

### 1.1:Instructions

And the following instructions:

| BIN | HEX | NAME | I/O |
|---|---|---|---|
| **0000** | 0x0 | *LD* | REG1,ADDR |
| **0001** | 0x1 | ST | REG1,ADDR |
| **0010** | 0x2 | MV | REG1,REG2 |
| **0011** | 0x3 | *ADD* | REG1,REG2 |
| **0100** | 0x4 | *SUB* | REG1,REG2 |
| **0101** | 0x5 | *LDP* | REG1,REG2 |
| **0110** | 0x6 | *PUSH* | REG1 |
| **0111** | 0x7 | *POP* | REG1 |
| **1000** | 0x8 | *JMP* | ADDR |
| **1001** | 0x9 | *JZ* | ADDR |
| **1010** | 0xA | *JNZ* | ADDR |
| **1011** | 0xB | *JC* | ADDR |
| **1100** | 0xC | *JNC* | ADDR |
| **1101** | 0xD | *CALL* | ADDR |
| **1110** | 0xE | *RET* | - |
| **1111** | 0xF | *NOP* | - |

## 2:Memory

### 2.0:Details for external hardware support

The SCAP has an 8 bit data bus and a 16 bit address bus. The memory layout can be anything on devices using SCAP, so you may want to keep the devices mappde between 0xFF00 and 0xFFFD.

## 3:Instruction format

```
 xxxx xx xx xxxxxxxxxxxxxxxx
  ^     ^  ^                ^
  |     |  REG2     ADDR
  |     REG1
OPCODE
```

## 4:Interrupts

When the interrupt line is pulsed, the CPU jumps to the address whose lower byte is the byte read from 0xFFFE and upper one is the byte read from 0xFFFF. Interrupts behave like CALL instructions.