BRAC University

Semester: Summer 25, 2025

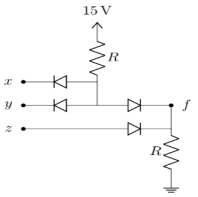
CSE 251(Section:10)

Assignment: 2	**Deadline: 25th july, 2pm**	**Marks:** 100
Q1-Q5: CO2		

Q1. Diode logic gates. [20]

a) Design a logic circuit using ideal diodes to implement the logic function f(A,B,C,D) . The function gives a logical high **if all of the A,B,C inputs are simultaneously high or D is high**.

b) Design an ideal diode based ckt. to get the **largest voltage output** from 3 voltages.

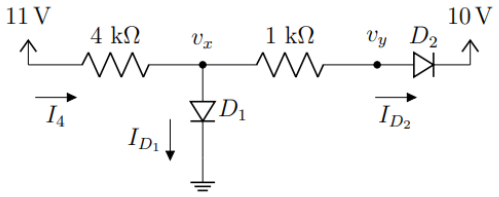


c) i)Deduce the logic function for the given circuit below.

ii)what will be the output voltage if Vx=7V, Vy= 4V, Vz= 2V assuming both ideal model and CVD(0.7V) model.

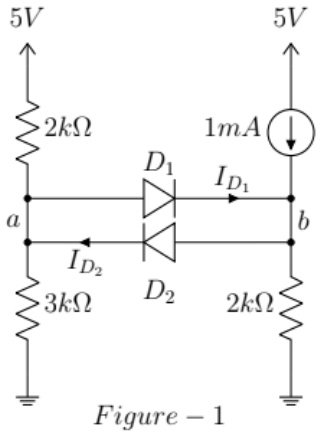
Q2-Q5 (Diode ckt solve using method of assumed states)

Q2. Analyze the following circuit to **find the values of I_{D1} , I_{D2} , v_x, and v_y**. Here, use the Method of Assumed State using the CVD model of diode with V_{D0} = 0.7V. [20]



Q3) Solve the diode network ckt to **find the V_a, V_b and diode currents** . [20]

(Solve using method of assumed states using the CVD model of diode with V_{D0} = 0.8V)



$Figure - 1$

(20)

Q4) Solve the circuit **for the diode currents and voltages at all nodes**. Use the Method of Assumed State using the CVD model of diode with V_{D0} = 0.6V
[20]

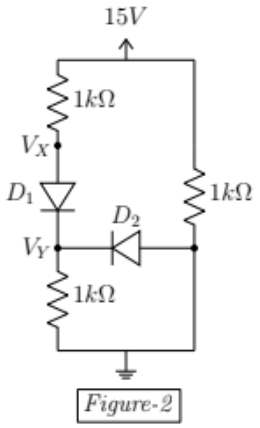
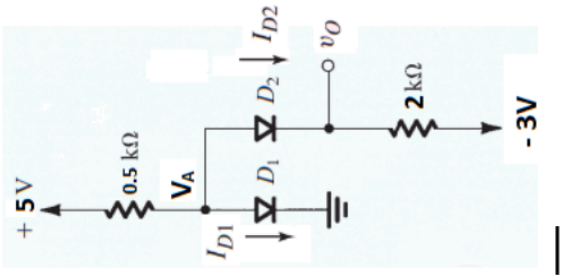


Figure-2

Q5)



Analyze the following circuit. **Calculate** the values of V_A, V_0, I_{D1}, and I_{D2}. You must validate your assumptions. Use the Constant-Voltage Drop model with a cut in voltage of 0.6V [V_{D0} = 0.6 V]. *[Hints: You may start with calculating the voltage values first]*