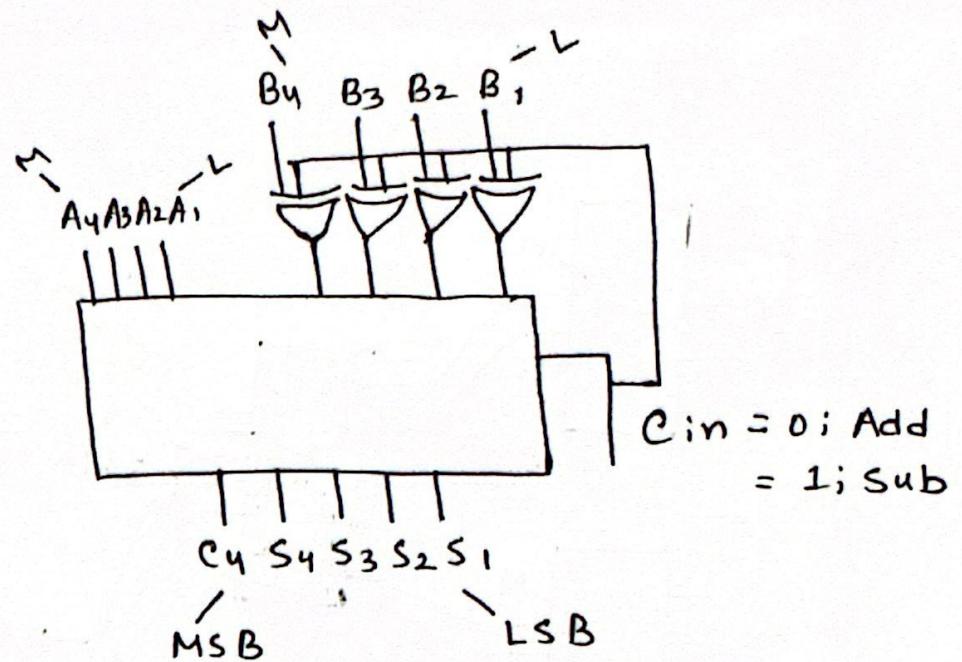


**For all the following:** Make sure that your circuit is efficient, meaning you should use the lowest number of components. You may use external gates if required.

- Build an adder cum subtractor (4 bits)
- Draw the block diagram of a 20 bits parallel adder.
- Build a 13 person voting system using full and parallel adders.
- Build a 8 person voting system using full and parallel adders.
- Build a 15 person voting system using full and parallel adders.
- Consider A is a 4 bit number. Design  $A - 3$  using a 4 bit parallel adder. Use external gates if required.
- Consider A is a 4 bit number. Design  $A + 3$  using a 4 bit parallel adder. Use external gates if required.
- Consider two numbers: 7 and 5. You can only calculate addition and subtraction between those two numbers. Design a circuit that can perform the above calculations based upon the user's intention.

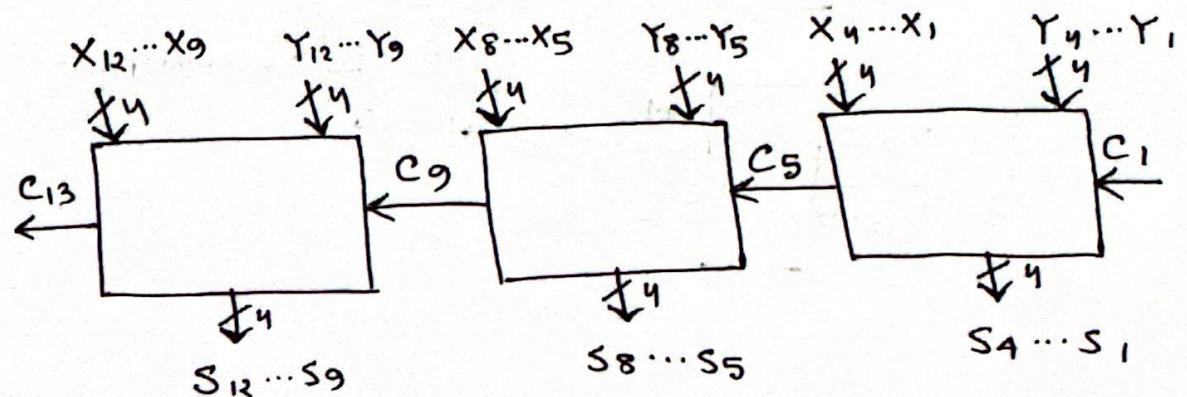
- Design a full adder using two half adders. You must use two NOR gates and no OR gates.
- Design a full adder using two half adders. You must use three NAND gates and no OR gates.
- Build a circuit that implements the 2's complement number system (3 bits) using encoder(s) and decoder(s).
- Design an Octal to Binary encoder.
- Design a 4x2 priority encoder prioritizing MSB.
- Design a 4x2 priority encoder prioritizing LSB.

(1)

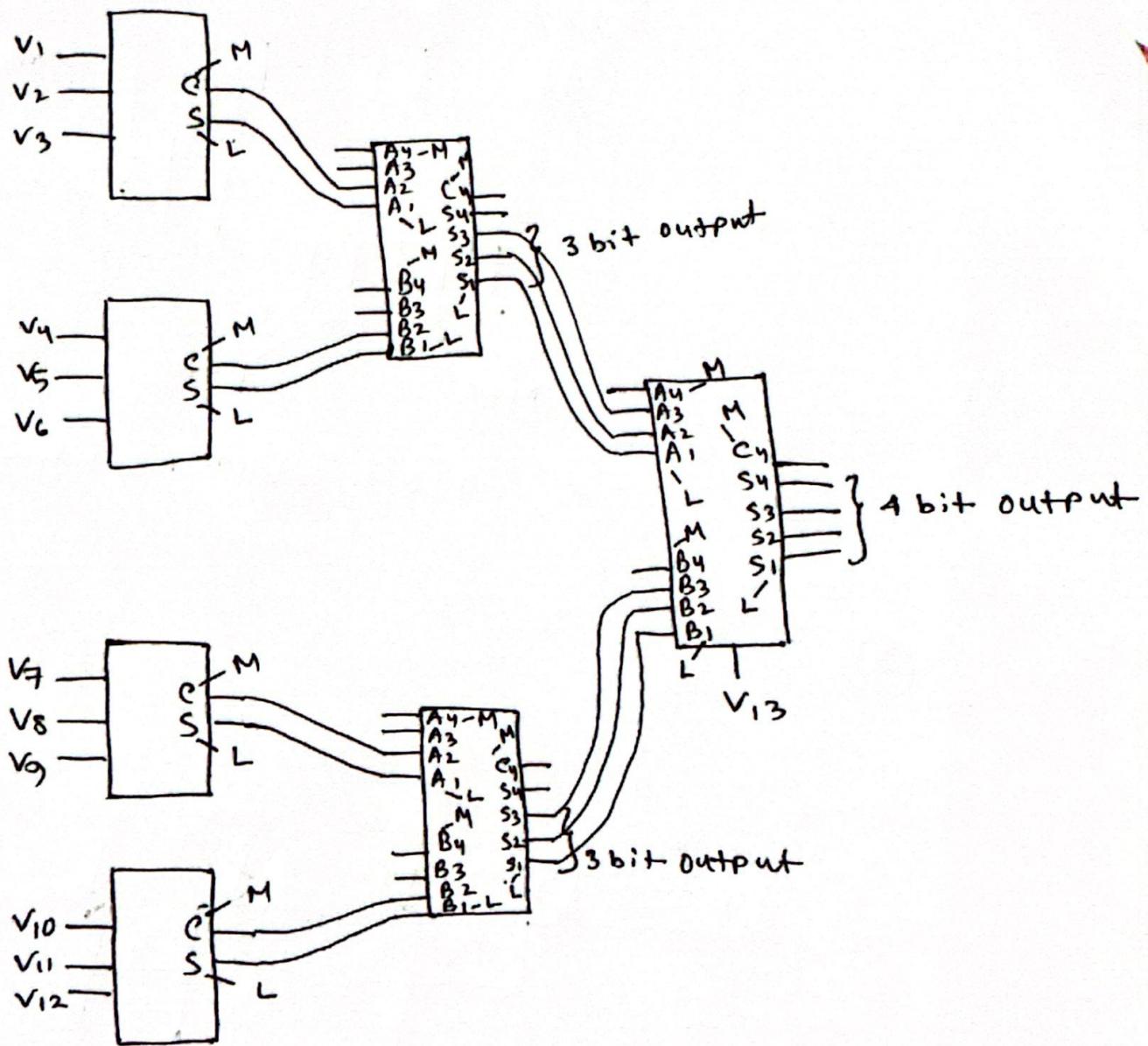


A bit adder-subtractor

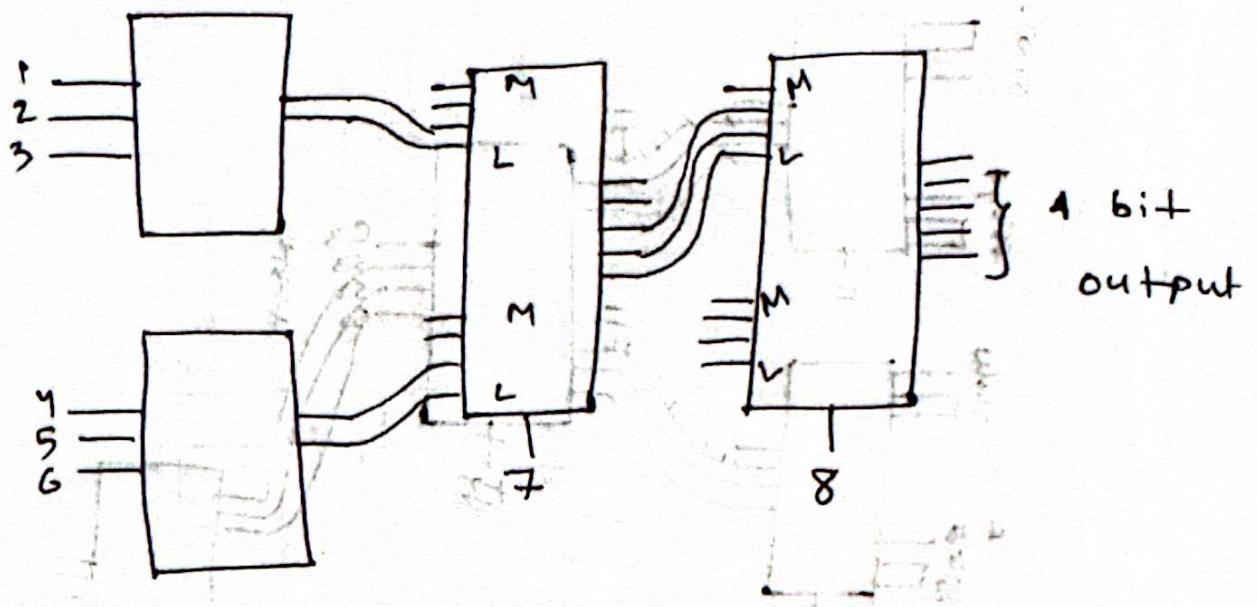
(2)



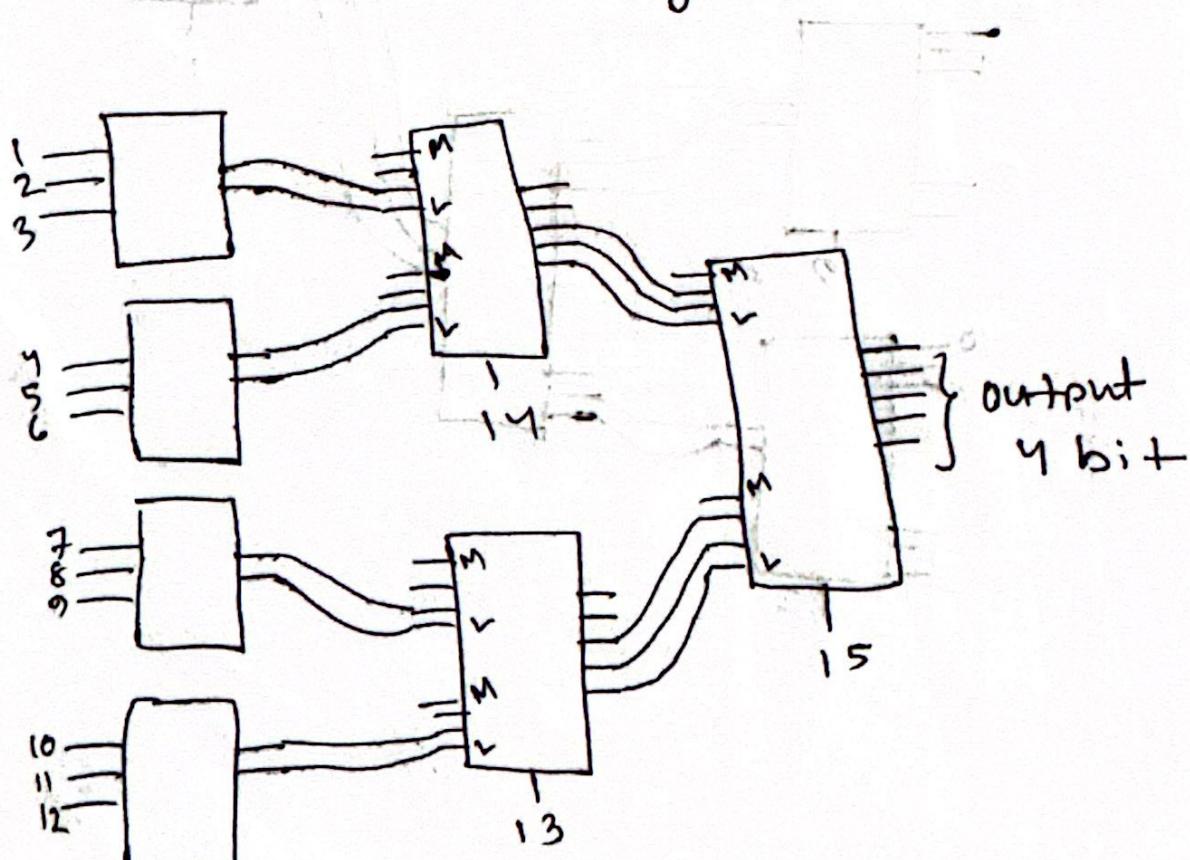
(3)



Build a 8 person voting system using full and parallel adder.



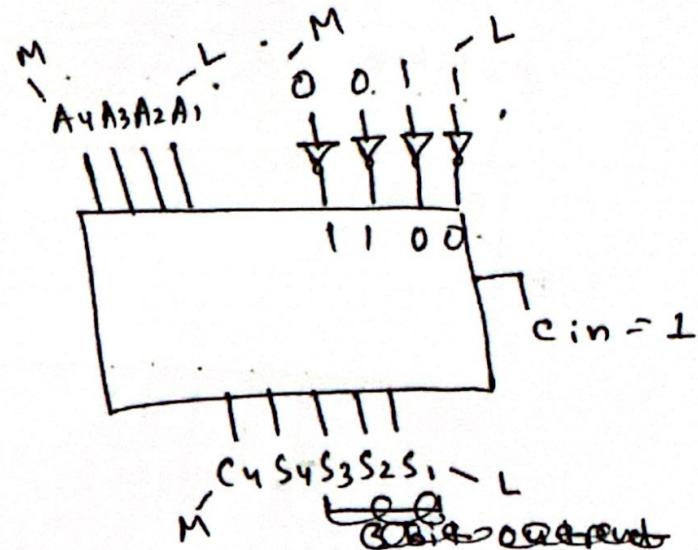
Build a 15 person voting system



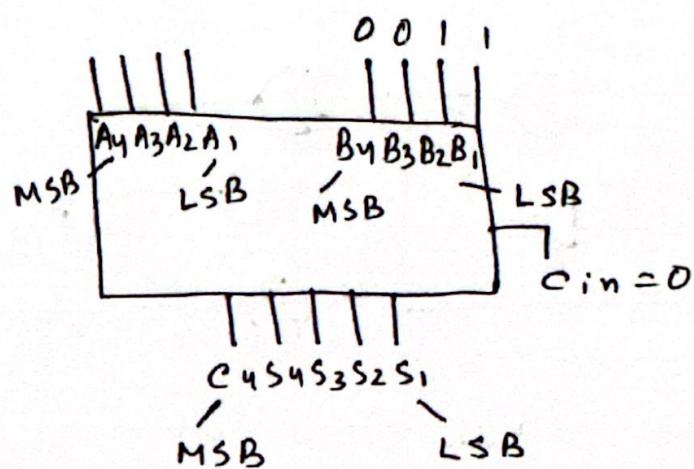
(A)  $A \rightarrow 1$  bit

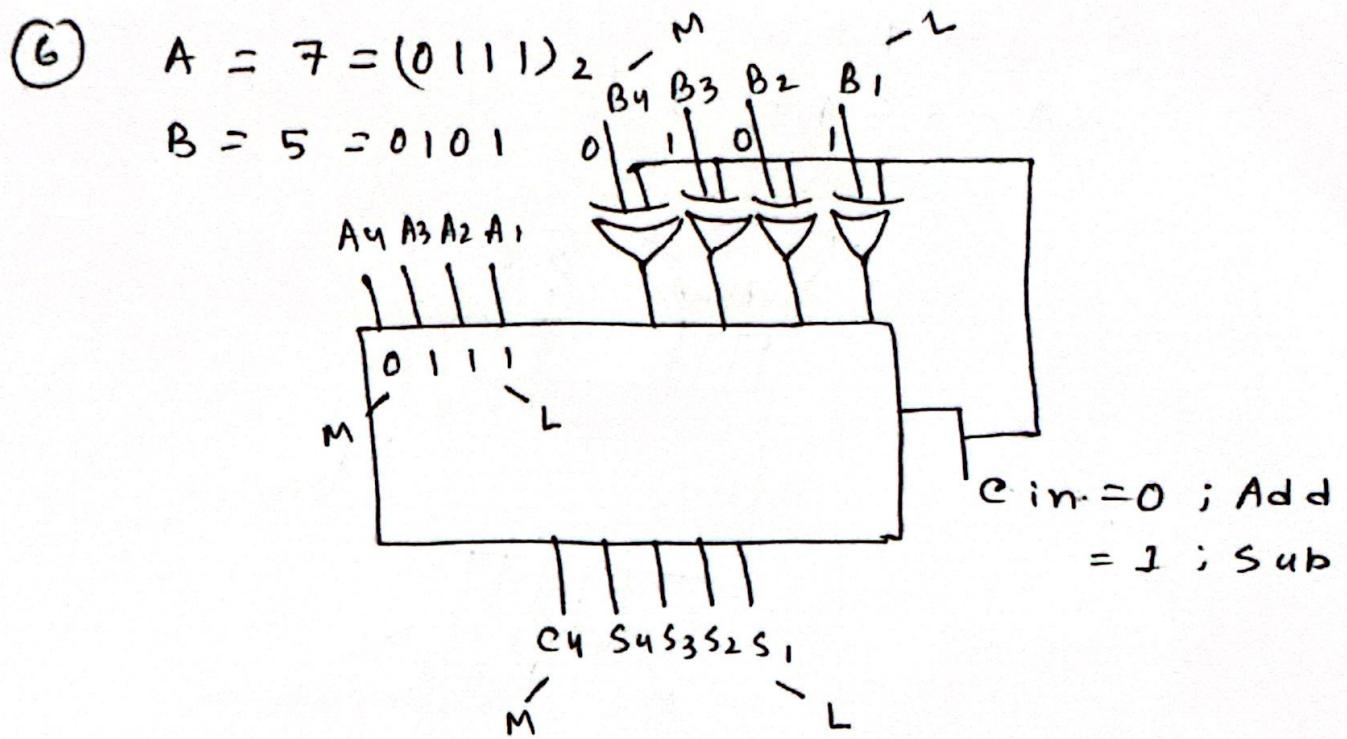
$$A - 3 = A + (-3)$$

$$\begin{array}{r} 3 \\ \downarrow \\ \begin{array}{r} 0011 \\ 1100 \\ +1 \\ \hline \end{array} \end{array}$$

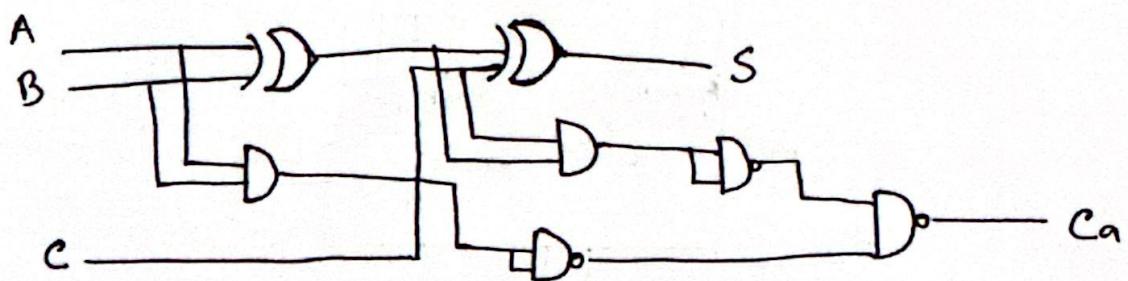


(5)

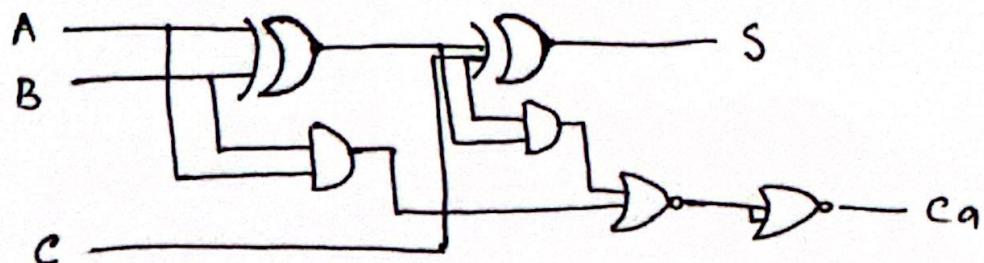




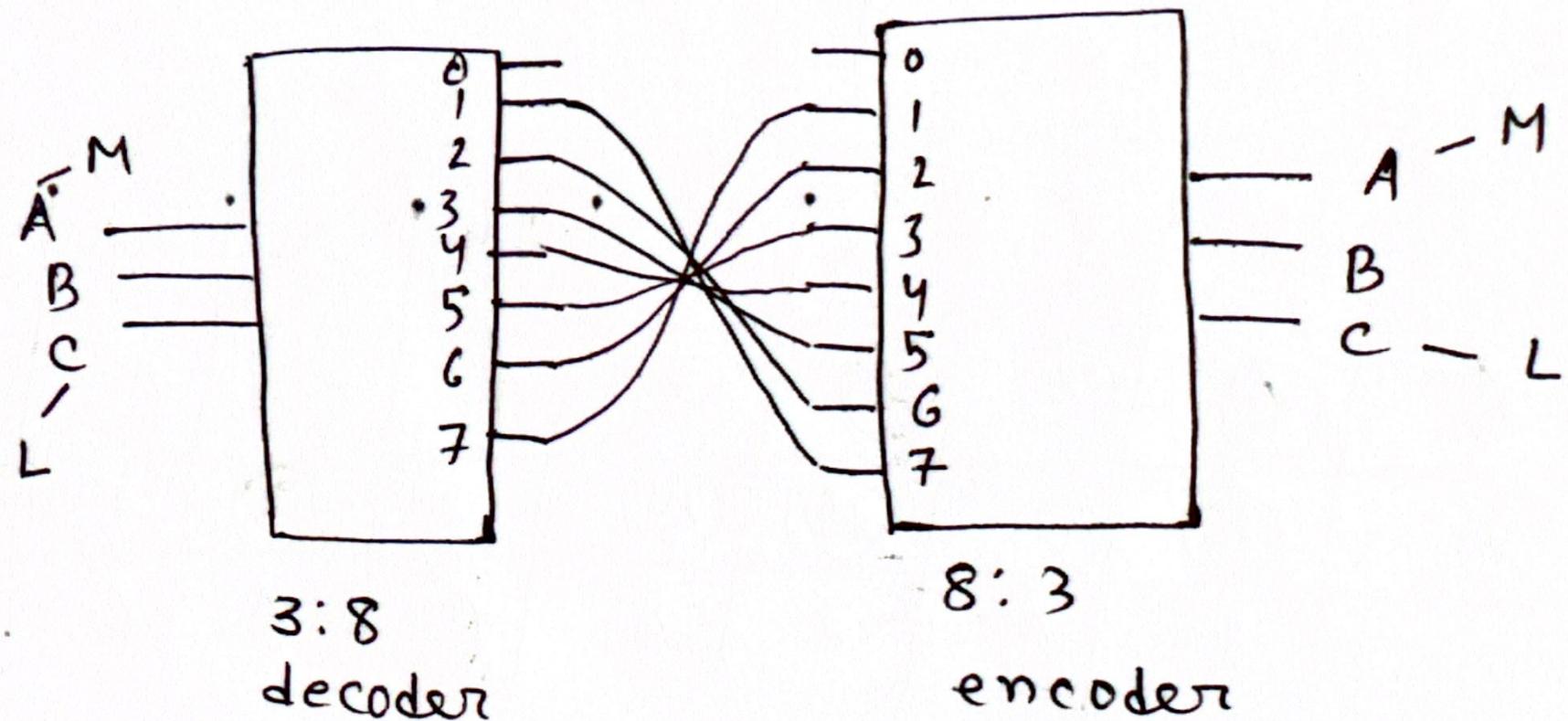
(7) Using 3 NAND gate and no OR gates



Using 2 NOR gates and no OR gates



⑨



# Example: Octal-binary encoder

**TABLE 5-3**  
**Truth Table of Octal-to-Binary Encoder**

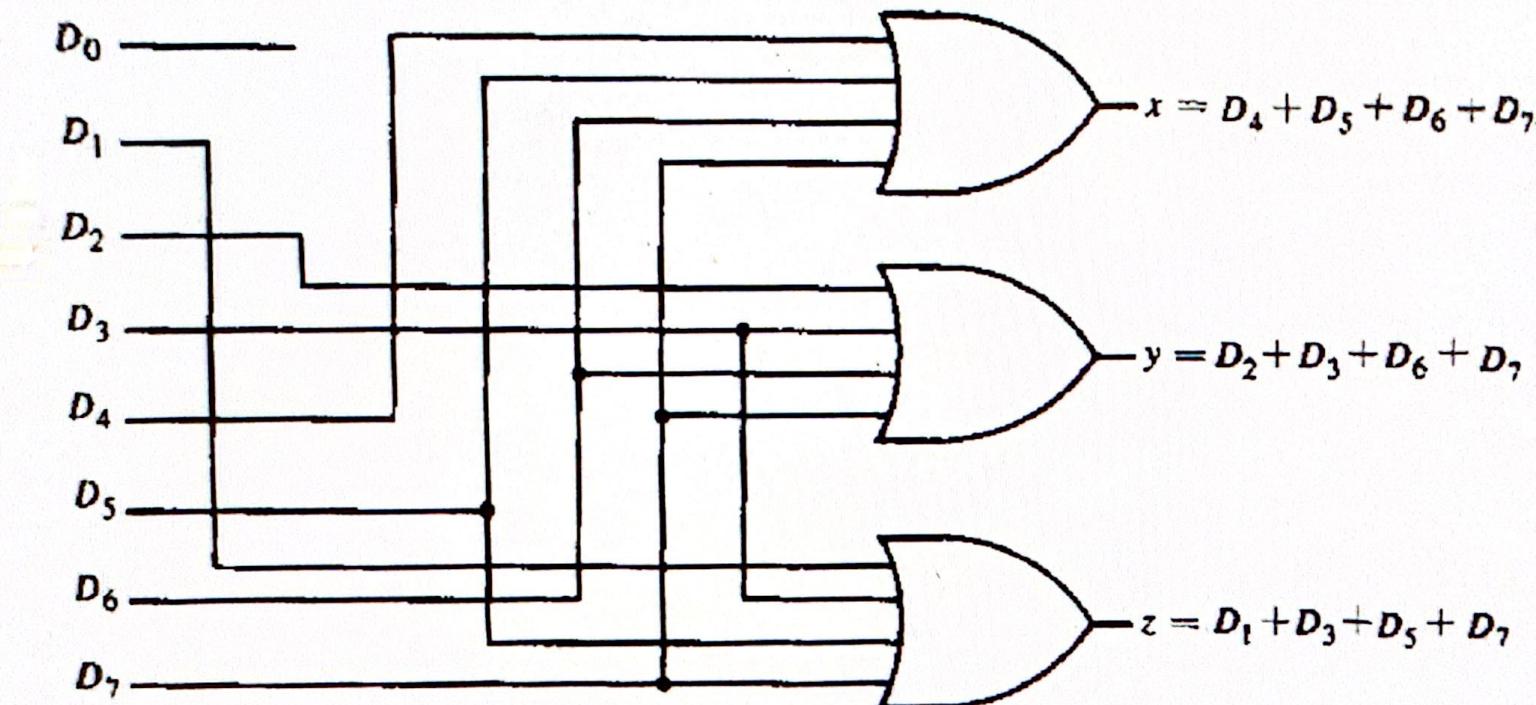
Inputs								Outputs		
$D_0$	$D_1$	$D_2$	$D_3$	$D_4$	$D_5$	$D_6$	$D_7$	$x$	$y$	$z$
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

$$z = D_1 + D_3 + D_5 + D_7$$

$$y = D_2 + D_3 + D_6 + D_7$$

$$x = D_4 + D_5 + D_6 + D_7$$

# Example: Octal-binary encoder



**FIGURE 5-13**

Octal-to-binary encoder

There are 8 input variables so there will  $2^8$  input combination, amongst which in Octal-binary encoder only 8 are useful

Design a  $1 \times 2$  priority encoder prioritizing MSB.

$I_3$	$I_2$	$I_1$	$I_0$	A	B
0	0	0	0	X	X
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

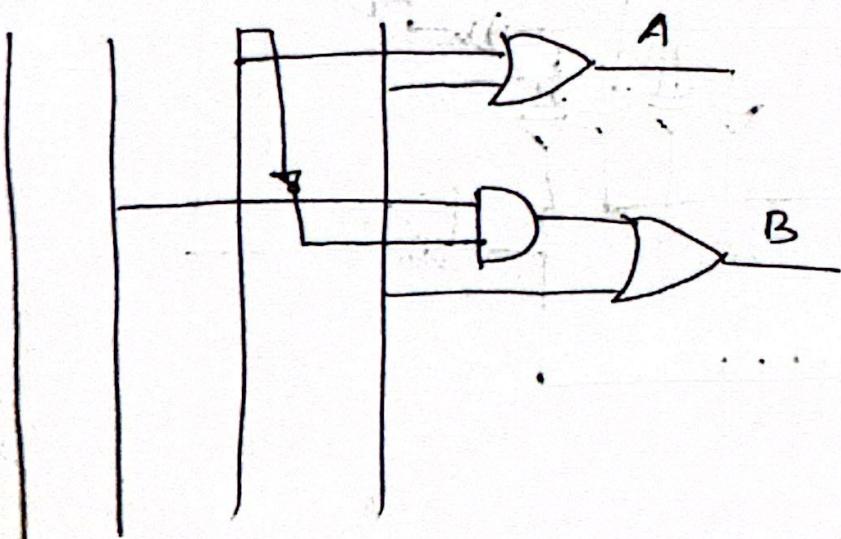
$\bar{I}_3\bar{I}_2$	$\bar{I}_3I_2$	$\bar{I}_3I_1$	$\bar{I}_3I_0$	$I_3\bar{I}_2$	$I_3I_1$
0	1	3	2		
1	1	1	1		
1	1	1	1		
1	1	1	1		

$$A = I_2 + I_3$$

		1	1
1	1	1	1

$$B = I_3 + I_1, \bar{I}_2$$

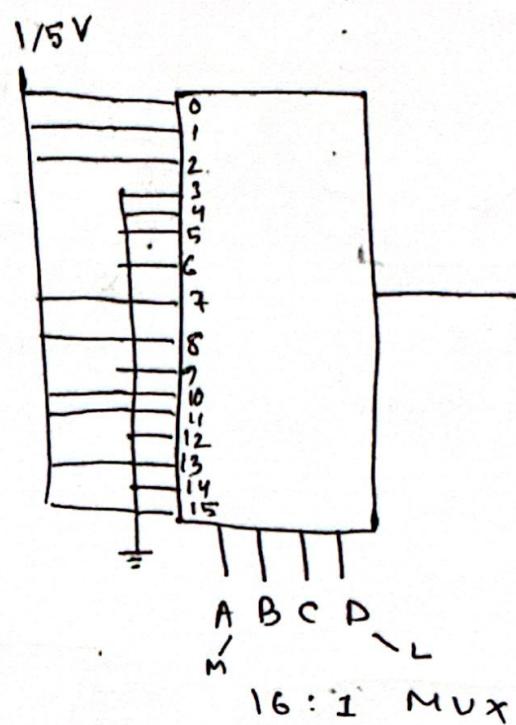
$I_0 \quad I_1 \quad I_2 \quad I_3$



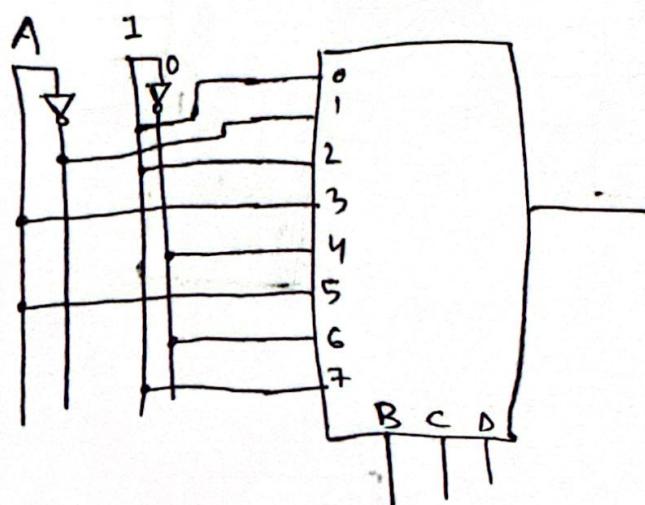
- Implement the following boolean function using a single 16:1 mux .  
 $F(A,B,C,D) = \sum(0,1,2,7,8,10,11,13, 15)$ . Use external gates if required.
- Implement the following boolean function using a single 8:1 mux.  
 $F(A,B,C,D) = \sum(0,1,2,7,8,10,11,13, 15)$ . Use external gates if required.
- Implement the following boolean function using a single 4:1 mux.  
 $F(A,B,C,D) = \sum(0,1,2,7,8,10,11,13, 15)$ . Use external gates if required.
- Implement the following boolean function using both 4:1 and 2:1 mux in a single circuit  
 $F(A,B,C,D) = \sum(0,1,2,7,8,10,11,13, 15)$ . Use external gates if required.
- Implement the following boolean function using **a**) 4x16 decoder(s) only **b**) 2x4 decoder(s) only  
 $F(A,B,C,D,E) = \sum(0,1,2,7,8,10,11,13, 15,18,21,24,25)$ . Use external gates if required.
- Build a full adder using encoder(s) and decoder(s).
- Build a BCD to Excess-3 code converter using encoder(s) and decoder(s).
- Build a BCD to Excess-5 code converter using encoder(s) and decoder(s).
- Design the circuit diagram for a 3x8 decoder.
- Design the circuit diagram for a 2x4 decoder.
- Design the circuit diagram for a 4:1 mux.
- Design a 8:1 mux using both 4:1 mux and 2:1 mux in a single circuit.
- Design AND, OR, NOT gate using 4:1 mux.
- Design AND, OR, NOT gate using 2:1 mux.
- Design a circuit that can demonstrate the usage of ENABLE pin in decoders.

(10)

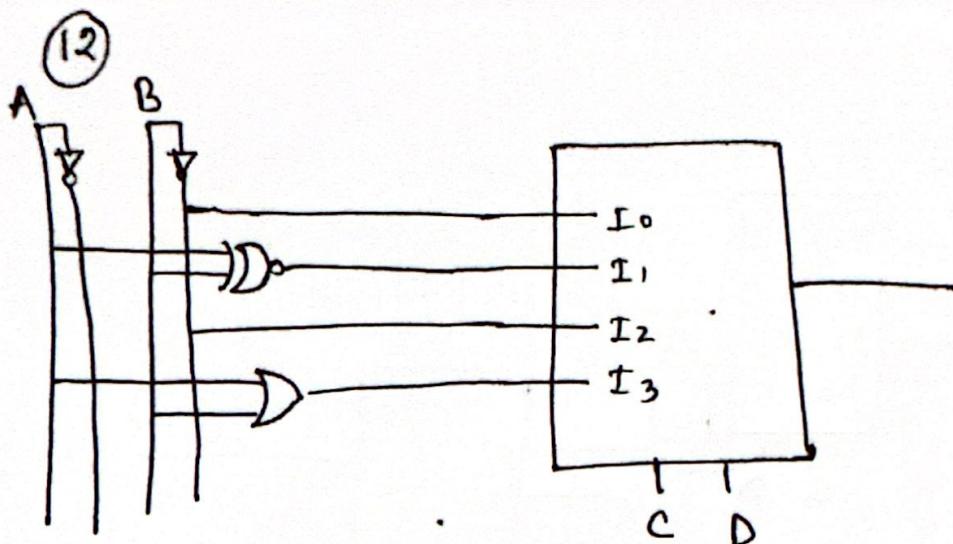
$$F(A, B, C, D) = \Sigma(0, 1, 2, 7, 8, 10, 11, 13, 15)$$



(11)



	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
$A'$	0	1	2	3	4	5	6	7
$A$	8	9	10	11	12	13	14	15
	1	$A'$	1	A	0	A	0	1



	I <sub>0</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>
A'B'	0	1	2	3
A'B	4	5	6	7
AB'	8	9	10	11
AB	12	13	14	15
	B'	A ⊕ B	B'	A + B

I<sub>0</sub> ⇒

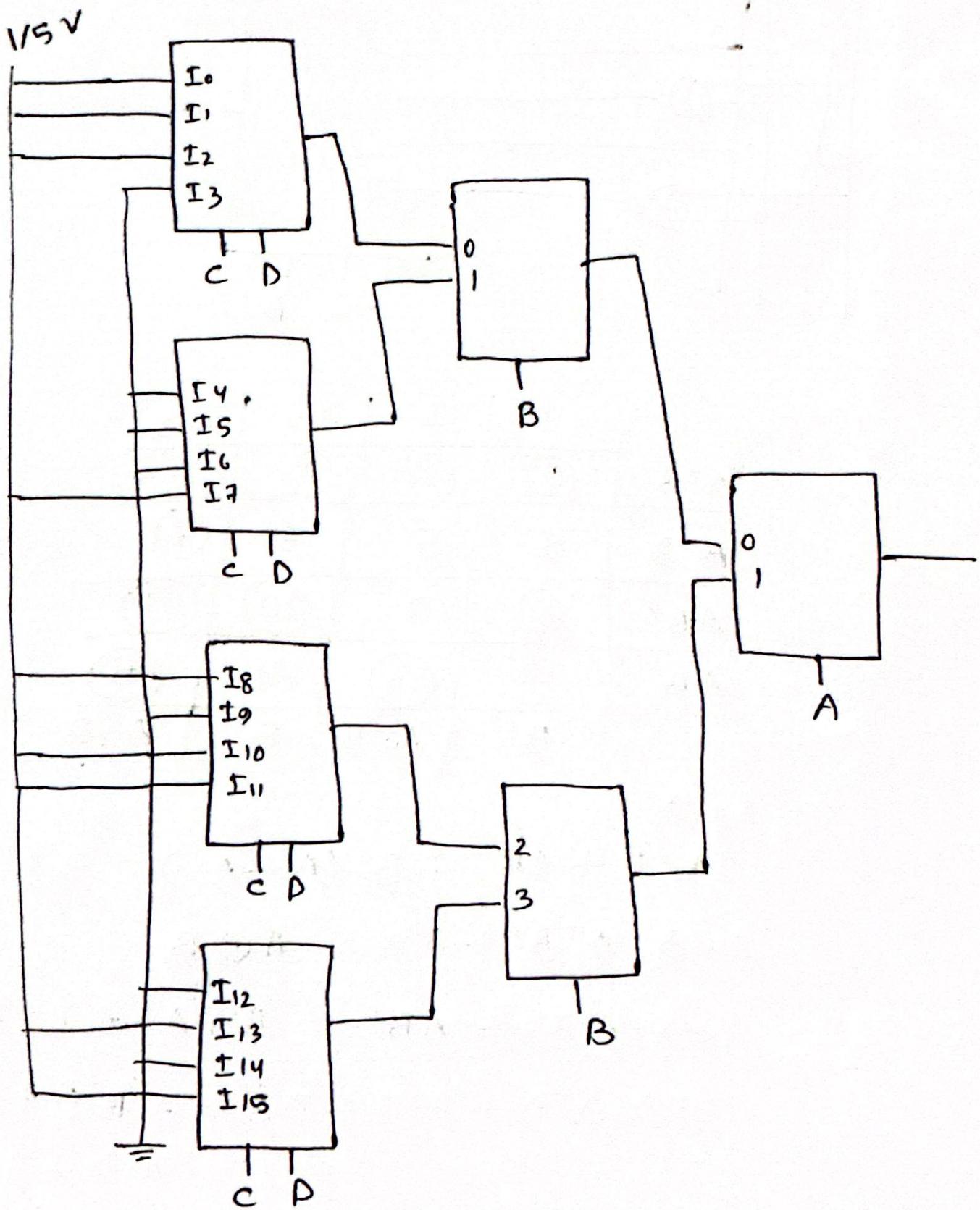
$$A'B' + AB' = B'(A + A') = B'$$

$$I_1 \Rightarrow A'B' + AB = A \oplus B$$

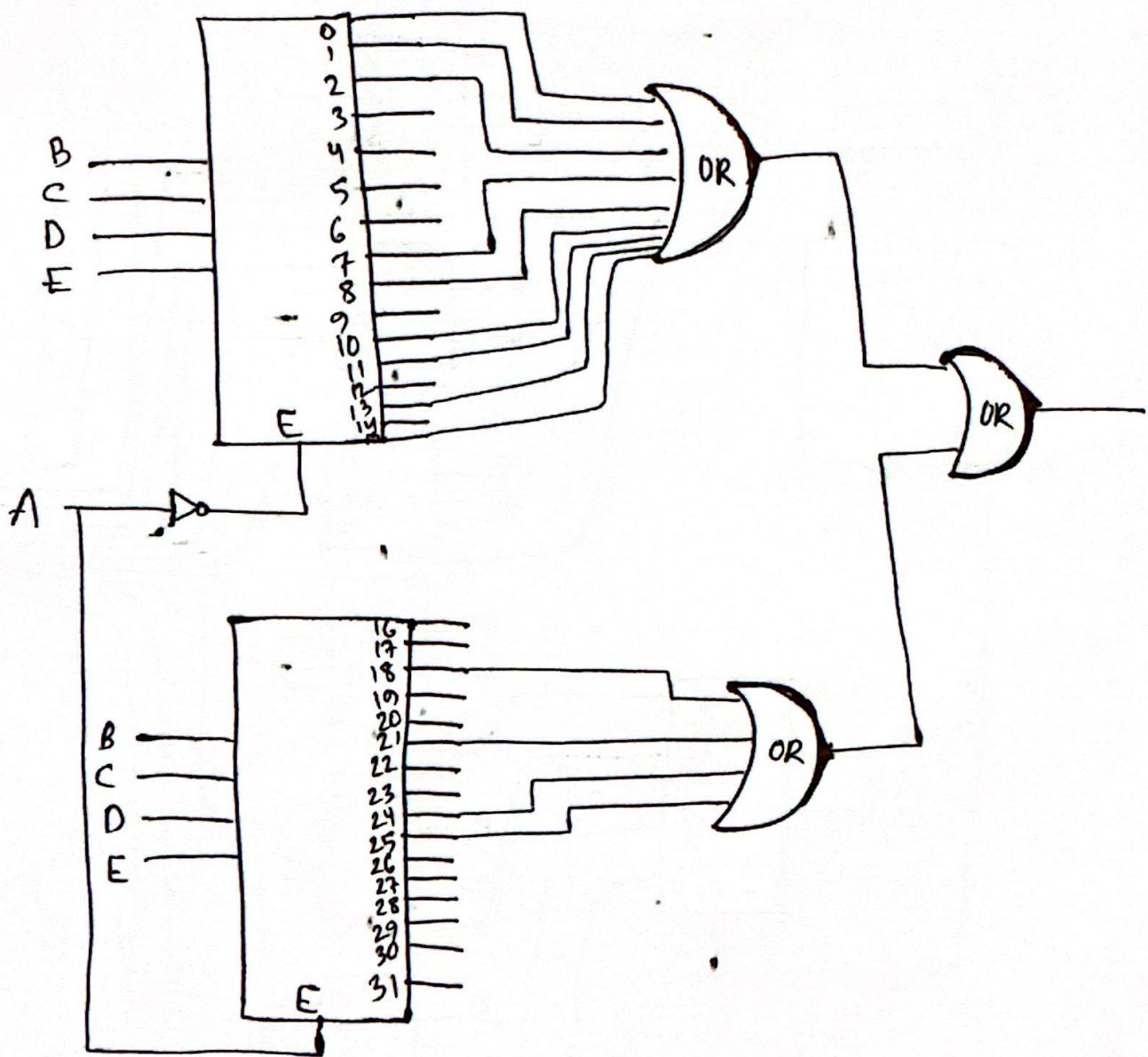
$$I_2 \Rightarrow A'B' + AB' = B'(A+A') = B'$$

$$\begin{aligned}
 I_3 \Rightarrow A'B + AB' + AB &= A'B + A(B+B') \\
 &= A'B + A \\
 &= (A'+A)(B+A) \\
 &= A + B
 \end{aligned}$$

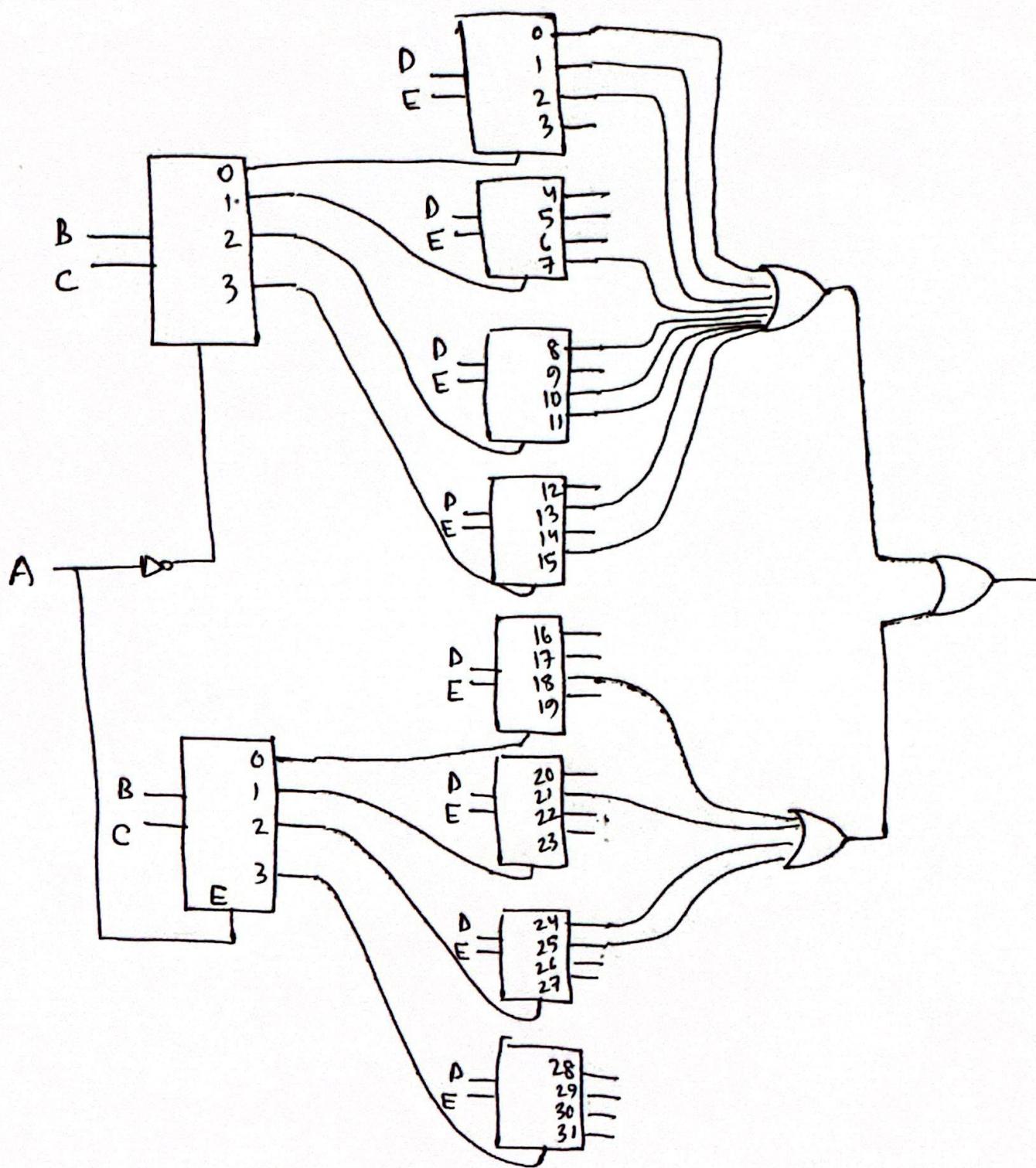
(13)



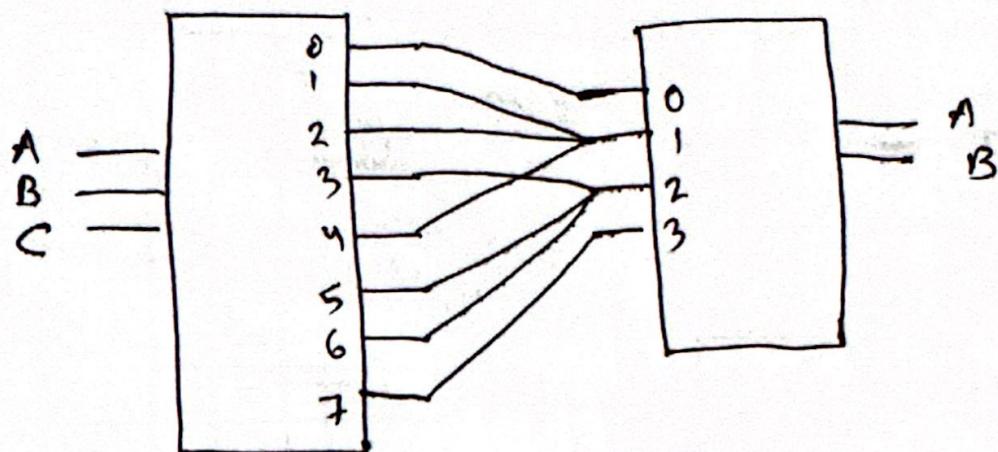
(H) a)



b)

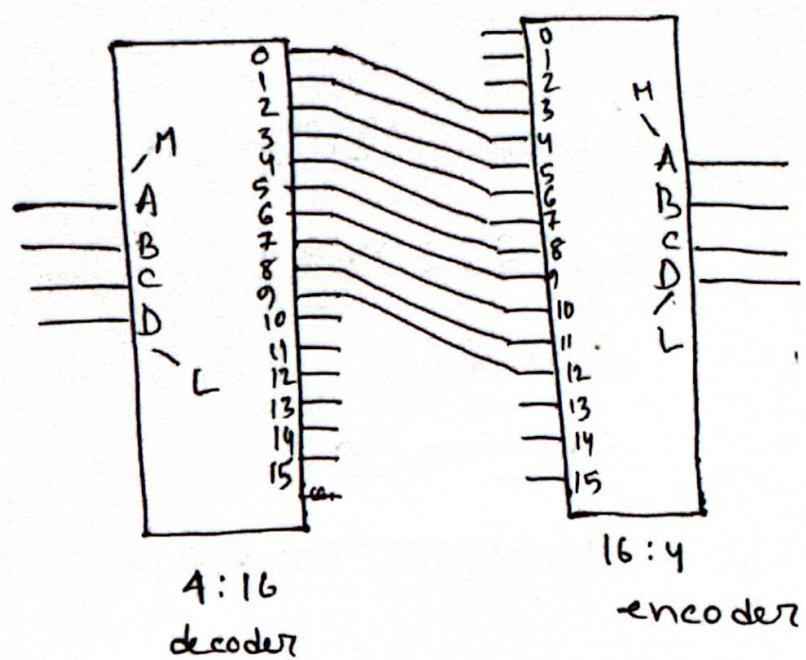


7 Design a full adder using encoder and decoder.

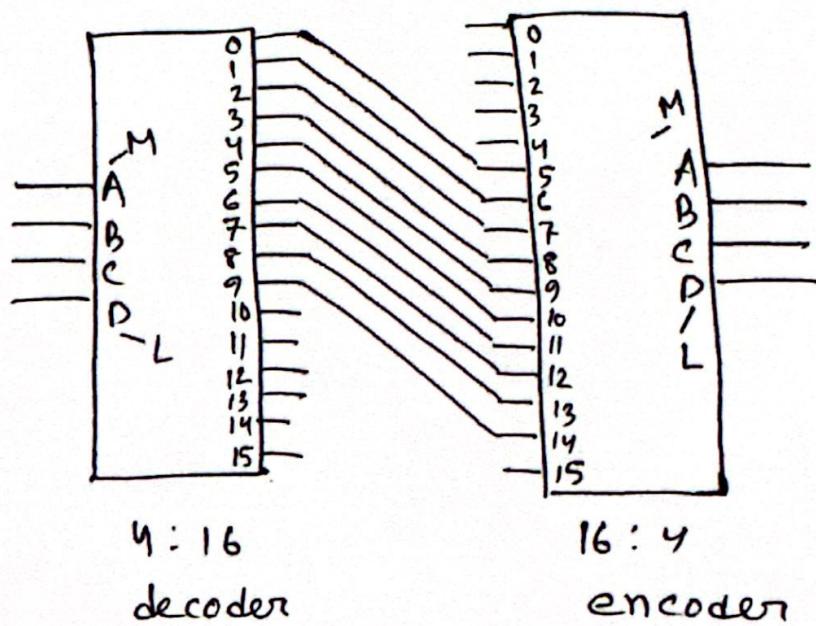


A	B	c	ca	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(15)



(16)



\* Design the circuit diagram for a  
3x8 decoder.

M	A	B	C	0 <sub>0</sub>	0 <sub>1</sub>	0 <sub>2</sub>	0 <sub>3</sub>	0 <sub>4</sub>	0 <sub>5</sub>	0 <sub>6</sub>	0 <sub>7</sub>
0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
2	0	1	0	0	0	1	0	0	0	0	0
3	0	1	1	0	0	0	1	0	0	0	0
4	1	0	0	0	0	0	0	1	0	0	0
5	1	0	1	0	0	0	0	0	0	1	0
6	1	1	0	0	0	0	0	0	0	0	1
7	1	1	1	0	0	0	0	0	0	0	1

$$O_0 = A'B'C'$$

$$O_1 = A'B'C$$

$$O_2 = A'BC'$$

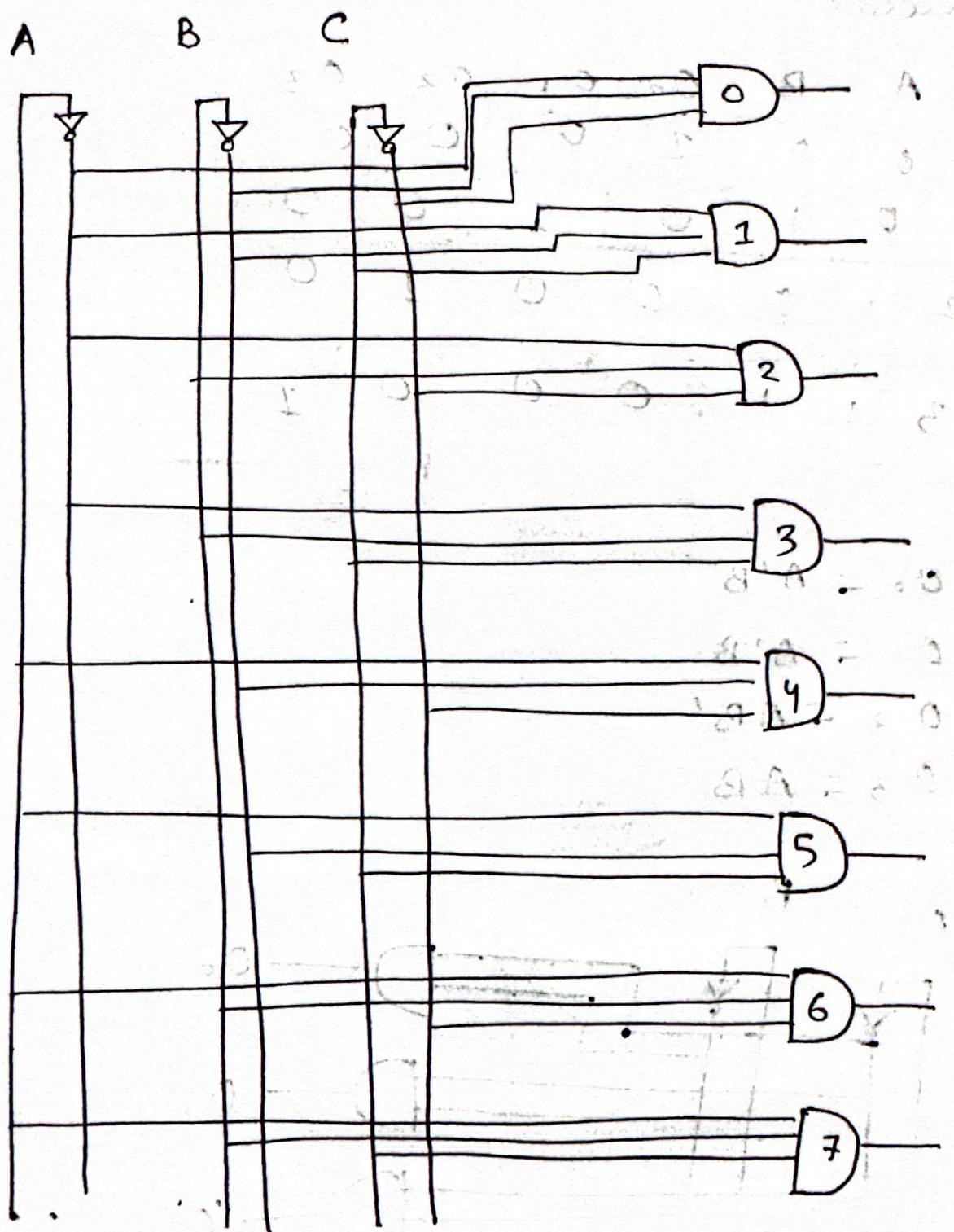
$$O_3 = A'BC$$

$$O_4 = AB'C'$$

$$O_5 = AB'C$$

$$O_6 = ABC'$$

$$O_7 = ABC$$



Design the circuit diagram for a  $2 \times 4$  decoder.

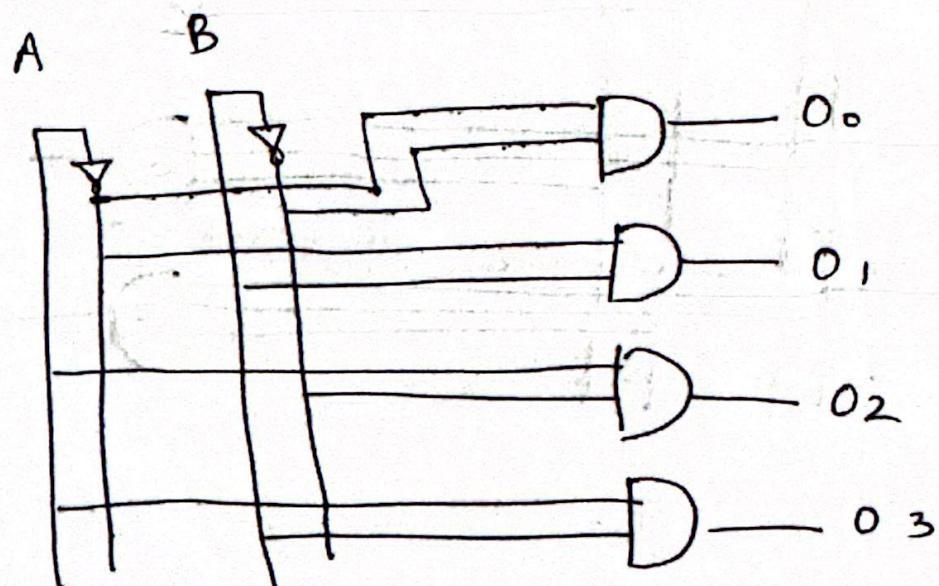
A	B	0 <sub>0</sub>	0 <sub>1</sub>	0 <sub>2</sub>	0 <sub>3</sub>
0	0	1	0	0	0
1	0	0	1	0	0
2	1	0	0	0	1
3	1	1	0	0	0

$$0_0 = A'B'$$

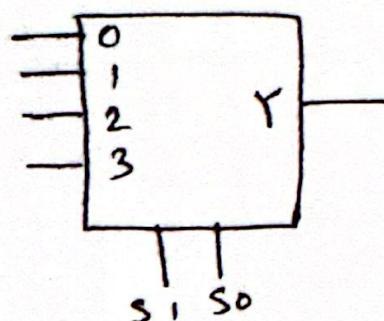
$$0_1 = A'B$$

$$0_2 = AB'$$

$$0_3 = AB$$

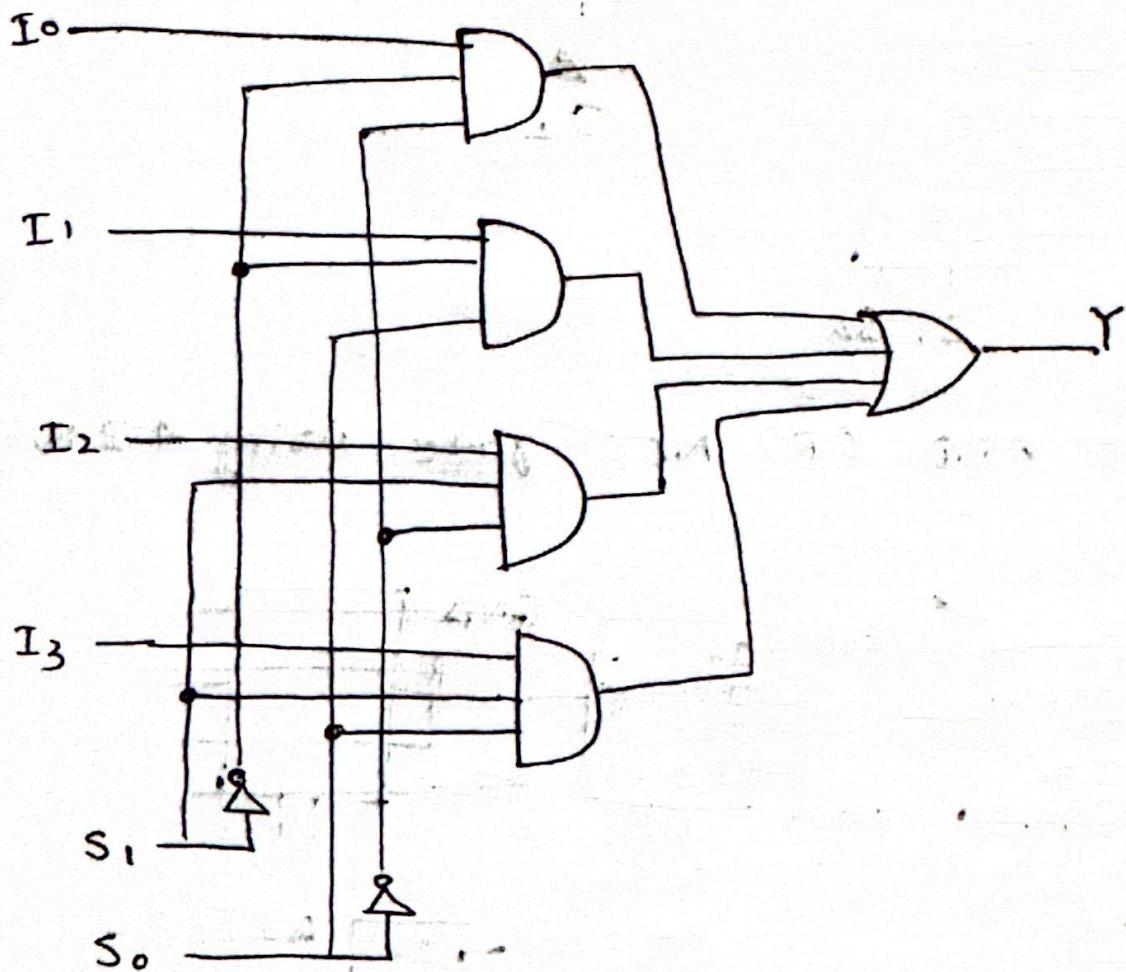


Design the circuit diagram for a 4:1 mux

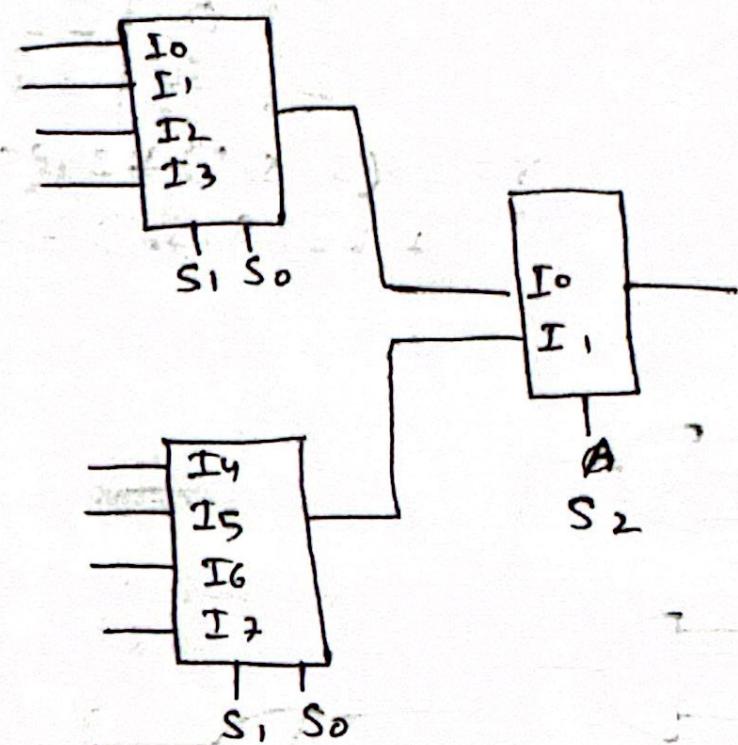


$S_1$	$S_0$	$Y$
0	0	$I_0$
0	1	$I_1$
1	0	$I_2$
1	1	$I_3$

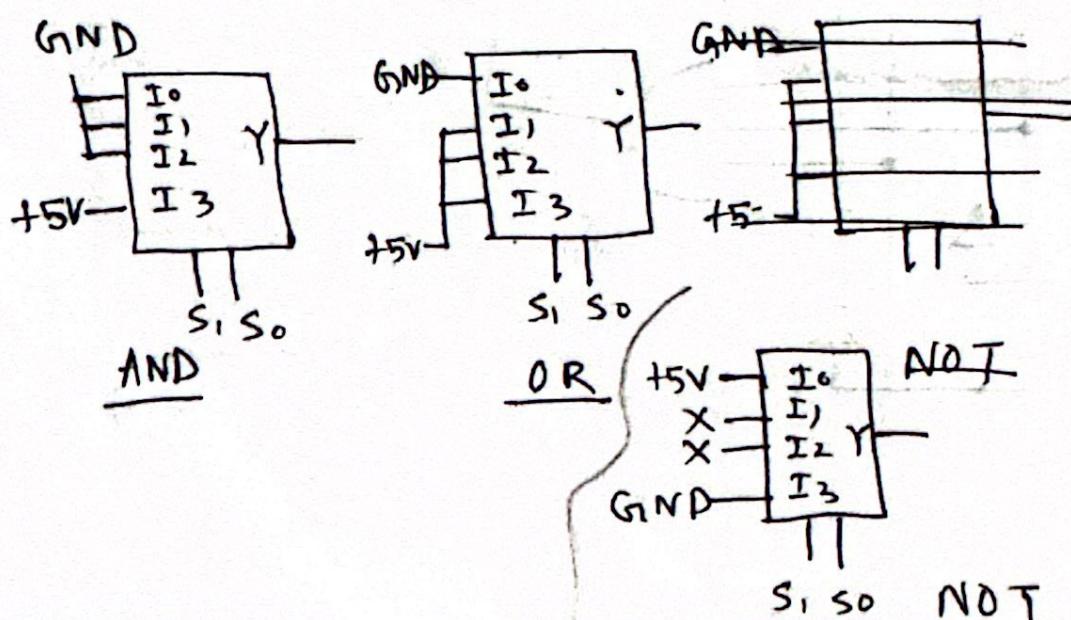
$$Y = I_0(S_1'S_0') + I_1(S_1'S_0) + I_2(S_1S_0') + I_3(S_1S_0)$$



Design 8:1 mux using both 1:1 mux and 2:1 mux in a single circuit.

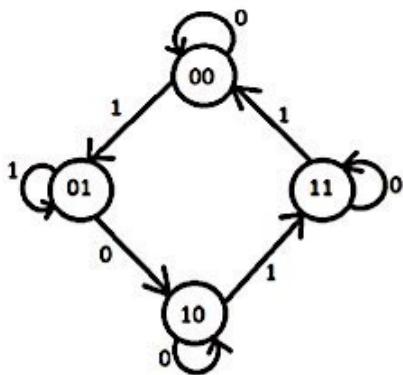


Design AND, OR, NOT gate using 4:1 mux



- Design a D FF using SR FF.
- Design a T FF using JK FF.
- Design a D FF using JK FF.
- Design a SR FF.
- Write down the excitation table for SR, D, JK and T FF.
- Write down the characteristics table for SR, D, JK and T FF.

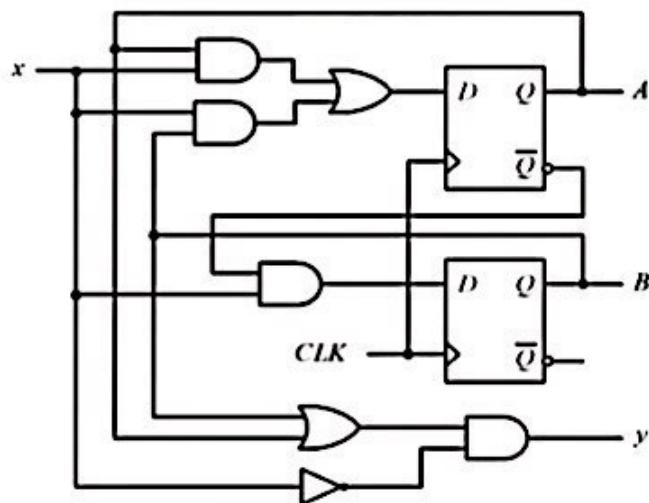
- Given the state diagram as follows, get the sequential circuit using SR flipflop.



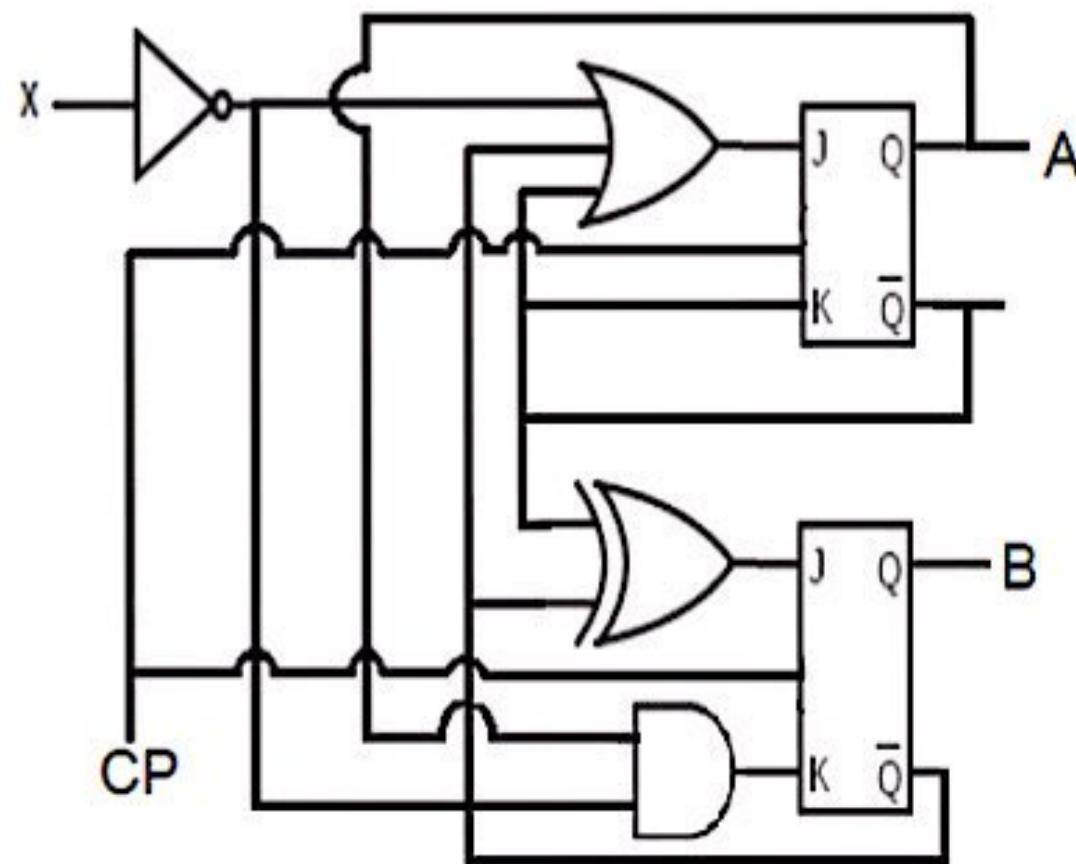
- Implement the following counter using T flip flop  
CSE110 -> CSE111 -> CSE220 -> CSE221 -> CSE331 -> CSE221 -> CSE321 -> CSE110
- 3->4->6->10->12->13->15->3
  - Implement the given counter using JK flip-flop.
  - Implement the given counter using T flip-flop.

NB: For states not given in question, please move to the initial state as per question.

- Implement 4 bit up counter using JK flip flop
- Implement 4 bit down counter using JK flip flop
- Implement 2 bit up/down counter using D flip flop
- Implement 3 bit up/down counter using T flip flop
- Implement 2 bit up/down counter using SR flip flop
- Implement 3 bit up/down counter using JK flip flop
- Implement the following counter using T FF:  
Green->Orange->Yellow->Red->Yellow->Orange->Yellow->Green
- Implement the following counter using JK FF: Green->Yellow->Red->Yellow->Green
- Implement the following counter using JK FF: 1->2->3->5->7->11->13->1
- Implement the following counter using SR FF: 2->3->6->8->10->12->2
- Draw the state diagram for the given circuit.



- Draw the state diagram for the given circuit.

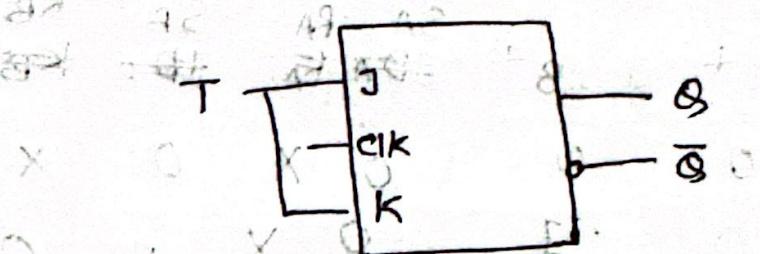


## Assignment 1

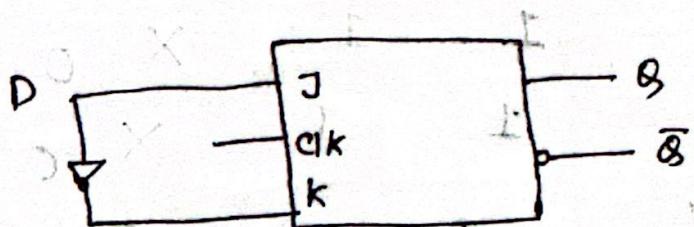
1. Design a D FF using SR FF



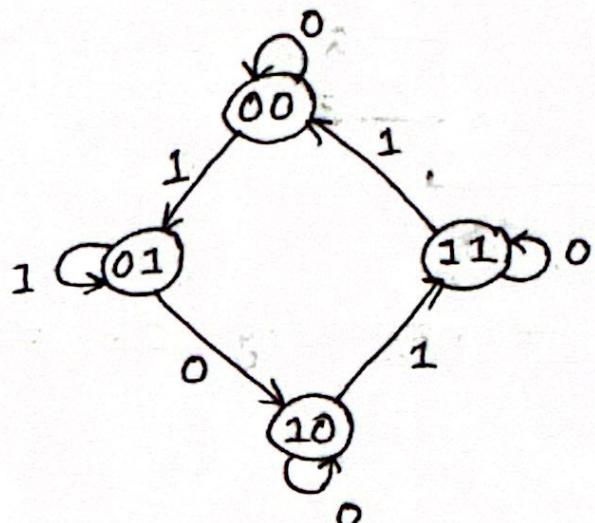
2. Design a T FF using JK FF.



3. Design a D FF using JK FF



④ Given the state diagram as follows, get the sequential circuit using SR flipflop.



A	B	$\alpha$	$A^+$	$B^+$	<del>SA</del>	<del>RA</del>	<del>SB</del>	<del>RB</del>
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	0
0	1	0	1	0	1	0	0	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	0
1	1	0	1	1	X	0	X	0
1	1	1	0	0	0	1	0	1

## SR flip-flop excitation table

$S(t)$	$S(t+1)$	$S$	$R$
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

$$S_A = \Sigma (2, 7, 4, 5, 6)$$

$$R_A = \Sigma (0, 1, 3, 7)$$

$$S_B = \Sigma (1, 3, 5, 6)$$

$$R_B = \Sigma (1, 3, 5, 8)$$

	$\bar{B}X$	$B\bar{X}$	$BX$	$B\bar{X}$
$\bar{A}$	0	1	3	2
A	X <sub>4</sub>	X <sub>5</sub>	X <sub>7</sub>	X <sub>6</sub>

$$S_A = B\bar{X}$$

	$\bar{B}X$	$B\bar{X}$	$BX$	$B\bar{X}$
$\bar{A}$	X <sub>0</sub>	X <sub>1</sub>	X <sub>3</sub>	X <sub>2</sub>
A	X <sub>4</sub>	X <sub>5</sub>	X <sub>7</sub>	X <sub>6</sub>

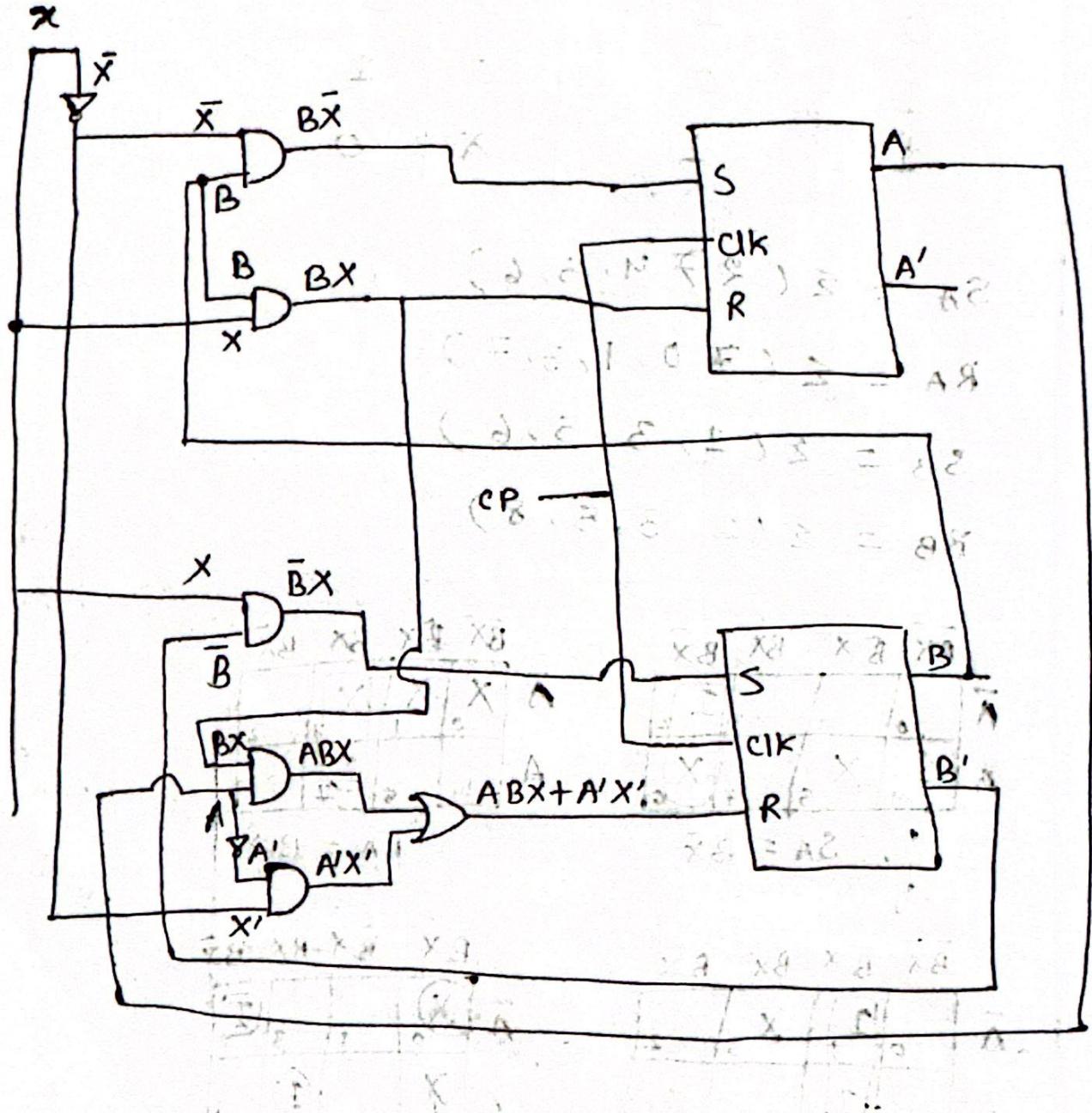
$$R_A = B\bar{X}$$

	$\bar{B}X$	$B\bar{X}$	$BX$	$B\bar{X}$
$\bar{A}$	0	1	X <sub>3</sub>	X <sub>2</sub>
A	X <sub>4</sub>	X <sub>5</sub>	X <sub>7</sub>	X <sub>6</sub>

$$S_B = \bar{B}X$$

	$\bar{B}X$	$B\bar{X}$	$BX$	$B\bar{X}$
$\bar{A}$	X <sub>0</sub>	1	3	2
A	X <sub>4</sub>	5	1	6

$$R_B = ABX + \bar{A}\bar{B}\bar{X}$$



8

CSE 110 → 000

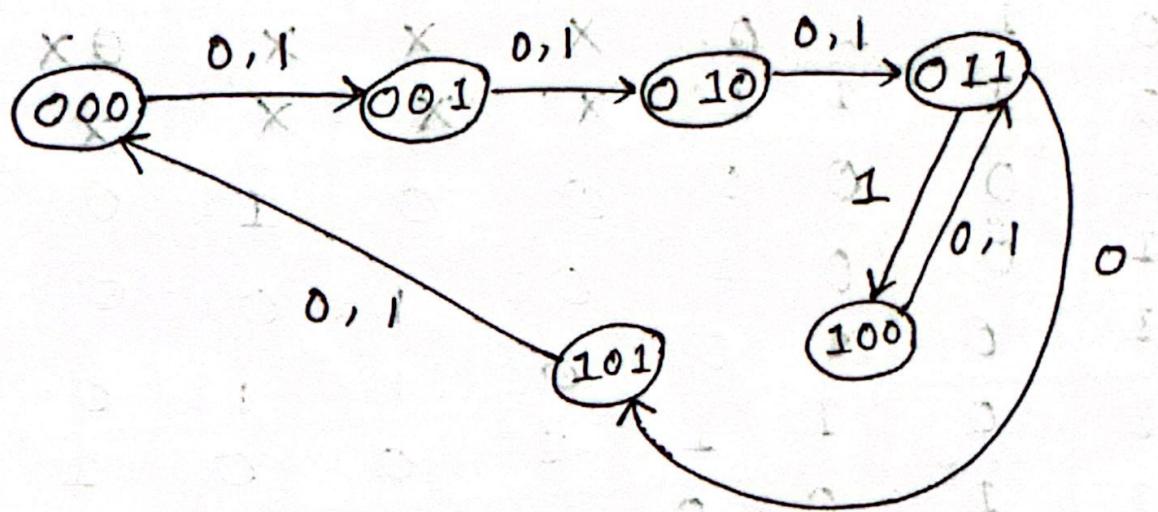
CSE 111 → 001

CSE 220 → 010

CSE 221 → 011

CSE 331 → 100

CSE 321 → 101



$x$	A	B	C	$A^+$	$B^+$	$C^+$	$T_A$	$T_B$	$T_C$
0 0	0 0	0 0	0 0	0 0	0 1	0 1	0 0	0 0	1 1
0 0	0 0	0 1	0 0	1 0	1 0	0 0	0 0	1 1	1 1
0 0	1 0	0 0	0 0	1 1	1 1	0 0	0 0	1 1	1 1
0 0	1 1	1 1	1 1	0 0	1 1	1 1	1 1	1 1	0 0
0 1	0 0	0 0	0 0	0 0	1 1	1 1	1 1	1 1	1 1
0 1	0 1	0 0	0 0	0 0	0 0	1 1	0 1	0 0	1 1
0 1	1 0	0 0	X 0	X 0	X 0	0 X	X X	X X	X X
0 1	1 1	1 0	X 0	X 0	X 0	X 0	X X	X X	X X
1 0	0 0	0 0	0 0	0 0	1 1	0 0	0 0	0 0	1 1
1 0	0 0	1 0	0 0	1 0	1 0	0 0	1 1	1 1	1 1
1 0	0 1	0 0	0 0	0 0	1 1	1 1	0 0	0 0	1 1
1 0	1 1	1 1	1 1	1 0	0 0	1 1	1 1	1 1	1 1
1 1	0 0	0 0	0 0	0 0	1 1	1 1	1 1	1 1	1 1
1 1	0 1	1 0	0 0	0 0	0 0	0 0	1 0	1 0	1 1
1 1	1 1	1 0	X 0	X 0	X 0	X X	X X	X X	X X
1 1	1 1	1 1	X 0	X 0	X 0	X X	X X	X X	X X

$$T_A = \{3, 4, 5, 11, 12, 13\}$$

$$T_B = \{1, 3, 4, 9, 11, 12\}$$

$$T_C = \{0, 1, 2, 4, 5, 8, 9, 10, 11, 12, 13\}$$

$\bar{x}A$	$BC$	$B'C'$	$B'C$	$BC$	$BC'$	
$x'A'$	0	1	1	2		
$x'A$	1	4	1	5	$x_7$	$x_6$
$\bar{x}A$	1	12	1	13	$x_{15}$	$x_{14}$
$x'A'$	8	9	1	11	10	

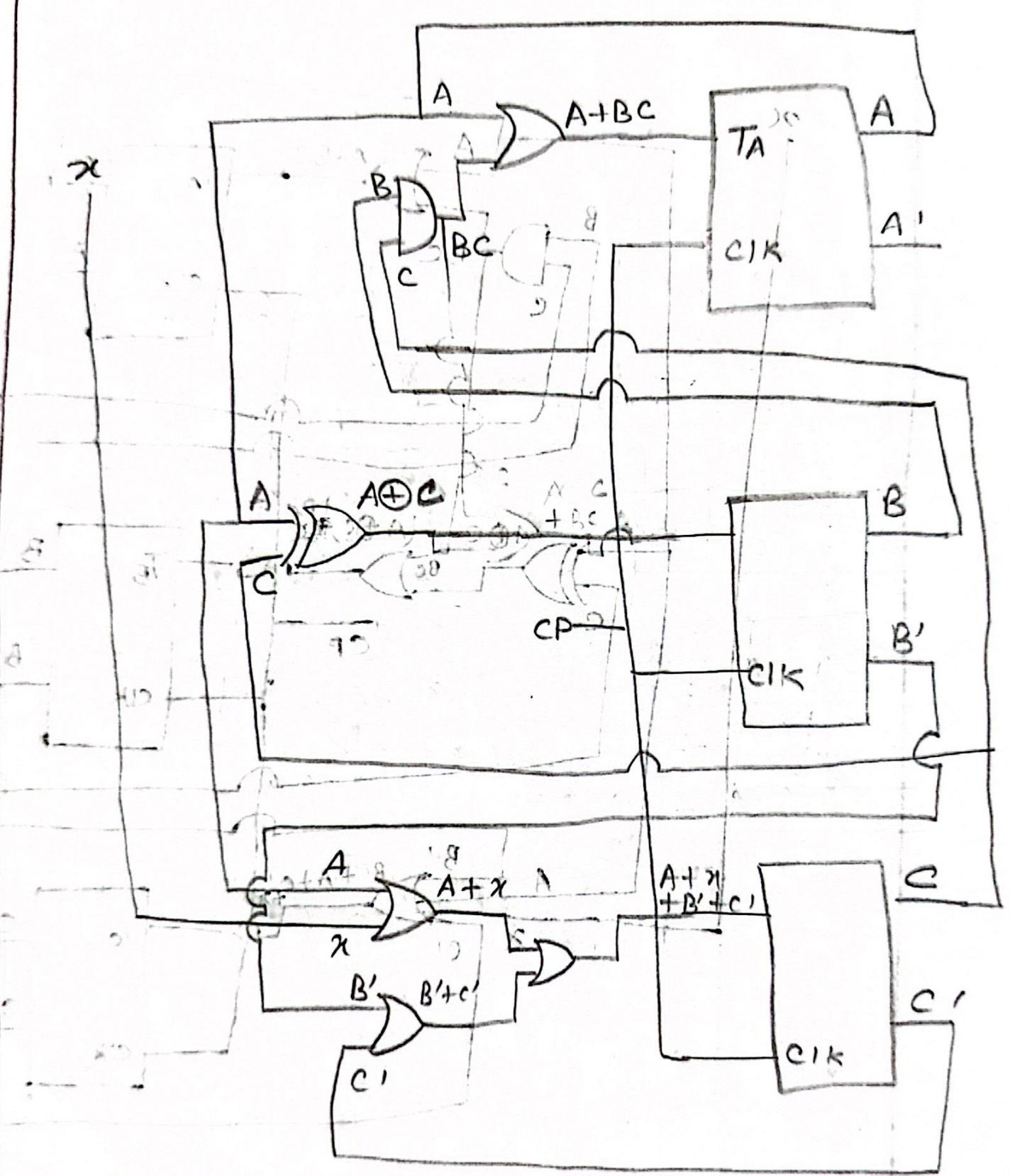
$$T_A = A + BC$$

$\bar{x}A$	$BC$	$B'C'$	$B'C$	$BC$	$B,C'$	
$x'A'$	0	1	1	3	2	
$x'A$	1	4	1	5	$x_7$	$x_6$
$\bar{x}A$	1	12	1	13	$x_{15}$	$x_{14}$
$x'A'$	8	1	9	1	11	10

$$\begin{aligned} T_B &= A'C + BC \\ &\quad + AC' \\ &= (A \oplus C) + BC \end{aligned}$$

$\bar{x}A$	$BC$	$B'C'$	$B'C$	$BC$	$B,C'$	
$x'A'$	1	1	3	2		
$x'A$	1	4	1	5	$x_7$	$x_6$
$\bar{x}A$	1	12	1	13	$x_{15}$	$x_{14}$
$x'A'$	8	1	9	1	11	10

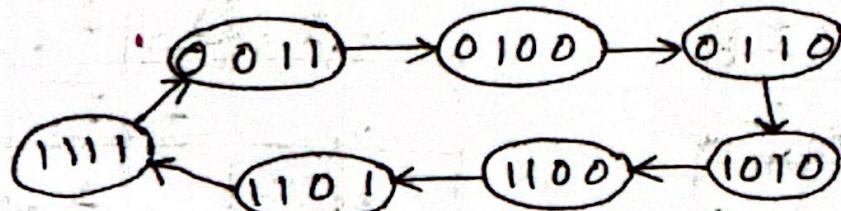
$$\begin{aligned} T_C &= B' + A \\ &\quad + C' + x \end{aligned}$$



⑨.  $3 \rightarrow 4 \rightarrow 6 \rightarrow 10 \rightarrow 12 \rightarrow 13 \rightarrow 15 \rightarrow 3$

$\downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow$

0011 0100 0110 1010 1100 1101 1111 0011



$A_3$	$A_2$	$A_1$	$A_0$	$A_3^+$	$A_2^+$	$A_1^+$	$A_0^+$	$T_{A_3}$	$T_{A_2}$	$T_{A_1}$	$T_{A_0}$
0	0	0	0	0	0	1	1	0	0	1	1
0	0	0	1	0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	1	0	0	0	1	0
0	1	0	1	0	0	1	1	0	1	1	0
0	1	1	0	1	0	1	0	1	1	0	0
0	1	1	1	0	0	1	1	0	1	0	0
1	0	0	0	0	0	1	1	1	0	1	1
1	0	0	1	0	0	1	1	1	0	1	0
1	0	1	0	1	1	0	0	0	1	1	0
1	0	1	1	0	0	1	1	1	0	0	0
1	1	0	0	1	1	0	1	0	0	0	1
1	1	0	1	1	1	1	1	0	0	1	0
1	1	1	0	0	0	1	1	1	1	0	1
1	1	1	1	1	0	1	1	1	1	0	0

$A_3 A_2$	$A_1 A_0$	$\bar{A}_3 \bar{A}_2$	$\bar{A}_1 \bar{A}_0$	$A_1 \bar{A}_0$	$A_1 A_0$
0	1	3	10	2	
4	5	7	11	6	
8	13	15	14	1	
18	9	11	10		

$$T_{A_3} = A_3 \bar{A}_2 + A_1 A_0 + A_1 \bar{A}_0$$

$$\bar{A}_1 \bar{A}_0 \quad \bar{A}_1 A_0 \quad A_1 \bar{A}_0 \quad A_1 A_0$$

$\bar{A}_3 \bar{A}_2$	10	11	13	2
14	1	5	7	6
12	13	15	14	
18	9	11	10	

$$T_{A_1} = \bar{A}_3 \bar{A}_1 + \bar{A}_1 A_0$$

$$+ A_3 \bar{A}_2 \bar{A}_0 + \bar{A}_3 \bar{A}_2 A_0$$

0	1	13	2
4	15	17	6
12	13	15	14
8	9	11	10

$$T_{A_2} = A_1 A_2 + A_3 \bar{A}_2 A_0 + A_1 A_0 \bar{A}_3$$

10	11	13	2
4	5	7	6
12	13	15	14
8	9	11	10

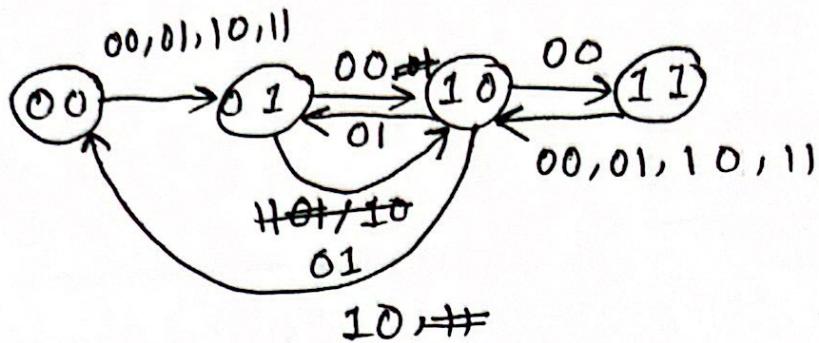
$$T_{A_0} = A_3 \bar{A}_1 \bar{A}_0$$

$$+ \bar{A}_3 \bar{A}_2 A_1$$

$$+ \bar{A}_3 \bar{A}_2 \bar{A}_0$$

$$+ A_3 A_2 \bar{A}_0$$

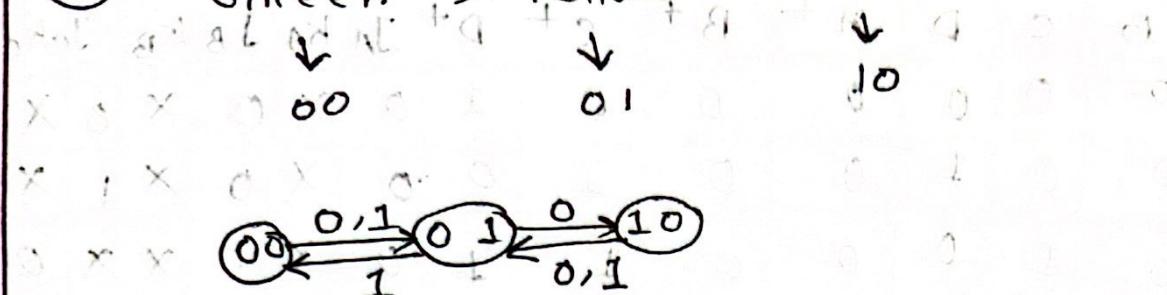
(12) Green  $\rightarrow$  Orange  $\rightarrow$  yellow  $\rightarrow$  red  $\rightarrow$  yellow  $\rightarrow$  orange  
 ↓      ↓      ↓      ↓  
 00      01      10      11       $\rightarrow$  yellow  $\rightarrow$  green



$x$	$y$	A	B	$A^+$	$B^+$	$T_A$	$T_B$
0	0	0	0	0	1	0	1
0	0	0	1	1	0	1	1
0	0	1	0	1	1	0	1
0	0	1	1	1	0	0	1
0	1	0	0	0	1	0	1
0	1	0	1	1	0	1	1
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	1
1	0	0	0	0	1	0	1
1	0	0	1	1 X	0 X	1 X	1 X
1	0	1	0	0	0	1	0
1	0	1	1	1	0	0	0 1
1	1	0	0	0	1	0	1
1	1	0	1	1 X	0 X	1 X	1 X
1	1	1	0	0 X	0 X	1 X	0 X
1	1	1	1	1	0	0	1

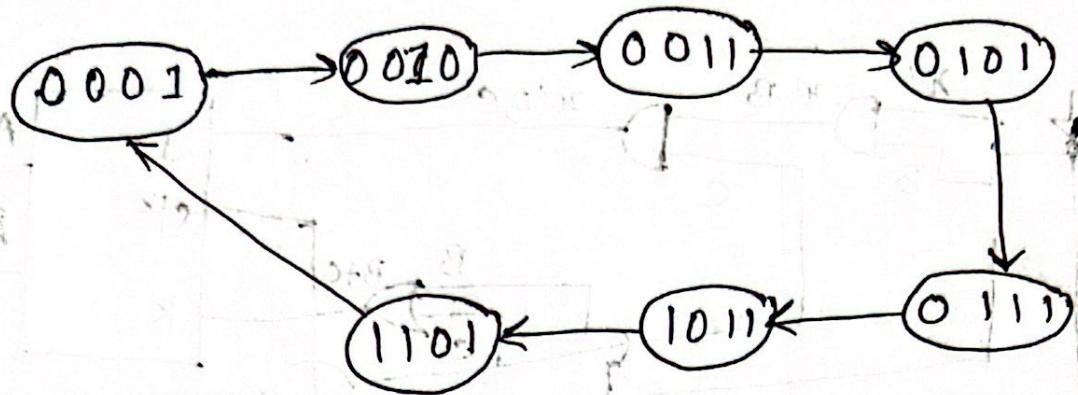
13

Green → Yellow → Red → yellow → green



$\alpha$	A	B	$A^+$	$B^+$	$J_A$	$KA$	$JB$	$KB$
0	0	0	0	1	0	X	1	X
0	0	1	1	0	1	X	X	1
0	1	0	0	1	0	X	1	X
0	1	1	X	X	X	X	X	X
1	0	0	0	1	0	X	1	X
1	0	1	0	0	0	X	X	1
1	1	0	0	1	X	1	1	X
1	1	1	X	X	X	X	X	X

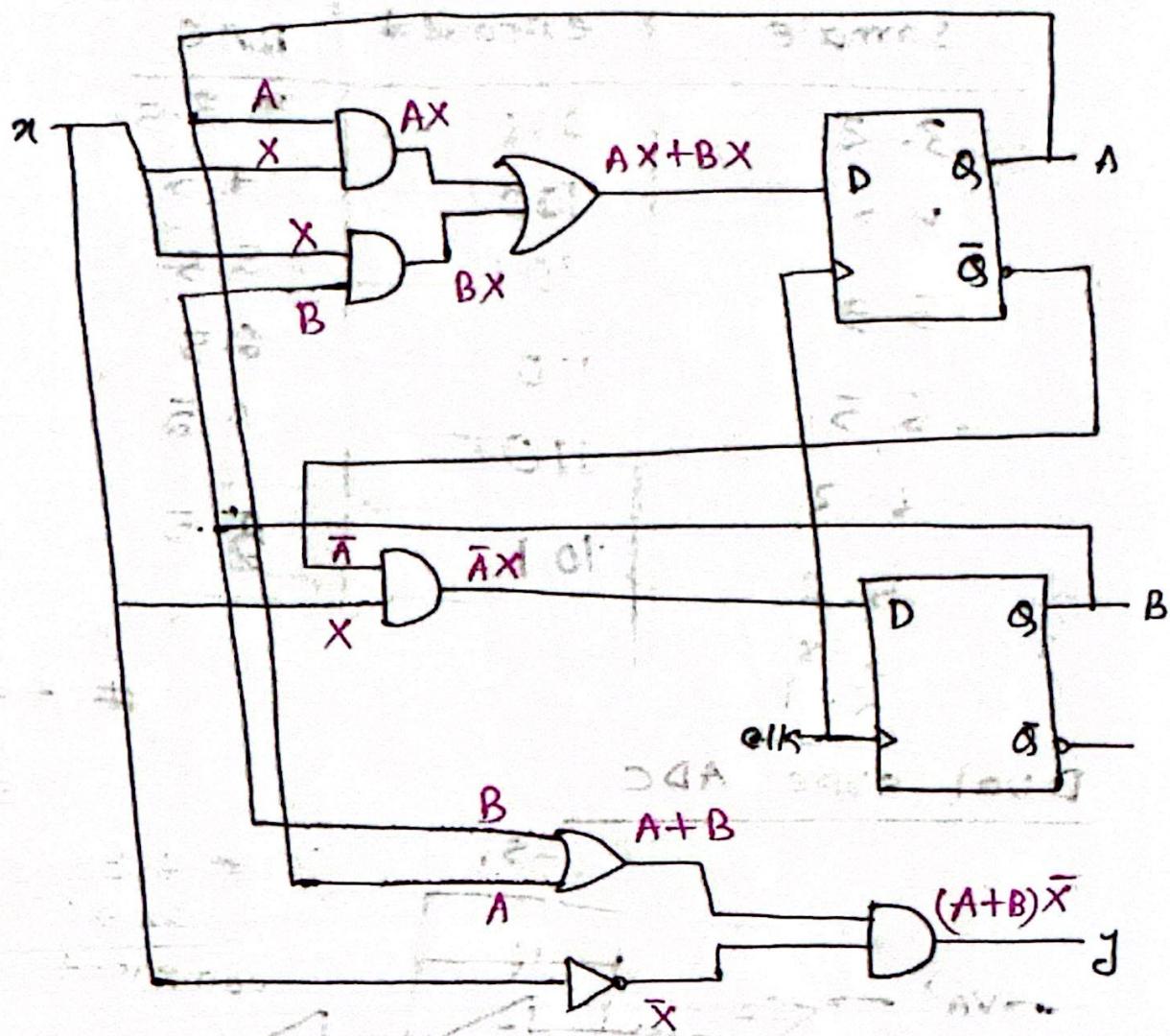
(11)  $1 \rightarrow 2 \rightarrow 3 \rightarrow 5 \rightarrow 7 \rightarrow 11 \rightarrow 13 \rightarrow 1$



A	B	C	D	$A^+$	$B^+$	$C^+$	$D^+$	$J_A$	$K_A$	$J_B$	$K_B$	$J_C$	$K_C$	$J_D$	$K_D$
0	0	0	0	0	0	0	1	0	x	0	x	0	x	1	x
0	0	0	1	0	0	1	0	0	x	0	x	1	x	x	1
0	0	1	0	0	0	1	1	0	x	0	x	x	0	1	x
0	0	1	1	0	1	0	1	0	x	1	x	x	1	x	0
0	1	0	0	0	0	0	1	0	x	x	1	0	x	1	x
0	1	0	1	0	1	1	1	0	x	x	0	1	x	1	x
0	1	1	0	0	0	0	1	0	x	x	1	x	1	1	x
0	1	1	1	1	0	1	1	1	x	x	1	x	0	x	0
1	0	0	0	0	0	0	1	x	1	0	x	0	x	1	x
1	0	0	1	0	0	0	1	x	1	0	x	0	x	0	x
1	0	1	0	0	0	0	1	x	1	0	x	x	1	1	x
1	0	1	1	1	1	0	1	x	0	1	x	x	1	x	0
1	1	0	0	0	0	1	1	x	1	x	1	1	x	1	x
1	1	0	1	0	0	0	1	x	1	x	1	0	x	x	0
1	1	1	0	0	0	0	1	x	1	x	1	x	1	1	x
1	1	1	1	0	0	0	1	x	1	x	1	x	1	x	0

## Assignment 4

⑥



i) 2 flip-flops are there

$$D_a : Ax + Bx$$

$$D_b : \bar{Ax}$$

$$Y : (A + B)\bar{x}$$

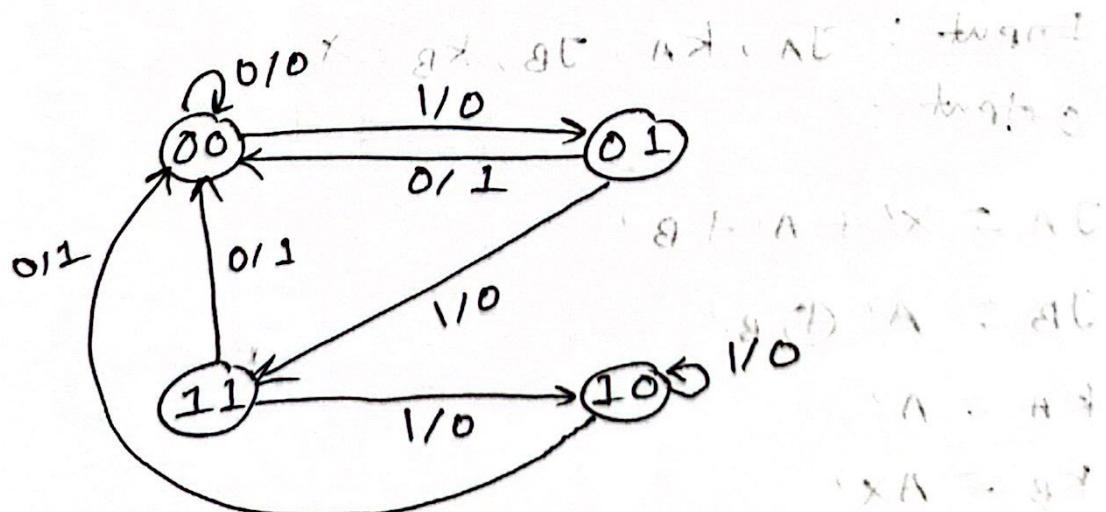
## State table

A	B	$\pi$	$D_a$	$D_b$	y	$A^+$	$B^+$
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	0	0	1	0	0
0	1	1	1	1	0	1	1
1	0	0	0	0	1	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	1	0	0
1	1	1	1	0	0	1	0

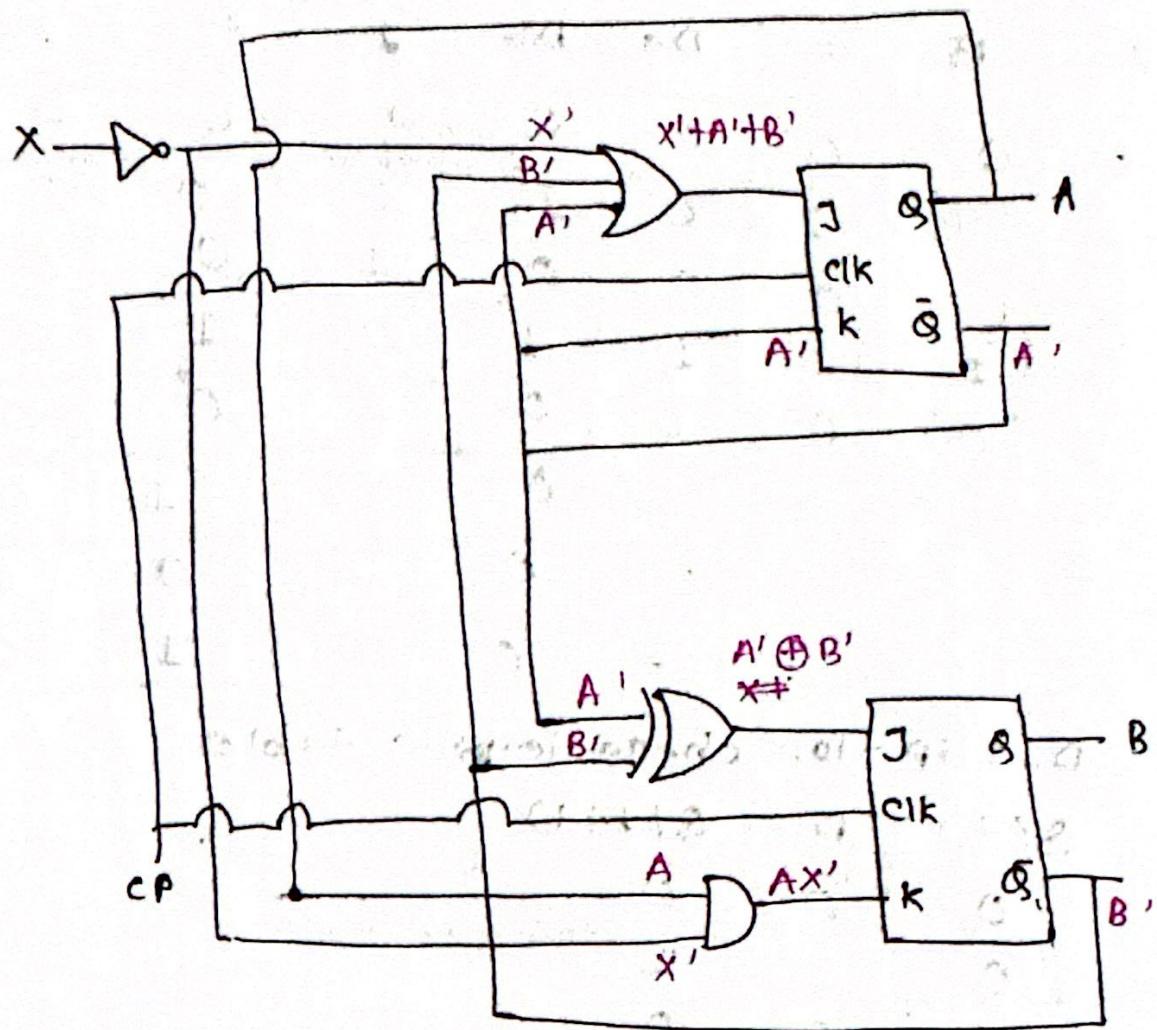
D flip flop characteristic table

$Q(+)$	D	$Q(++)$
0	0	0
0	1	1
1	0	0
1	1	1

state diagram:  $g + A$  : state transition



(7)

Present state :  $A, B$ Next state :  $A^+, B^+$ Input :  $J_A, K_A, J_B, K_B, X$ 

Output :

$$J_A = X' + A' + B'$$

$$J_B = A' \oplus B'$$

$$K_A = A'$$

$$K_B = AX'$$

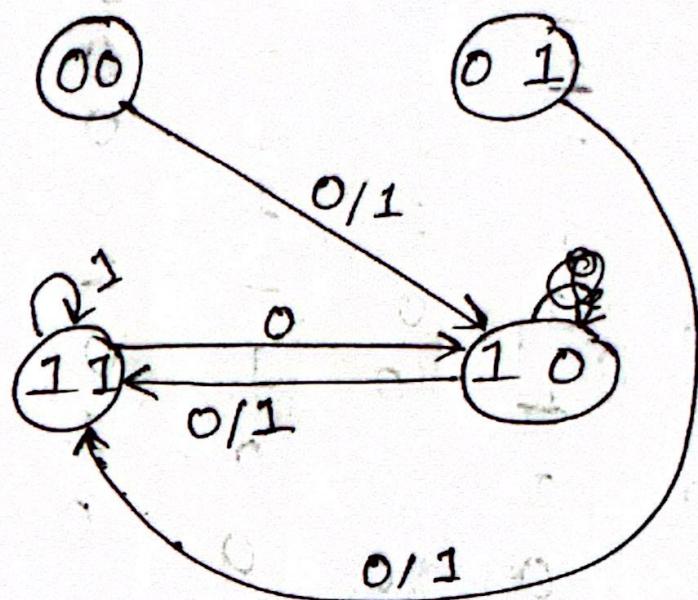
State table

A	B	x	J <sub>A</sub>	K <sub>A</sub>	J <sub>B</sub>	K <sub>B</sub>	A <sup>+</sup>	B <sup>+</sup>
0	0	0	1	1	0	0	1	0
0	0	1	1	1	0	0	1	0
0	1	0	1	1	1	0	1	1
0	1	1	1	1	1	0	1	1
1	0	0	1	0	1	0	1	0
1	0	1	1	0	1	1	1	1
1	1	0	1	0	0	1	1	0
1	1	1	0	0	0	0	1	1

JK characteristic table

Q(t)	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

State diagram :



## Practice sheet (memory)

\* How many address line do we need for a 64 MB RAM with 16 bit / word?

Capacity = no of word  $\times$  bit per word

$$\Rightarrow 64 \text{ MB} = Y \times 16$$

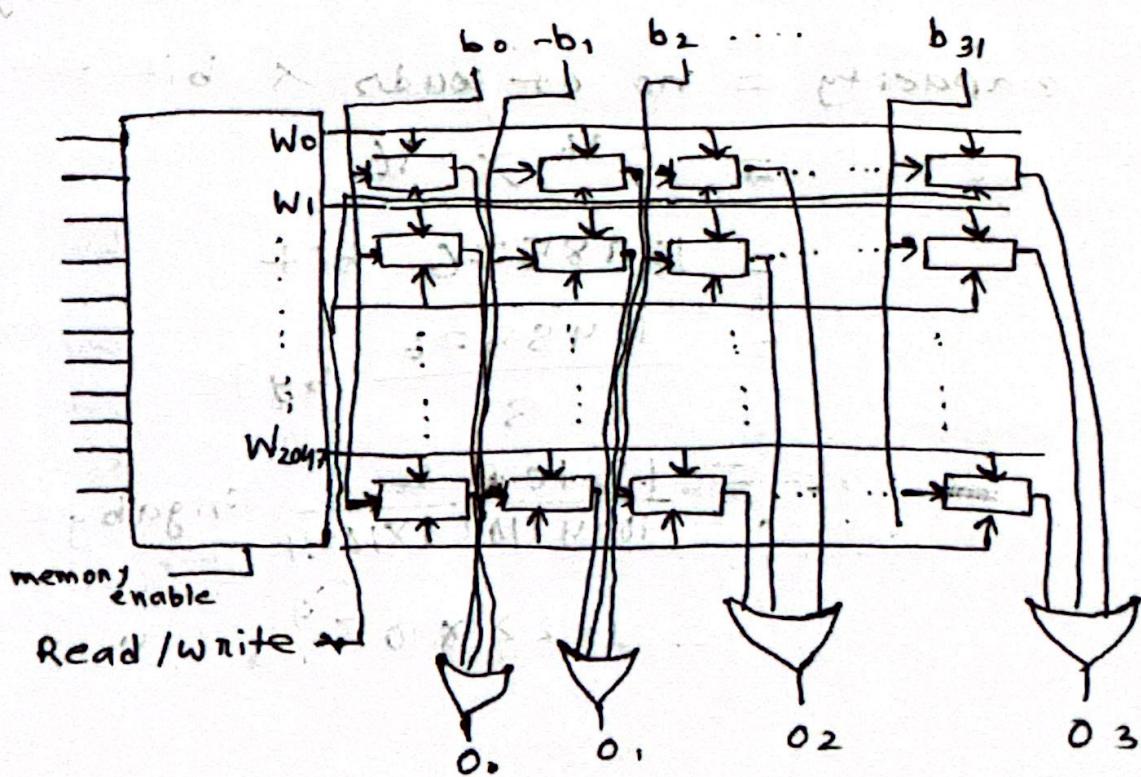
$$\Rightarrow 64 \times 8 \times 1024 \times 1024 = 16Y$$

$$\Rightarrow Y = 33554432$$

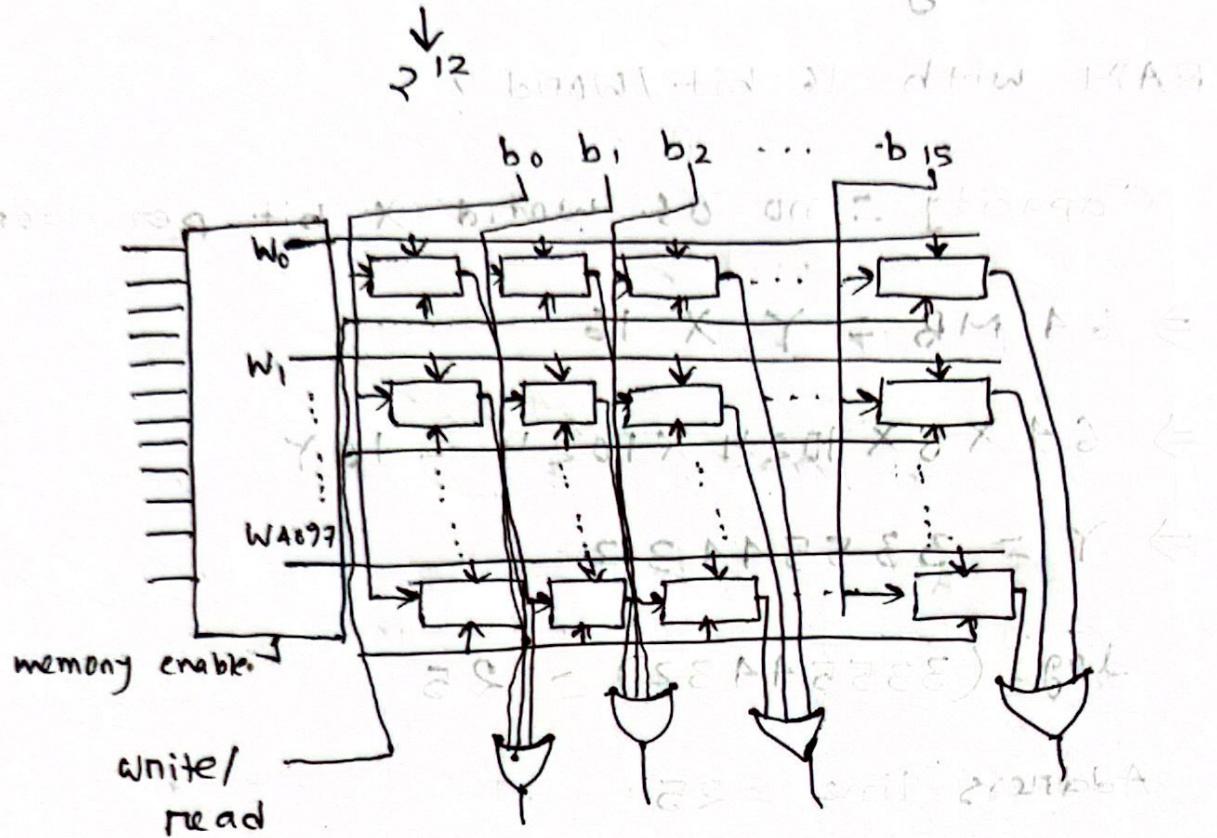
$$\log_2(33554432) = 25$$

Address line = 25

\* Design a  $2048 \times 32$  RAM showing internal details



\* Design a  $1024 \times 16$  RAM showing internal details



\* What is the capacity for a  $2^{16} \times 16$  RAM in Gigabytes?

capacity = no of words  $\times$  bit per word

$$= 2^{16} \times 16$$

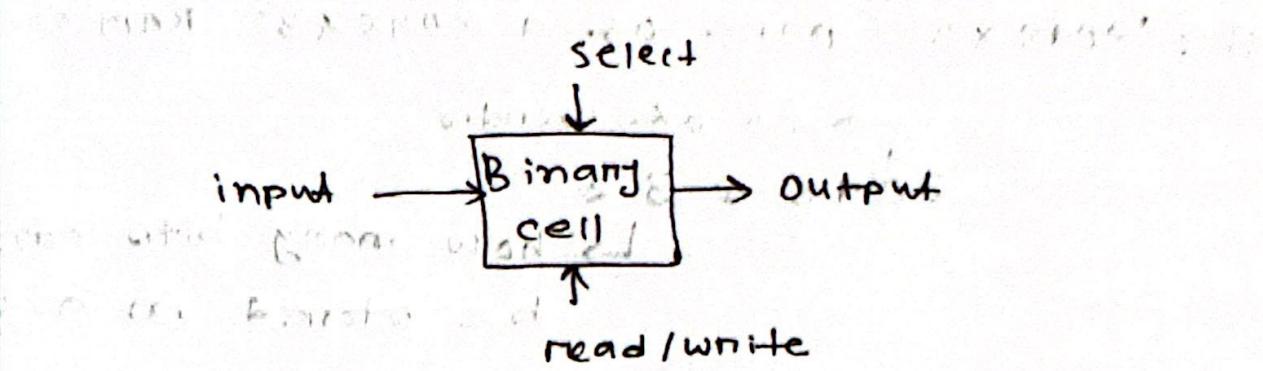
$$= 1048576 \text{ bit}$$

$$= \frac{1048576}{8} \text{ byte}$$

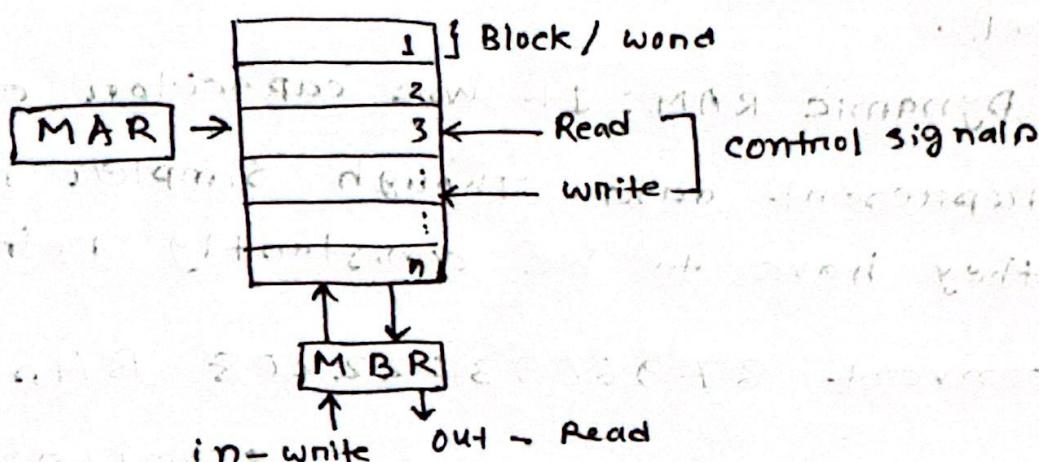
$$= \frac{131072}{1024 \times 1024 \times 1024} \text{ Gigabytes}$$

$$= 1.22 \times 10^{-4}$$

\* Draw the block diagram of a binary cell.



\* Draw and explain the functionalities of MAR and MBR.



\* What type of information can you get from the '2048 x 32' part of a 2048 x 32 RAM?

→ no of words  
2048 x 32 → 2<sup>11</sup> words  
↳ how many bits can be stored in a word

\* How many types of RAM are there? Explain

- There are two types of RAM.

i) Static RAM: It uses flip-flops as the memory cell.

ii) Dynamic RAM: It uses capacitors changes to represent data. Though simpler in circuitry, they have to be constantly refreshed.

\* Convert 8796093022208 Bits to Gigabytes

$$8796093022208 \text{ bits} = \frac{8796093022208}{8 \times 1024 \times 1024 \times 1024} = 1024 \text{ Gigabytes}$$

\* Convert 3 Terabytes to bits.

$$\begin{aligned}3 \text{ Terabyte} &= 3 \times 8 \times 1024 \times 1024 \times 1024 \times 1024 \\&= 3.64 \times 10^{13} \text{ bits.}\end{aligned}$$