

Department of Computer Science and Engineering
BRAC University
CSE 260: Digital Logic Design

Experiment Name:

Experiment # 1: Familiarization with Fundamental Logic Gates

Experiment # 2: Universal Gates, Applications of Boolean Algebra

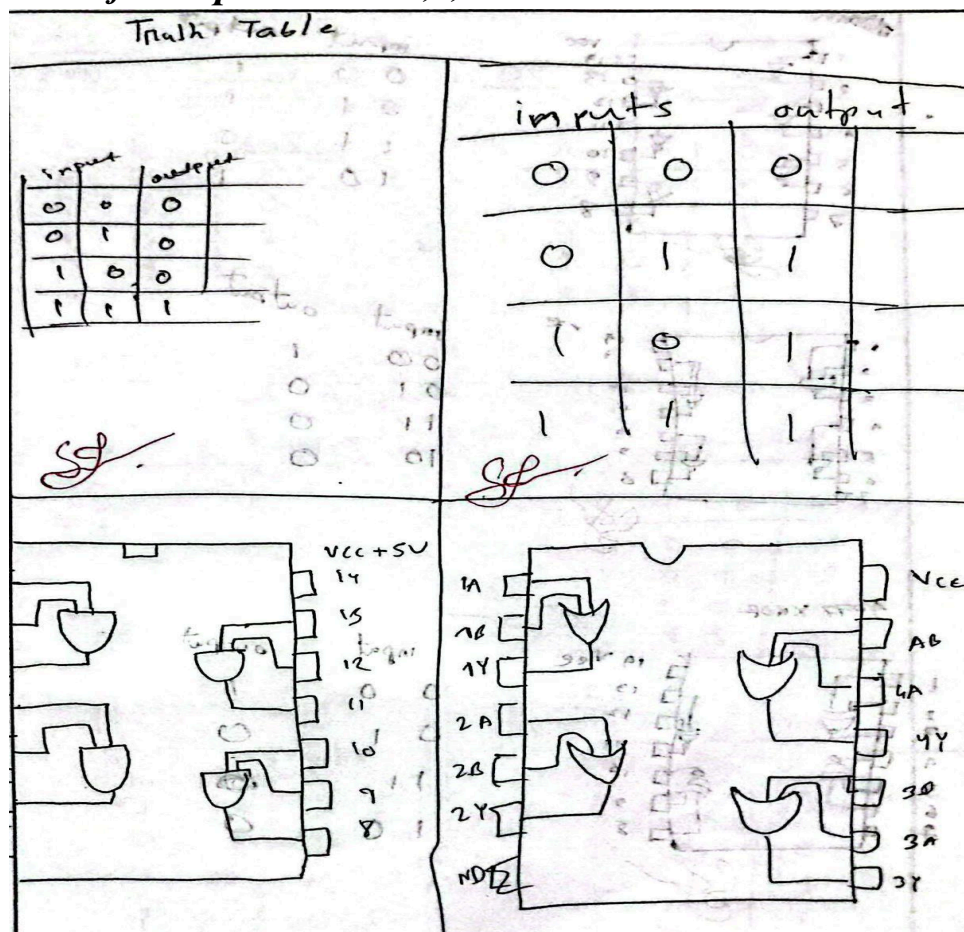
Experiment # 3: Parity Bit Checker and Generator

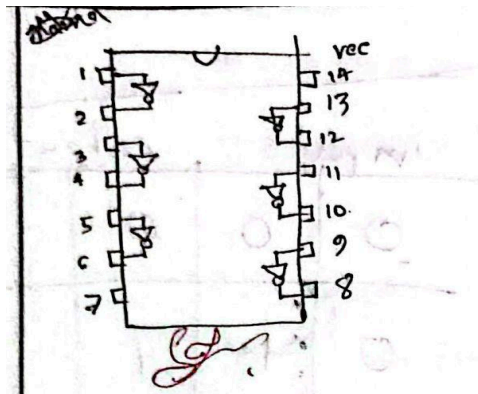
Required Components for Experiment -1,2,3:

1. IC 7408 \times 1
2. IC 7432 \times 1
3. IC 7404 \times 1
4. IC 7400 \times 1
5. IC 7402 \times 1
6. IC 7486 \times 1
7. IC 4077 \times 1

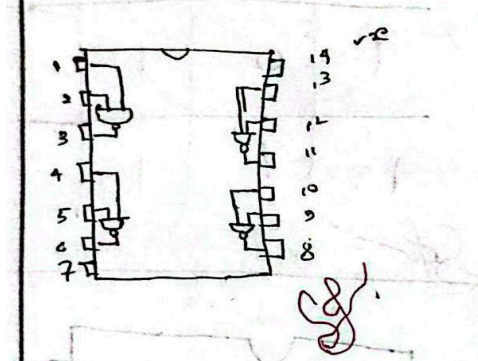
Experimental Setup for Experiment - 1,2,3:

Result for Experiment - 1,2,3:

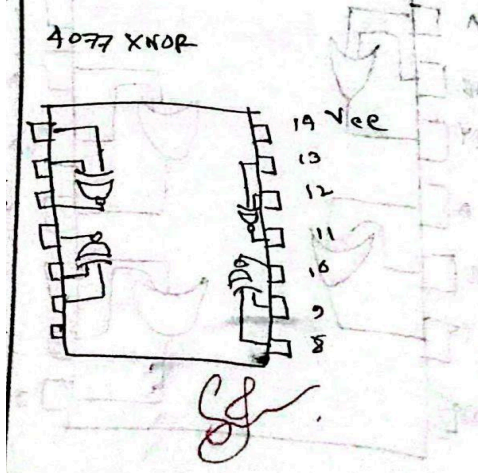




| input | | output |
|-------|---|--------|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |
| 1 | 0 | 1 |



| input | | output |
|-------|---|--------|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |
| 1 | 0 | 0 |



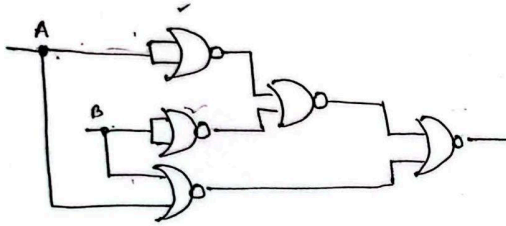
| input | | output |
|-------|---|--------|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |
| 1 | 0 | 0 |

TOPIC NAME : _____

TIME : _____

DATE : _____

Output



| | | |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

$$\left(((A+A)' + (B+B)')' + (A+B)' \right)'$$

$$= ((A+A)' + (B+B)')'' \cdot (A+B)''$$

$$= ((A' \cdot A') + (B' \cdot B')) \cdot (A+B)$$

$$= (A' + B') \cdot (A+B)$$

$$= AA' + AB' + A'B + BB'$$

$$= AB' + A'B$$

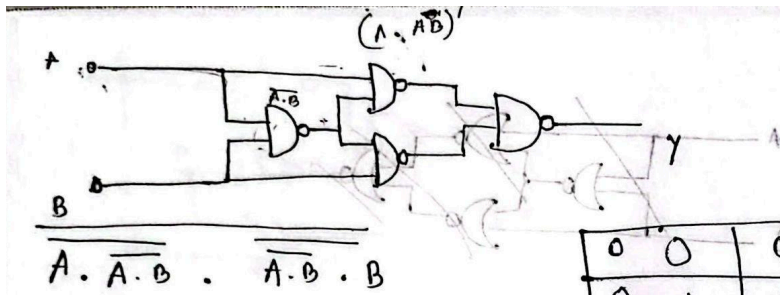
| inputs | | output |
|--------|---|--------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

$$(A+B') = A + (A'+0) \cdot B$$

$$AA' + AB' + A'B + BB'$$

$$= AB' + A'B$$

Abbrar



$$= (A \cdot (A \cdot B)')'' + ((A \cdot B)' \cdot B)''$$

$$= (A' + A \cdot B) + (A \cdot B + B')$$

| | | |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

$$= \left((A \cdot (A \cdot B)')' \cdot ((A \cdot B)' \cdot B)' \right)'$$

$$= (A \cdot (A \cdot B)')'' + ((A \cdot B)' \cdot B)''$$

$$= (A \cdot (A \cdot B)') + (B \cdot (A \cdot B)')$$

$$= (A(\bar{A} + \bar{B})) + (B(\bar{A} + \bar{B}))$$

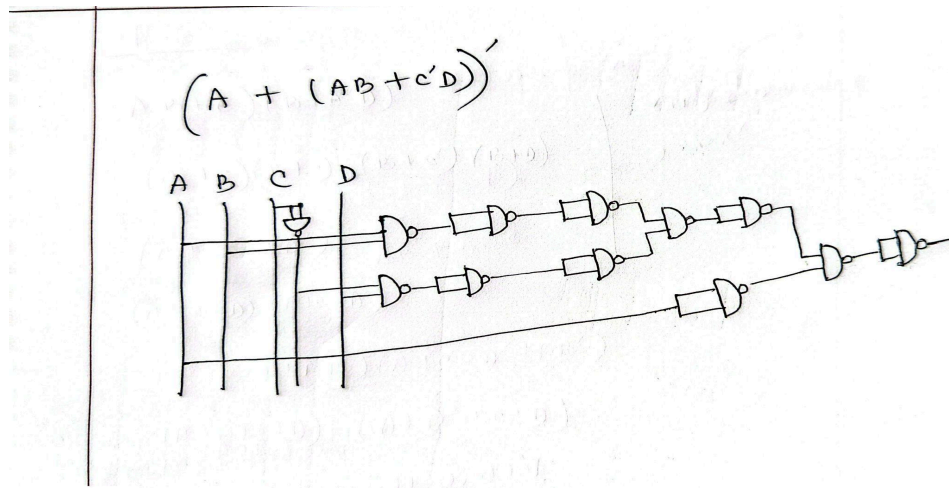
$$= A\bar{B} + \bar{A}B$$

| Data | | | | | |
|------|----------------|----------------|----------------|----------------|--------|
| | D ₃ | D ₂ | D ₁ | D ₀ | Parity |
| a | 1 | 0 | 0 | 1 | 0 |
| b | 0 | 0 | 0 | 1 | 1 |
| c | 1 | 1 | 1 | 1 | 0 |
| d | 0 | 0 | 0 | 0 | 0 |

| | Parity | D ₃ | D ₂ | D ₁ | D ₀ | Error |
|---|--------|----------------|----------------|----------------|----------------|-------|
| a | 1 | 1 | 0 | 0 | 1 | 1 |
| b | 0 | 0 | 0 | 0 | 1 | 1 |
| c | 0 | 1 | 1 | 1 | 1 | 0 |
| d | 1 | 0 | 0 | 0 | 0 | 1 |

Answer the following questions also as part of discussion:

1. Implement the following function using NAND gate only:
 $(A + (AB + C'D))'$. Do not simplify the function. Draw the circuit diagram only.
2. Draw the circuit diagrams of 3-bit parity checker and generator using NOR gate(s) only



[2]

