

Department of Computer Science and Engineering
BRAC University
CSE260: Digital Logic Design

Group: 06

Group members:

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Experiment # 4: Design and Implementation of 4-bit Parallel Binary Adder

Experiment # 5: Implementation of 4-bit Magnitude Comparator

Experiment # 6: Design circuits using encoder & decoder.

Experiment # 7: Function Implementation Using MUX.

Required Components for Lab - 4:

1. IC 7408
2. IC 7432
3. IC 7486
4. IC 7483

Required Components for Lab - 5:

1. IC 7408
2. IC 7432
3. IC 7404
4. IC 4077

Required Components for Lab - 6:

1. IC 74138
2. IC 74148

Required Components for Lab - 7:

1. IC 74153
2. IC 7408
3. IC 7432
4. IC 7404

Experimental Setup:

Experimental Setup for Lab - 4:

Experimental Setup for Lab - 5:

Experimental Setup for Lab - 6:

Experimental Setup for Lab - 7:

Result:

Result for Lab - 4:

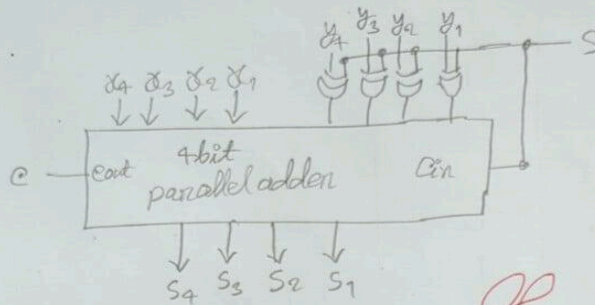
Result for Lab - 5:

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Result for Lab - 6:

Result for Lab - 7:

(Lab 4)



(i) 4bit Parallel Adder:

	A	B	Cin	C4	S4	S3	S2	S1
a	0000	1000	0	0	1	0	0	0
b	1100	1101	0	1	1	0	0	1
c	1110	0011	0	1	0	0	0	1
d	1111	1111	0	1	1	1	1	0

(ii) 4bit Parallel Adder cum Subtractor:

	A	B	Cin	C4	S4	S3	S2	S1
a	1100	1000	1	0	0	1	0	0
b	1100	1101	0	1	1	0	0	1
c	1110	0011	1	0	1	0	1	1
d	1111	1111	0	1	1	1	1	0

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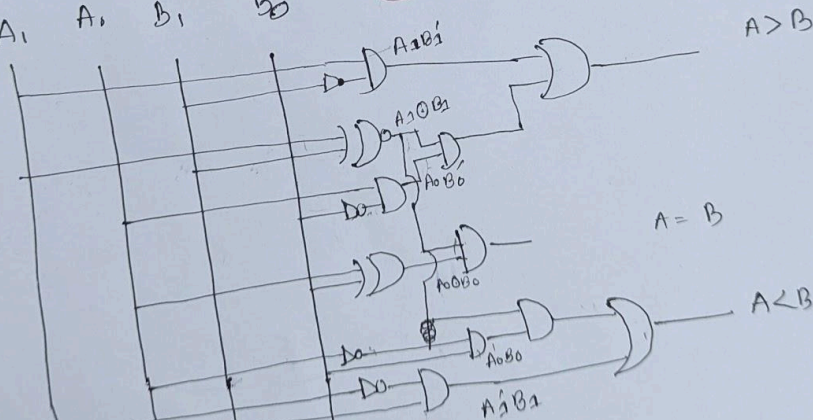
A	B	$A > B$	$A = B$	$A < B$
00	00	0	✓ 1	0
10	01	✓ 1	0	0
11	11	0	✓ 1	0
01	01	0	0	✓ 1
01	10	0	0	✓ 1
01	00	✓ 1		

$$A > B = A_1 B_1' + A_1 \odot B_1 \cdot A_0 B_0'$$

$$A < B = A_1' B_1 + A_1 \odot B_1 \cdot A_0' B_0$$

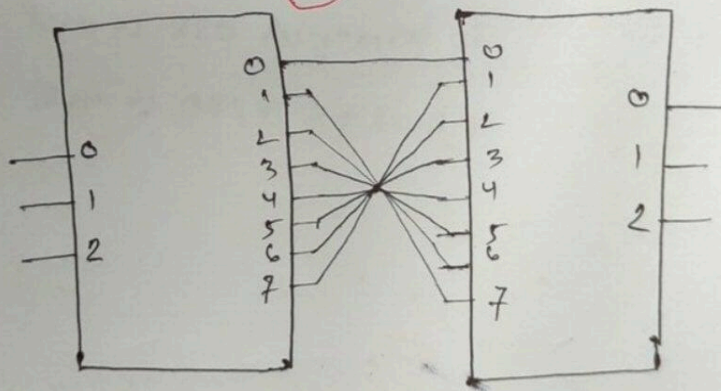
$$A = B = (A_0 \odot B_0) (A_1 \odot B_1)$$

$A_1 \quad A_0 \quad B_1 \quad B_0$



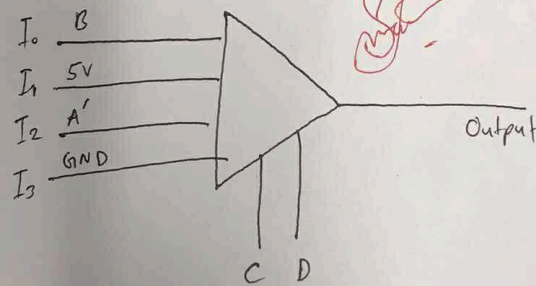
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Inputs				Active Low outputs		
minterm	C	B	A	D2	D1	D0
0	0	0	0	1	1	1
1	0	0	1	0	0	0
2	0	1	0	0	0	1
3	0	1	1	0	1	0
4	1	0	0	0	1	1
5	1	0	1	1	0	0
6	1	1	0	1	0	1
	1	1	1	1	1	0



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MUX input lines				Selectors		Output
13	12	11	10	S1	S0	Y
0	0	0	1	0	0	1
1	1	1	0	0	0	0
0	0	1	0	0	1	1
1	1	0	1	0	1	0
0	1	0	0	1	0	1
1	0	1	1	1	0	0
1	0	0	0	1	1	1
0	1	1	1	1	1	0



$$I_0 = A'B + AB = B$$

$$I_1 = 1$$

$$I_2 = A'B' + A'B = A'$$

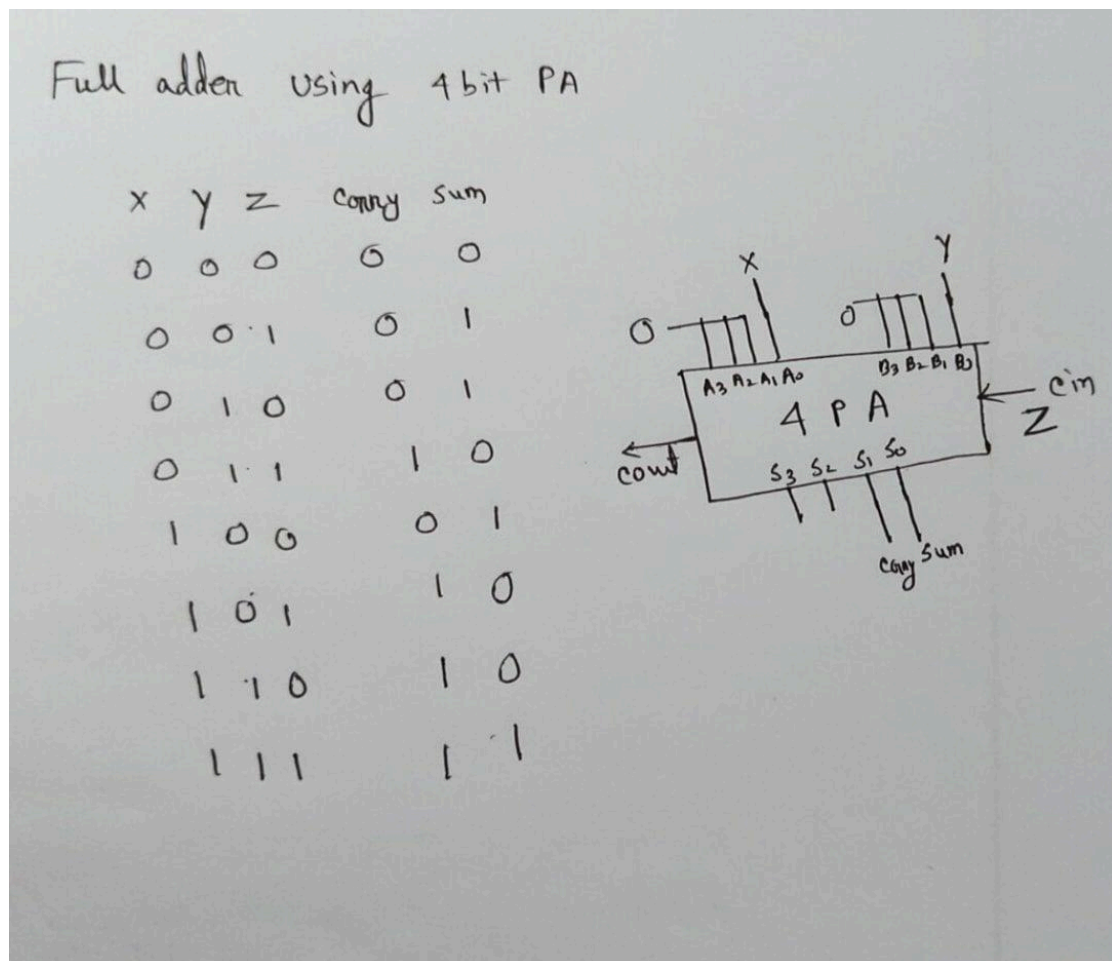
$$I_3 = 0$$

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Discussion:

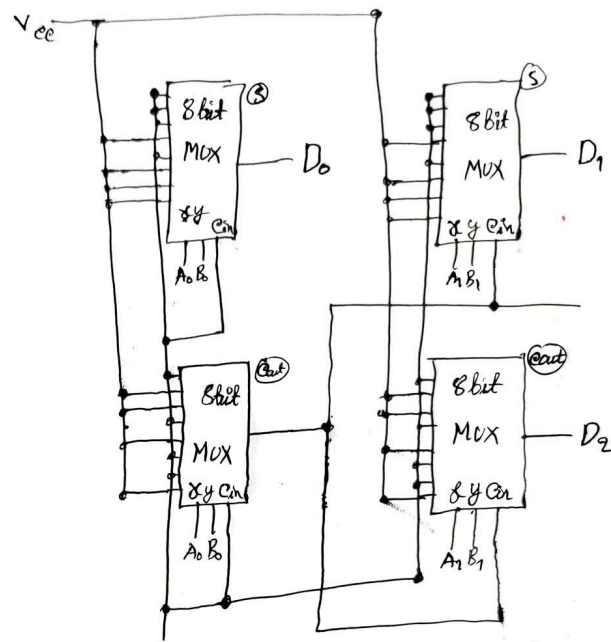
Answer the following questions also as part of discussion:

1. Design a Full adder using a 4-bit Parallel adder.
2. Design a 2-bit Parallel adder using exactly four 8:1 Mux(s)



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x	y	G_m	G_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



$$B \approx B_1 B_0$$

$$= A_1 A_0 + B_1 B_0$$

$$D_2 D_1 D_0$$