UNIT-3 DIGITAL ELECTRONICS

*

OR 

NOT 

AND 

NAND  $\overline{AB}$

NOR  $\overline{A+B}$

XOR  $A \oplus B$

$Y = \bar{A}B + A\bar{B}$

0 if same

odd fn gate

o/p = 1 for odd no. of 1

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

XNOR  $A \odot B$

$Y = \overline{\bar{A}B + A\bar{B}}$

$Y = AB + \bar{A}\bar{B}$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

* Principle of duality : 0 with 1, 1 with 0, + with .

LAWS

* Distributive Law : $A + BC = (A+B)(A+C)$

* De Morgan's Theorem: $\overline{A+B} = \bar{A}\cdot\bar{B}$

$\overline{A+B+C} = \bar{A}\cdot\bar{B}\cdot\bar{C}$

* Absorption Theorem: $A + AB = A$ dual: $A\cdot(A+B) = A$

$A + \bar{A}B = A + B$

$A(\bar{A}+B) = A\cdot B$

* Consensus Theorem : $AB + \bar{A}C + BC = AB + \bar{A}C$

#	SOP	POS
	make f = 1 and take them	make f = 0
	AND - OR	OR - AND
	$f = \Sigma m(\ )$	$f = \pi M(\ )$
	min-terms	max terms

To convert to SOP

eg $F = A + B\cdot C$

$F = A\cdot 1\cdot 1 + B\cdot C\cdot 1$

$F = A(B+\bar{B})(C+\bar{C}) + (A+\bar{A})BC$

To convert to POS

eg: $F = (x'+y)(x+z)(y+z)$

$F = (x'+y+0)(x+0+z)(0+y+z)$

$F = (x'+y+zz')(x+yy'+z)(xx'+y+z)$

Half Adder

COMBINATIONAL CIRCUITS

29th November

Inputs		Outputs	
X	Y	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$Sum = \bar{X}\cdot Y + X\bar{Y} = X \oplus Y$ (X XOR Y)

$Carry = X \cdot Y$

Using NAND only
4 NAND for SUM
1 NAND for Carry
5

1 XOR for Sum
1 AND for Carry
2

Full Adder

	Input			Output	
	X	Y	Z	Carry	Sum
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	0	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	1	0
6	1	1	0	1	0
7	1	1	1	1	1

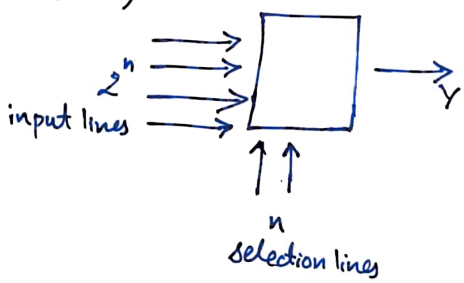
$Sum = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XYZ$
$= X \oplus Y \oplus Z$

$Carry = (X \oplus Y)Z + X\cdot Y = XY + YZ + XZ$

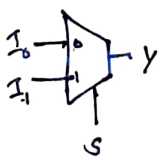
9 NAND

2 XOR
2 AND
1 OR

Multiplexer (MUX)



→ 2:1 MUX



S	Y
0	I_0
1	I_1

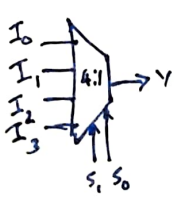
$Y = S'I_0 + SI_1$

↓ using NAND gates ⇒

$Y = ((S'I_0 + SI_1)')'$

$Y = ((S'I_0)' \cdot (SI_1)')' \rightarrow$ 4 NAND

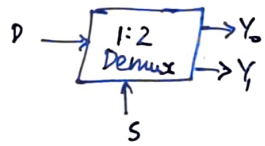
→ 4:1 MUX



S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$Y = S_1'S_0'I_0 + S_1'S_0I_1 + S_1S_0'I_2 + S_1S_0I_3$

Demultiplier (DEMUX)



S	Y_0	Y_1
0	D	-
1	-	D

$Y_0 = S'D$ $Y_1 = SD$

↓ using NAND

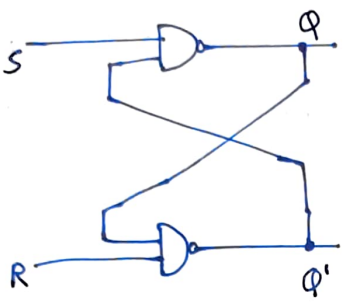
$Y_0 = ((S'D)')'$ $Y_1 = ((SD)')'$ → 4 NAND

SEQUENTIAL CIRCUITS

- Synchronous → clock
- Asynchronous → no clock

* When clk = 0 always memory state

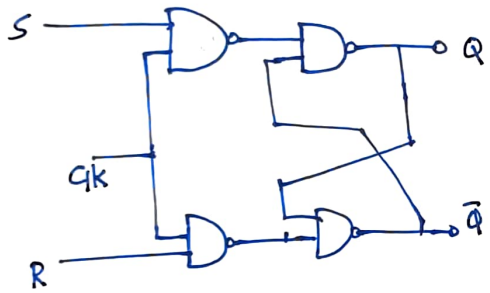
The R-S (Reset - Set) Latch



Input S	Input R	Output Q_{t+1}
1	1	$Q_{prev.}$ (memory)
0	1	1 (set)
1	0	0 (reset)
0	0	Invalid

$Q_{t+1} = \bar{S} R + Q\bar{R}$

The R-S (Reset-Set) Flip-Flop / Gated R-S latch



Clk = 0 => memory

S = 0, R = 0 ⇒ memory

S = 0, R = 1 ⇒ reset

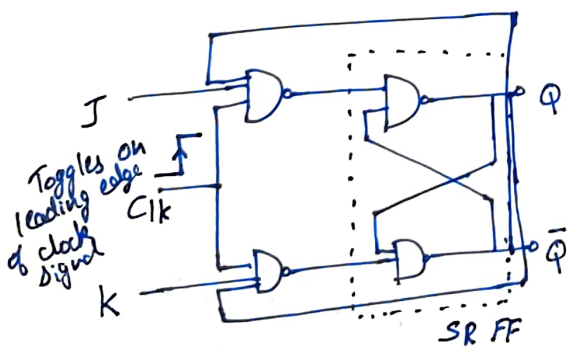
S = 1, R = 0 ⇒ set

$$Q_{t+1} = S + \bar{R} Q$$

Clk	S_t	R_t	Q_t	Q_{t+1}	Operation
1	0	0	0	0	No change (memory)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set (always)
1	1	0	1	1	
1	1	1	0	X	Invalid
1	1	1	1	X	
0	X	X	X	Q_t	No change (memory)

JK Flip-Flop

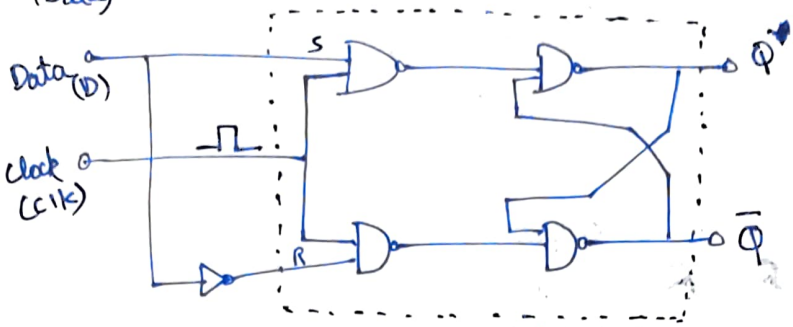
(J = S & K = R)



$$Q_{t+1} = J\bar{Q} + \bar{K}Q$$

Clk	J	K	Q_t	Q_{t+1}	$\bar{Q}$	Operation
1	0	0	0	0		Same as R-S Latch: memory
1	0	0	1	1		
1	0	1	0	0		Reset Q = 0
1	0	1	1	0		
1	1	0	0	1		Set Q = 1
1	1	0	1	1		
1	1	1	0	1		Toggle
1	1	1	1	0		Toggle action
0	X	X	0	0		
0	X	X	1	1		

D-Flip-Flop
(Data)



gated R-S FF

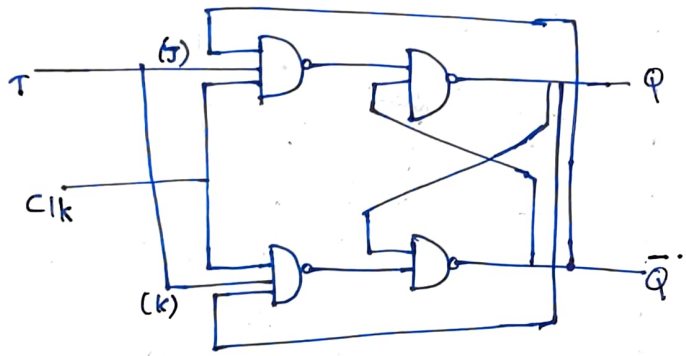
Input	Outputs	
	present state	next state
D	Q_t	Q_{t+1}
0	0	0
0	1	0
1	0	1
1	1	1

Clk	D	Q^+
0	X (doesn't matter)	Q (memory)
1	0	0
1	1	1

o/p follows I/P

$$Q_{t+1} = DQ$$

T-Flip-Flop
(Toggle)



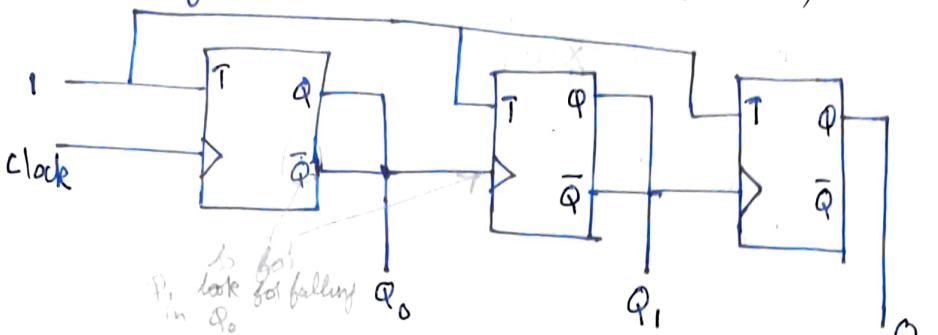
T-FF using JK-FF

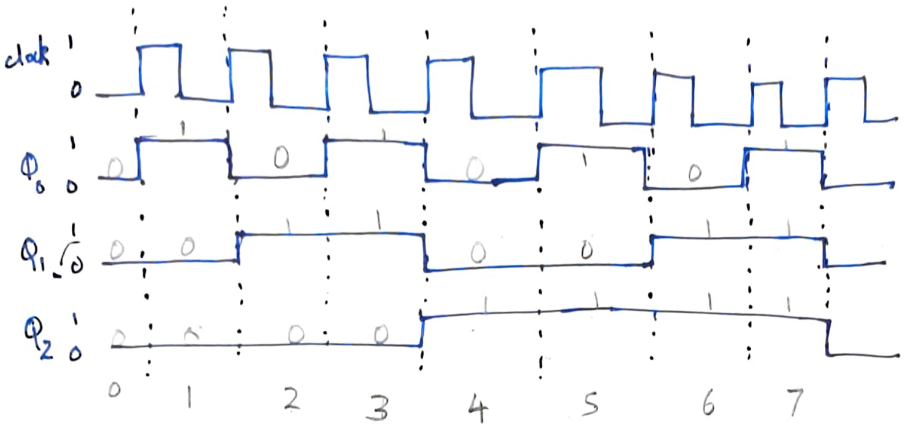
Clk	T	Q^+
0	X	Q (memory)
1	0	Q (memory)
1	1	Toggles

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

$$Q_{t+1} = T\bar{Q} + \bar{T}Q$$
$$= T \oplus Q$$

3-bit asynchronous U.P counter (uses TFF)

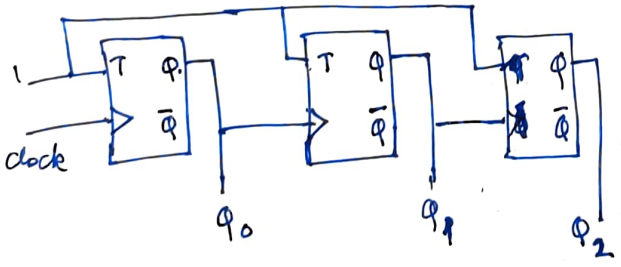


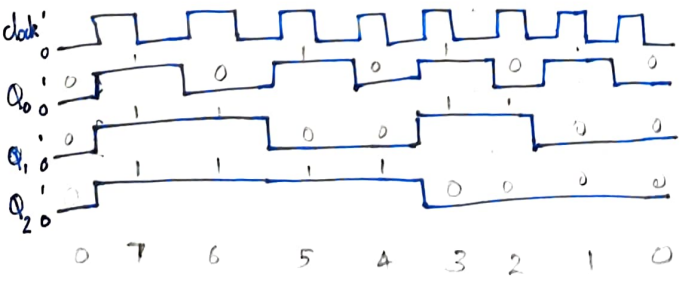


no. of negative edge of clock.	Q_0 (LSB) (2^0)	Q_1 (2^1)	Q_2 (MSB) (2^2)
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

SISO register uses D FF

3-bit asynchronous DOWN counter (uses TFF)



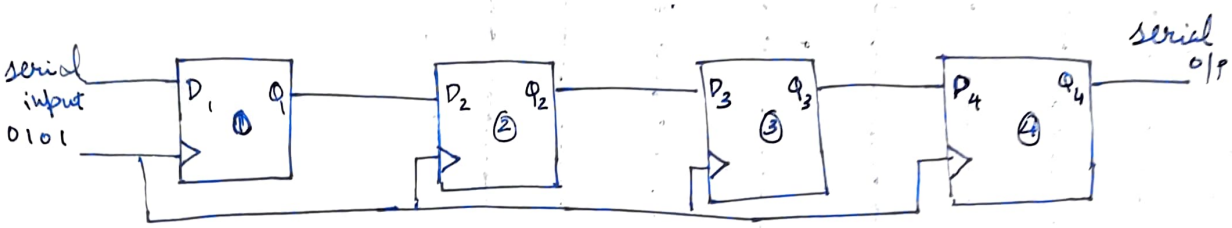


no. of negative edge of clock	Q_0 (LSB) 2^0	Q_1 2^1	Q_2 (MSB) 2^2
0	0	0	0
1	1	1	1
2	0	1	1
3	1	0	1
4	0	0	1
5	1	1	0
6	0	1	0
7	1	0	0

* NAND & NOR → universal gates

	NOT	AND	OR	NOR	XOR	XNOR
NAND $F = \overline{X \cdot Y}$	1	2	3	4	4	5
NOR $F = \overline{X+Y}$	1	3	2	4	5	4

4 bit SISO shift register



clk	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0
clk 1	1	0	0	0
clk 2	0	1	0	0
clk 3	1	0	1	0
clk 4	0	1	0	1
clk 5	0	0	1	0
clk 6	0	0	0	1

clk	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0
clk 1	1	0	0	0
clk 2	1	1	0	0
clk 3	1	0	1	0
clk 4	1	1	0	1
clk 5	1	0	1	0
clk 6	1	0	0	1
clk 7	1	0	0	0