Bahria University,

Karachi Campus

COURSE: Digital Design Lab
TERM: Spring 2025, CLASS: BSIT- 2A/B

PROJECT NAME

Digital Stop Watch

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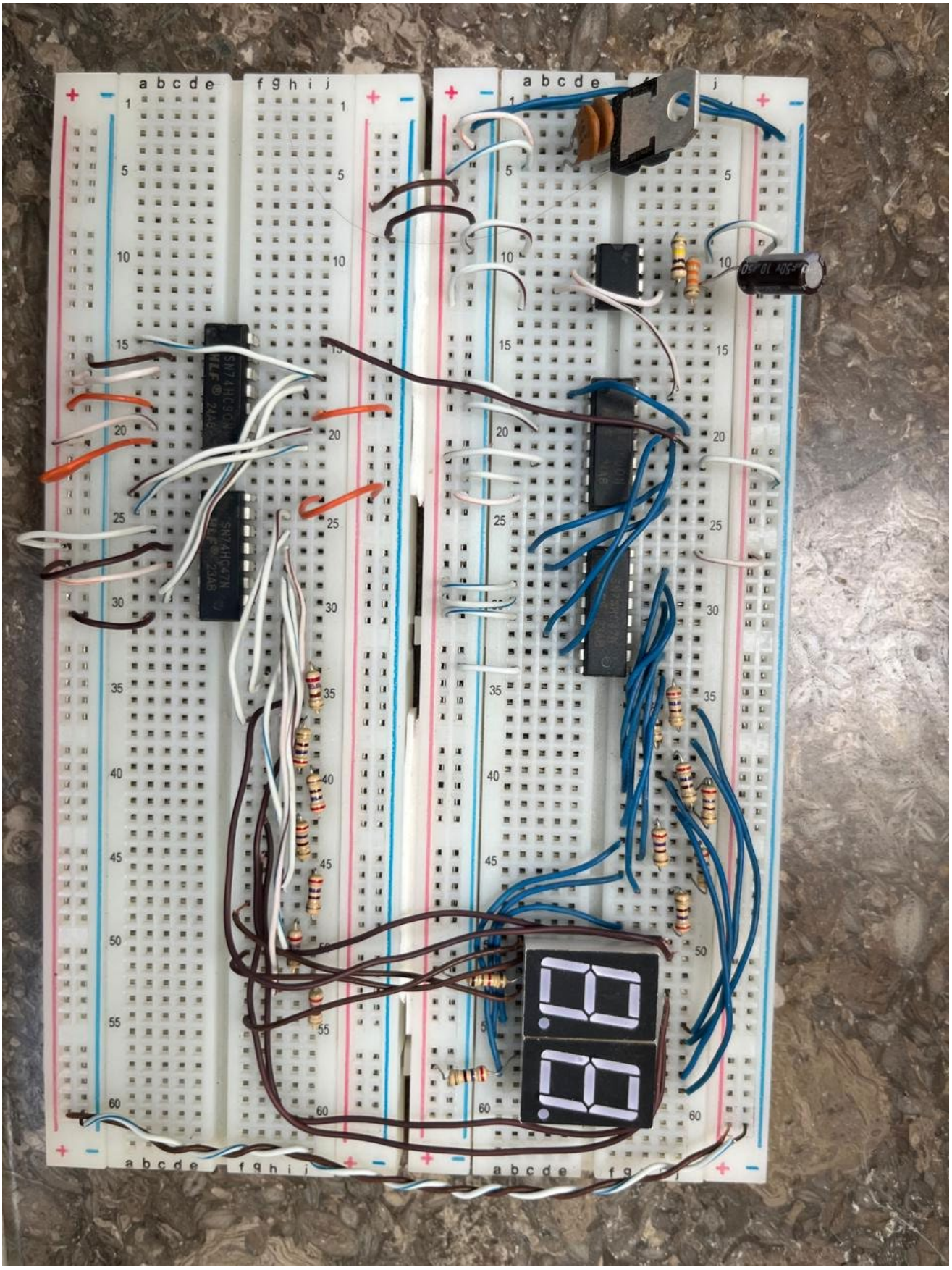
PROJECT SCREENSHOT



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1. INTRODUCTION & PROBLEM STATEMENT

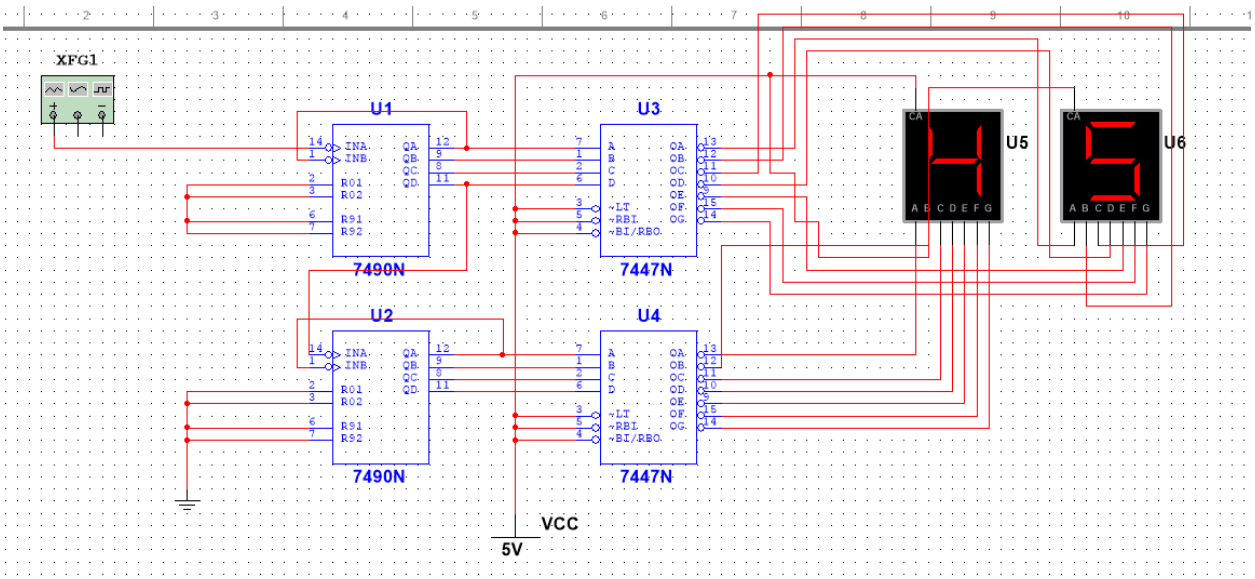
This project builds a basic digital stopwatch using simple logic components, without microcontrollers. It measures elapsed seconds and displays them on two 7-segment displays. The goal is to enhance understanding of counters, decoders, and timers in digital electronics.

2. COMPONENTS

Key components include:

- **555 Timer** (clock generator)
- **Voltage Regulator (e.g., 7805)** (maintains stable 5V)
- **7490 Decade Counters (2)** (counts pulses)
- **7447 BCD to 7-Segment Decoders (2)** (converts count to display output)
- **Common Anode 7-Segment Displays (2)** (shows elapsed time)
- **Resistors & Capacitors** (timing, stabilization, and current limiting)
- **Breadboard/PCB & 9V Battery**

3. CIRCUIT DIAGRAM



4. SIMULATION

Using tools like **Multisim** simulations confirmed the stopwatch function. The **555 Timer** generates 1 Hz pulses, incrementing the counters. At **9**, the first counter resets, triggering the second. Virtual displays verified proper counting.

5. SPECIFICATION

Parameter	Value
Clock Frequency	1 Hz
Operating Voltage	5V DC
Counting Range	00–99 seconds
Display Type	Two-digit 7-segment
ICs Used	7490(Counter), 7447 (decoder)

6. WORKING STEPS

- **Configure the 555 Timer for 1 Hz Clock Pulses:**

Component Used: NE 555 Timer

The **555 Timer** is running in astable mode – which simply means it keeps turning ON and OFF without the need to be being triggered. That makes it perfect for this project. This timer is the heartbeat of the system which sends blinking signals at approximately about **1Hz** or a pulse every **1.15 seconds** making the project as a stable stopwatch.

The Timing Components used in this project which determine the speed/frequency of pulse are:

1. R1 = 100 kΩ
2. R2 = 33 kΩ
3. C = 10 µf

Timing Configuration:

They are connected in this manner where R1 is bridged between Pin 8 (VCC) and Pin 7, R2 is bridged between Pin 7 and Pin 6/2 & C is bridged between Pin6/2 and GND.

The rest configuration of the 555 Timer is as follows;

Pin No.	Pin Name	Connection
1	GND	Connect to Ground (0V)
2	Trigger	Connect to Discharge (Pin 7) and to a junction with capacitor C to GND

3	Output	Connect to Counter IC input (e.g., Pin 14 of SN74HC90N)
4	Reset	Connect to VCC (disable reset function)
5	Control Voltage	(Optional) Connect 10 µF capacitor to GND for stability
6	Threshold	Connect to Discharge (Pin 7)
7	Discharge	Connect to both resistors R1 and R2 as shown in timing configuration
8	VCC	Connect to +5V (via 7805 regulator output)

➢ Connect 7490 Counters for Units and Tens Counting:

Component Used: SN7490N (Decade Counter)

The **7490 IC** counts from 0 to 9. We use two 7490s – the first one counts units (0–9), and the second one counts tens (10–99) by cascading the output of the first into the second.

7490 IC Pin Connections:

PIN NO.	PIN NAME	DESCRIPTION
1	CLKB	Clock Input B (for divide-by-5 section)
2	R1	Reset Input 1 (active high)
3	R2	Reset Input 2 (active high)
4	NC	Not Connected
5	VCC	Positive Supply Voltage (+5V)
6	R3	Reset Input 3 (active high)
7	R4	Reset Input 4 (active high)
8	QC	Output C (third bit of the counter output)
9	QB	Output B (second bit of the counter output)
10	GND	Ground (0V)
11	QD	Output D (fourth bit of the counter output)
12	QA	Output A (first bit of the counter output)
13	NC	Not Connected
14	CLKA	Clock Input A (for divide-by-2 section)

Typical Connections for Decade Counting:

- **Clock Input:** Apply the clock signal to **CLKA (Pin 14)**. This drives the divide-by-2 section, which in turn feeds the divide-by-5 section through internal connections.
- **Reset Inputs:** To reset the counter to 0000, apply a high signal to **R1 (Pin 2)** and **R2 (Pin 3)** simultaneously. For normal operation without resets, these pins can be connected to ground.
- **Outputs:** The counter outputs are available on **QA (Pin 12)**, **QB (Pin 9)**, **QC (Pin 8)**, and **QD (Pin 11)**. These can be connected to a BCD to 7-segment decoder like the 7447 IC to display the count on a 7-segment display.

Cascading Counters:

To count from 00 to 99, two 7490 ICs can be cascaded:

1. **Units Counter:** Receives the primary clock signal on **CLKA (Pin 14)**.
2. **Tens Counter:** The **QD (Pin 11)** output of the units counter is connected to the **CLKA (Pin 14)** of the tens counter. This configuration ensures that the tens counter increments by one each time the units counter completes a full cycle (counts from 0 to 9).

Note: Ensure that all unused reset inputs are connected to ground to prevent unintended resets.

➢ Wire 7447 Decoders to Drive 7-Segment Displays

Component Used: SN7447N (BCD to 7-Segment Decoder/Driver)

The **SN7447N** is a BCD to 7-segment decoder/driver designed to drive **common-anode** 7-segment displays. It accepts a 4-bit binary-coded decimal (BCD) input and provides the necessary outputs to illuminate the appropriate segments to display decimal digits 0 through 9.

Key Features:

- **Active-Low Outputs:** The outputs are active-low, suitable for driving common-anode displays.
- **Ripple Blanking Input (RBI) and Output (RBO):** Used for suppressing leading zeros in multi-digit displays.
- **Lamp Test (LT):** Allows testing of all segments.
- **Blanking Input (BI):** Can be used to turn off all segments, useful for power saving or display control.

7490 IC Pin Connections:

PIN NO.	PIN NAME	DESCRIPTION
1	B	BCD Input Bit 1
2	C	BCD Input Bit 2
3	LT	Lamp Test Input (active low)
4	RBO	Ripple Blanking Output
5	RBI	Ripple Blanking Input (active low)
6	D	BCD Input Bit 3
7	A	BCD Input Bit 0
8	GND	Ground (0V)
9	e	Segment Output 'e' (active low)
10	d	Segment Output 'd' (active low)
11	c	Segment Output 'c' (active low)
12	b	Segment Output 'b' (active low)
13	a	Segment Output 'a' (active low)
14	g	Segment Output 'g' (active low)
15	f	Segment Output 'f' (active low)
16	VCC	Positive Supply Voltage (+5V)

Typical Connections:

- **Power Supply:** Connect **Pin 16 (VCC)** to +5V and **Pin 8 (GND)** to ground.
- **BCD Inputs:** Connect the 4-bit BCD input to **Pins 7 (A)**, **1 (B)**, **2 (C)**, and **6 (D)**.
- **Control Inputs:**
    - **Lamp Test (LT, Pin 3):** Connect to VCC for normal operation; pulling it low turns on all segments.
    - **Ripple Blanking Input (RBI, Pin 5):** Connect to VCC if not used; used for suppressing leading zeros.
- **Outputs to 7-Segment Display:** Connect **Pins 9–15** to the corresponding segments **e, d, c, b, a, g, f** of the 7-segment display. Ensure to use current-limiting resistors (typically 330Ω to 470Ω) in series with each segment to prevent damage.

Note: The SN7447N is designed for **common-anode** 7-segment displays. Ensure compatibility when selecting your display.

- **Ensure Stable Power Using a Voltage Regulator**

Component Used: 7805 Voltage Regulator

To protect the circuit and ICs from voltage fluctuations, use a **7805 regulator** which converts 9V/12V input to a stable **+5V DC** output.

7805 Regulator Pin Connections:

PIN NO.	PIN NAME	CONNECTION
1	Input	Connect to 9V or 12V source
2	Ground	Connect to GND
3	Output	Connect to VCC of circuit (+5V)

- **Test & Debug via Simulation**

Before physically building the circuit, simulate the setup in software like **Proteus**, **Multisim**, or **Tinkercad Circuits**.

- ✓ Verify timing accuracy,
- ✓ Check counter overflow,
- ✓ Ensure segment displays show 00 to 99 correctly.

7. CONCLUSION

This project successfully demonstrates the design and implementation of a basic digital stopwatch using only fundamental logic components—without any microcontroller. By integrating a 555 Timer for generating 1 Hz clock pulses, 7490 decade counters for pulse counting, and 7447 decoder ICs to drive 7-segment displays, we achieved a working digital stopwatch that counts from 00 to 99 seconds. This hands-on exercise strengthened the understanding of digital timing, counting, and display systems. Through careful pin configuration, cascading logic, and simulation verification, the project highlights how foundational components like counters and decoders can be combined to perform meaningful digital operations. Moreover, the use of a voltage regulator ensures stable operation, making the circuit both educational and practically reliable.