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Subject : Microprocessor Lab
Date : 7/1/2022

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BCD to 7 - Segment Decoder

Title : Experiment No 2.

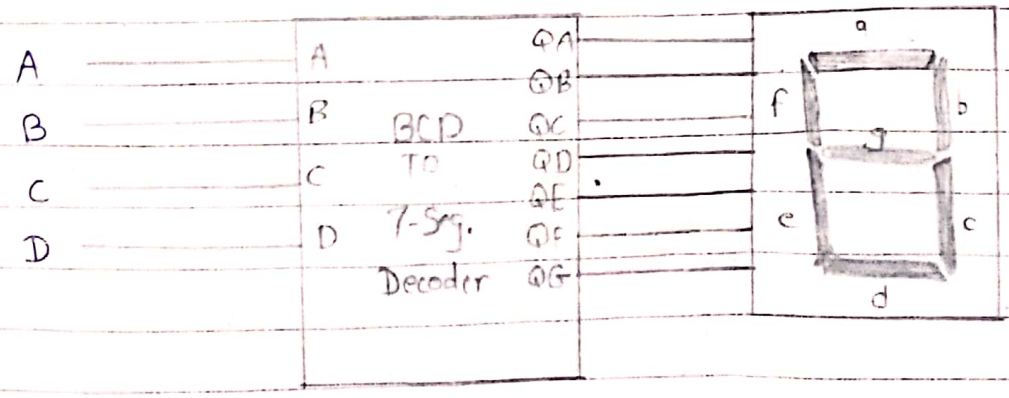
Aim : To design and implement BCD to 7 Segment decoder

Objective : Design and implement BCD to 7-Segment Decoder use K-Map to simplify the equation and common cathode 7 - segment display to perform experiment.

Platform : Proteus 8 professional Software.

Tools : AND gate, OR gate, NOT gate, LogicState, logicprobe, 7-Seg-com-cathode, 4511 (BCD to 7 segment decoder), Button, Logic Toggle.

Design :



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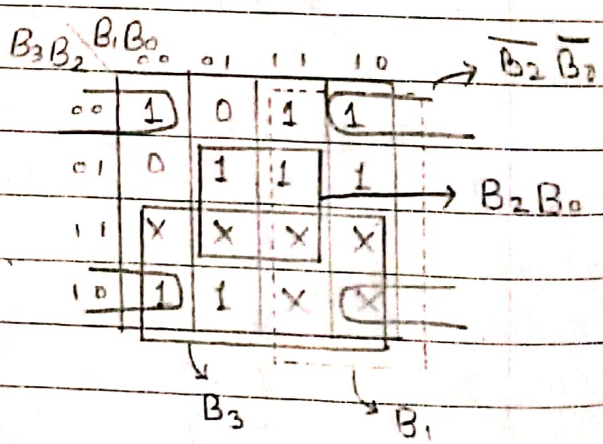
Truth Table :

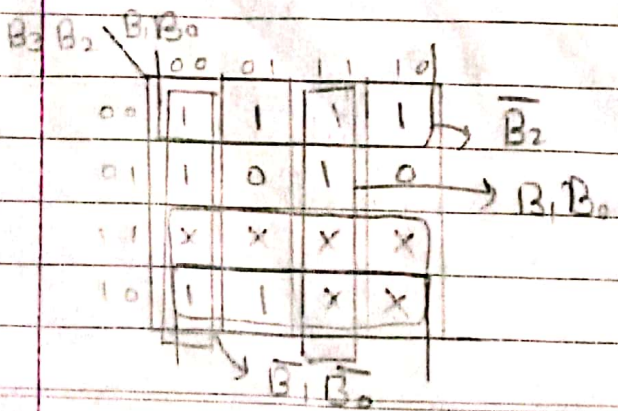
Decimal	BCD				Seven Segment						
	B_3	B_2	B_1	B_0	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

Calculations :

for a,

$$a = B_1 + B_3 + B_2B_0 + \overline{B_2}\,\overline{B_0}$$





for b,

$$b = \overline{B_2} + B_1B_0 + \overline{B_1}\,\overline{B_0}$$

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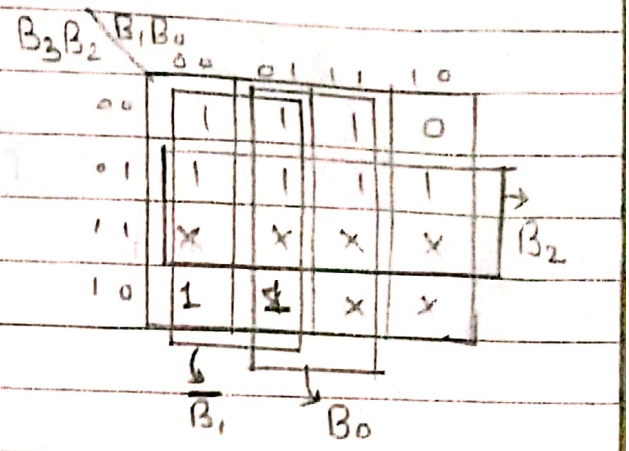
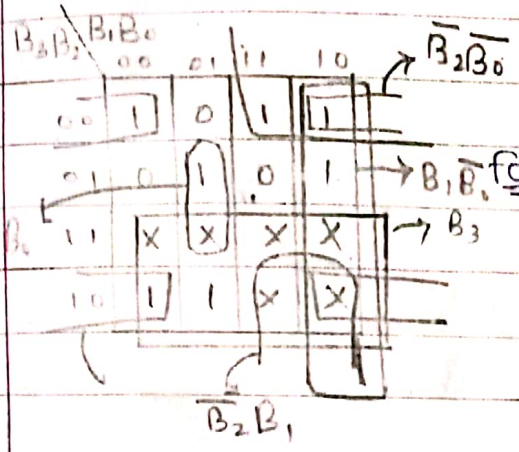
for c,



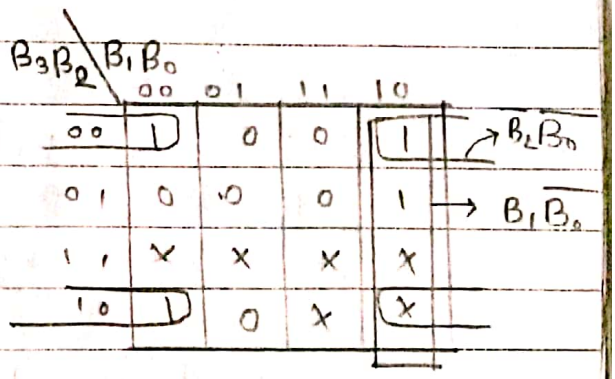
$$c = B_2 + \overline{B_1} + B_0$$



for d,

$$d = \overline{B_2}\,\overline{B_0} + B_1\overline{B_0} + B_2\overline{B_1}B_0 + \overline{B_2}B_1 + B_3$$

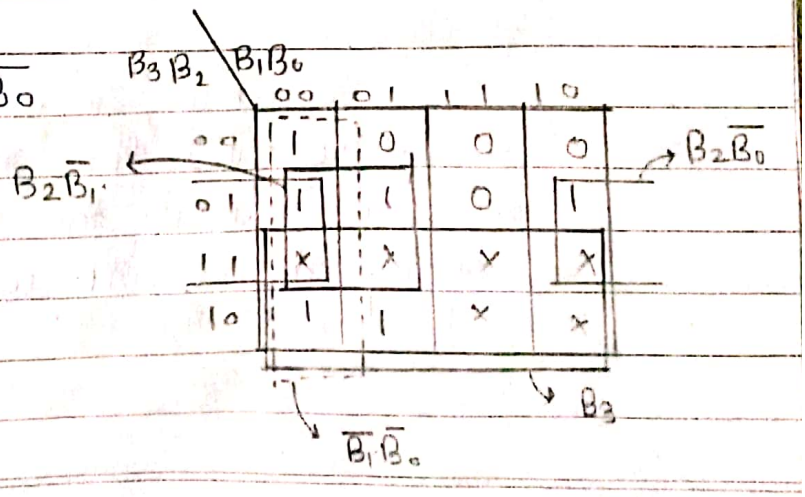
for e,



$$e = B_1\overline{B_0} + \overline{B_2}\,\overline{B_0}$$

for F,

$$f = B_2\overline{B_0} + B_3 + B_2\overline{B_1} + \overline{B_1}\,\overline{B_0}$$



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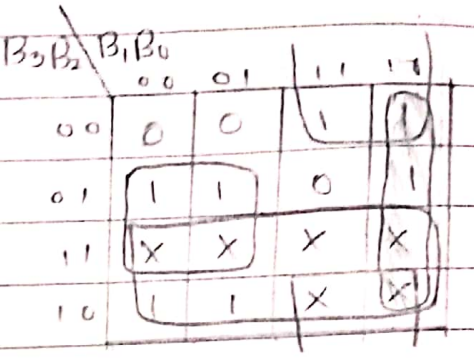
for g,

$g = \overline{B_2}B_1 + B_2\overline{B_1} + B_3 + B_1\overline{B_0}$



Result :

i) $a = B_3 + B_1 + B_2B_0 + \overline{B_2}\,\overline{B_0}$

$b = B_1B_0 + \overline{B_1}\,\overline{B_0} + \overline{B_2}$

$c = B_2 + \overline{B_1} + B_0$

$d = B_3 + \overline{B_2}\,\overline{B_0} + B_1\overline{B_0} + B_2\overline{B_1}B_0 + \overline{B_2}B_1$

$e = B_1\overline{B_0} + \overline{B_2}\,\overline{B_0}$

$F = B_3 + B_2\overline{B_0} + B_2\overline{B_1} + \overline{B_1}\,\overline{B_0}$

$g = B_3 + \overline{B_2}B_1 + B_2\overline{B_1} + B_1\overline{B_0}$

ii) Truth table of BCD to 7 segment decoder is verified.

Conclusion :

We can design BCD to 7-Segment decoder using logic gates. The circuits operation can be understood through the truth table itself but after making the circuit we get visual representation and more clear idea about it. Also this circuit can be used as a timer.

Implementation :

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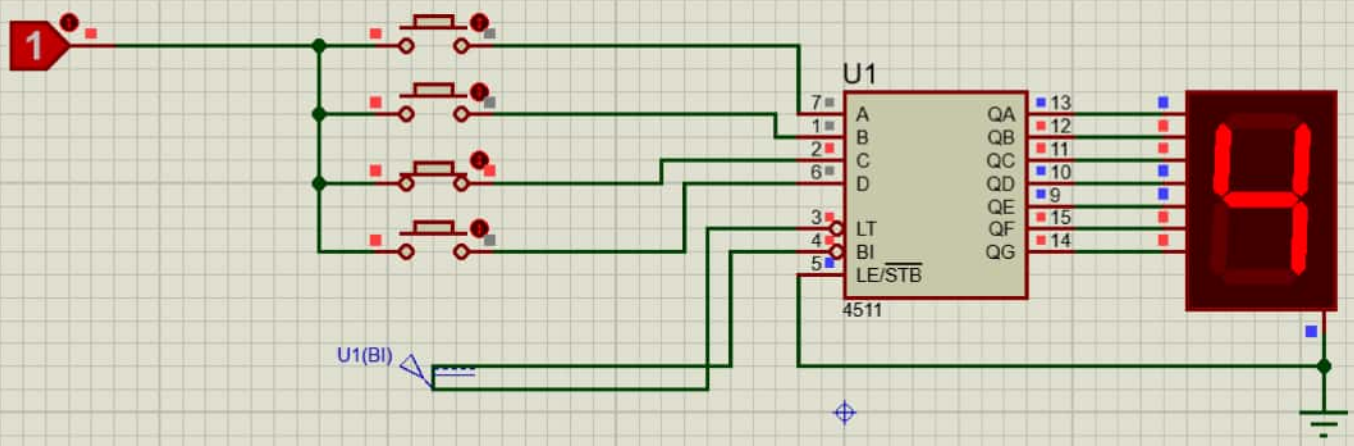

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