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STREAM- INFORMATION TECHNOLOGY

MAKAUT ROLL NO- 11200221003

SUBJECT- ANALOG & DIGITAL ELECTRONICS LAB

COLLEGE- GOVERNMENT COLLEGE OF ENGINEERING AND LEATHER TECHNOLOGY

SEMESTER- 3RD

SESSION- 2022-23

# EXPERIMENT NO. 4

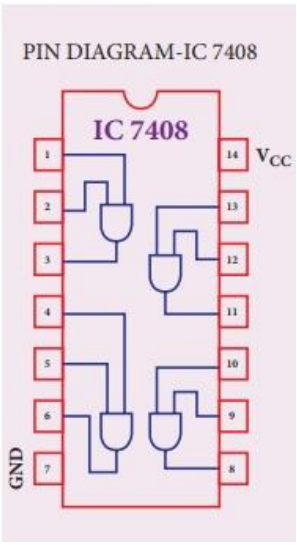
Design a 2-to-4 Line Decoder with Enable input using minimum number of basic gates.

## TRUTH TABLE

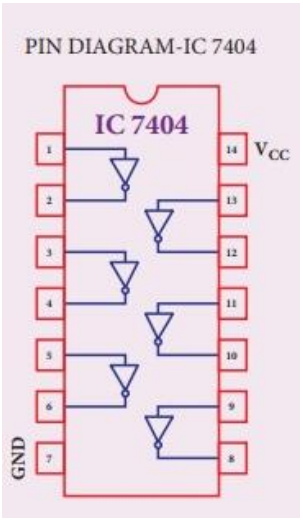
| $En$ | $w_1$ | $w_0$ | $y_0$ | $y_1$ | $y_2$ | $y_3$ |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | x | x | 0 | 0 | 0 | 0 |

## PIN DIAGRAM OF THE ICs USED

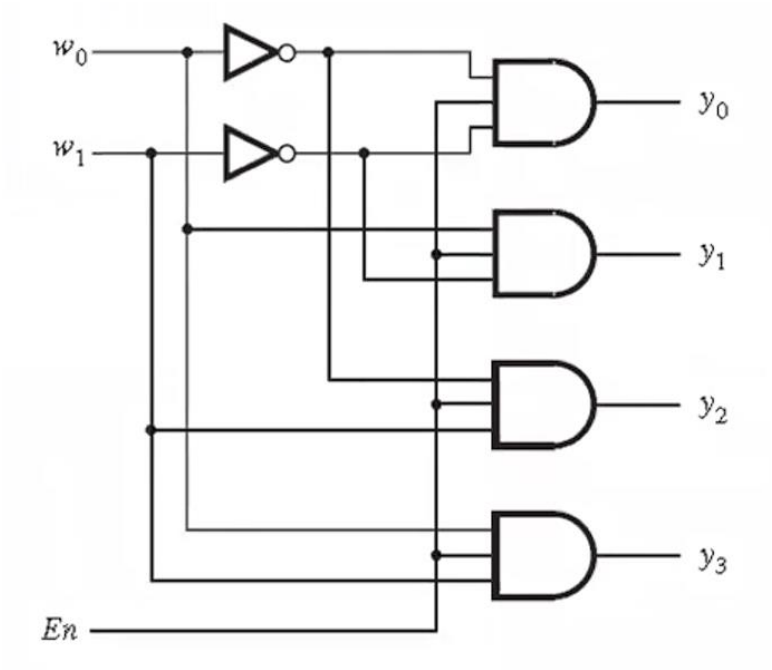
1) AND GATE



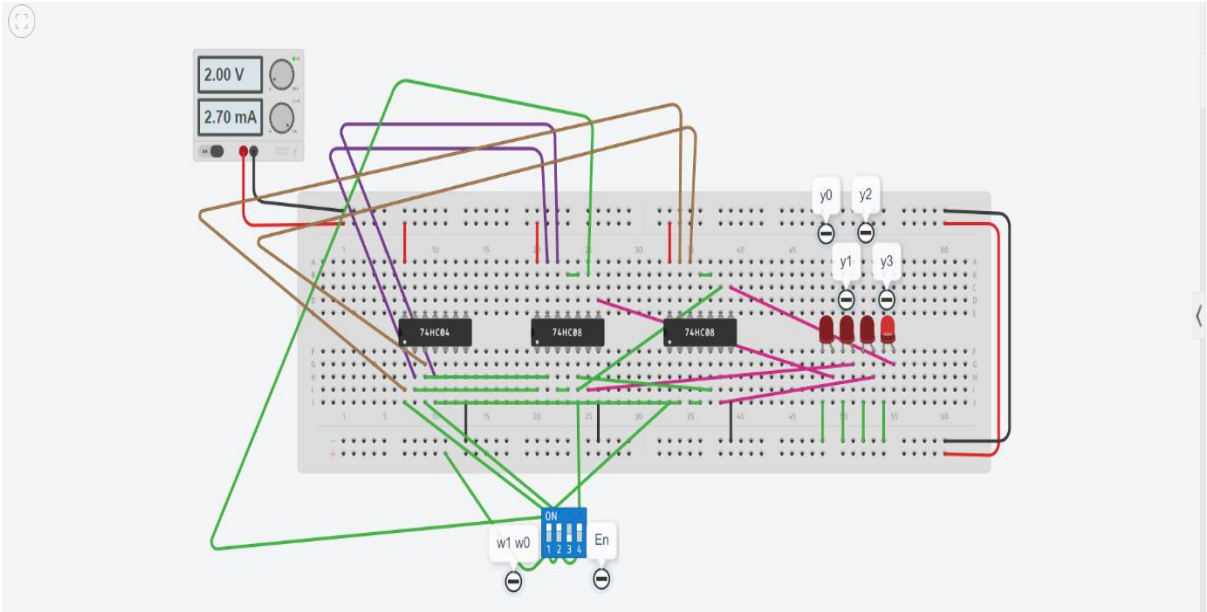

2) NOT GATE



## CIRCUIT DIAGRAM




## CONCLUSION



# EXPERIMENT NO. 5

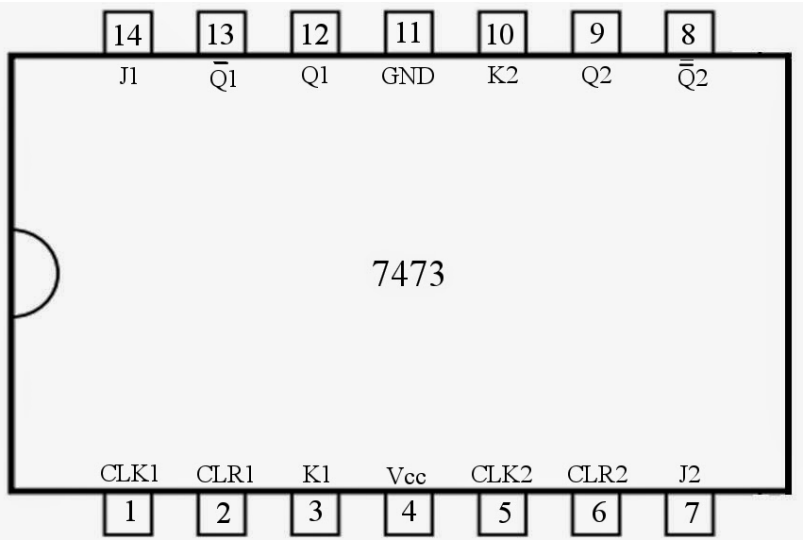
## Design a MODULO-4 Asynchronous up Counter (MOD-4 UP RIPPLE Counter).

## COUNTER STATE TABLE

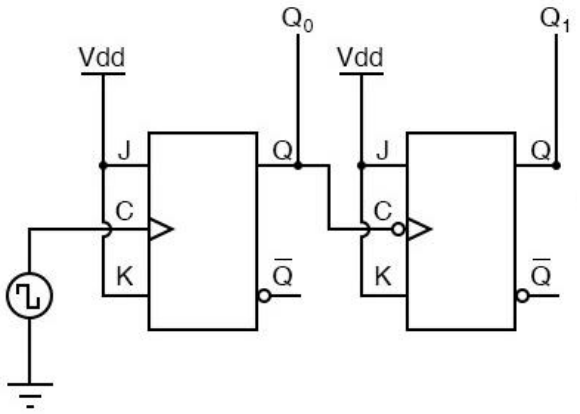
| Counter State | Q1 | Q0 |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| 3 | 1 | 1 |
| 0 | 0 | 0 |

## PIN DIAGRAM OF THE ICs USED

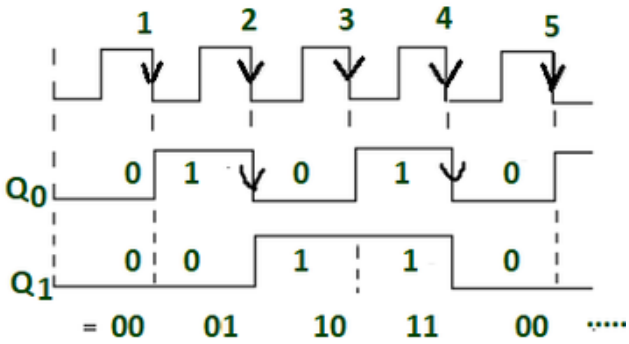
1) JK Flip Flop



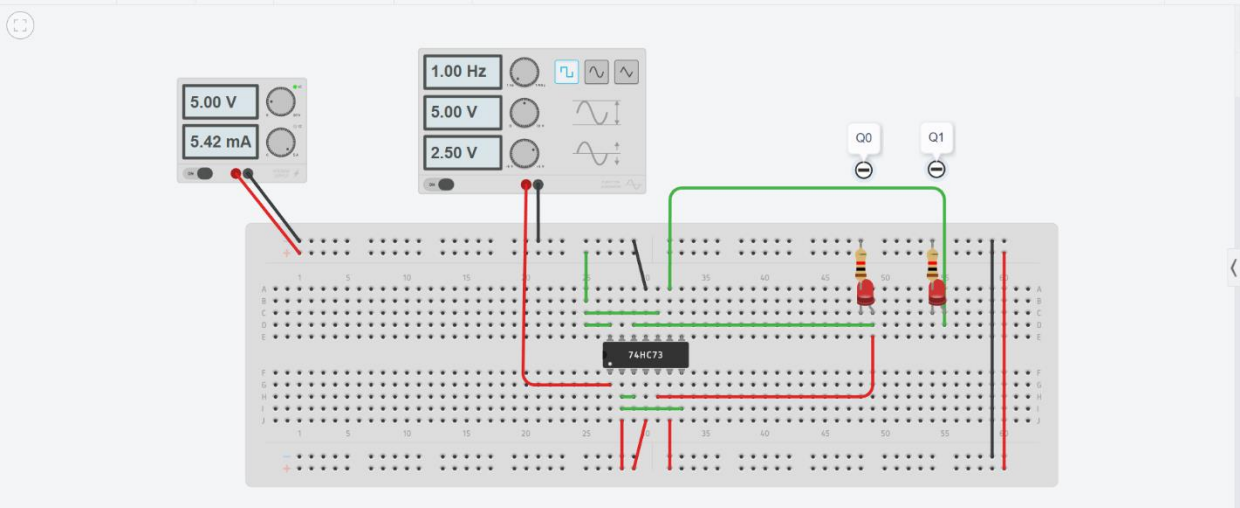
## CIRCUIT DIAGRAM




## TIMING DIAGRAM



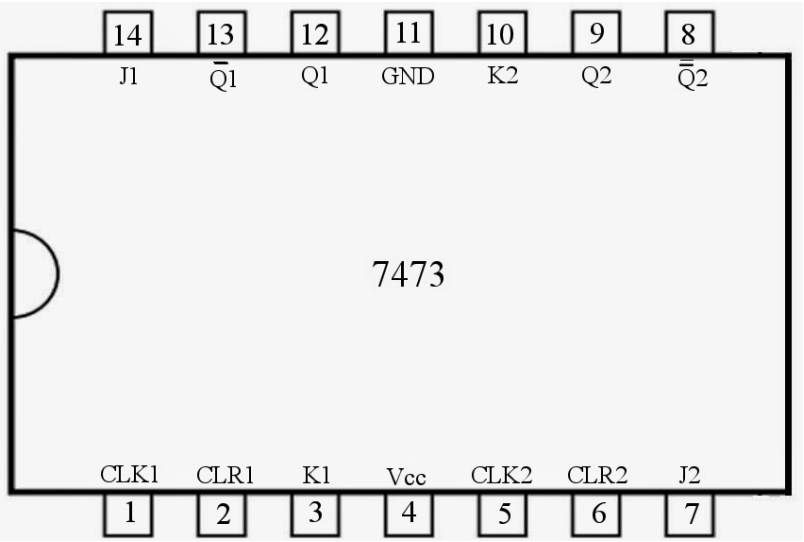

## CONCLUSION



# EXPERIMENT NO. 6

## Design a MODULO-3 Synchronous up Counter.

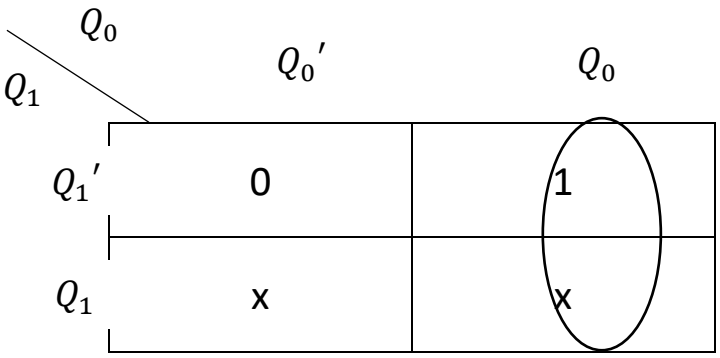
## Pin Diagram of JK Flip Flop (7473 IC)



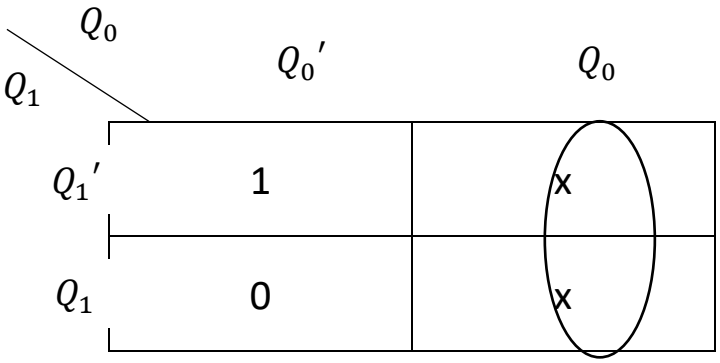

## Counter State Table

| Present State | | Next State | | Inputs | | | |
|---|---|---|---|---|---|---|---|
| $Q_1$ | $Q_0$ | $Q_1$ | $Q_0$ | $J_1$ | $K_1$ | $J_0$ | $K_0$ |
| 0 | 0 | 0 | 1 | 0 | x | 1 | x |
| 0 | 1 | 1 | 0 | 1 | x | x | 1 |
| 1 | 0 | 0 | 0 | x | 1 | 0 | x |

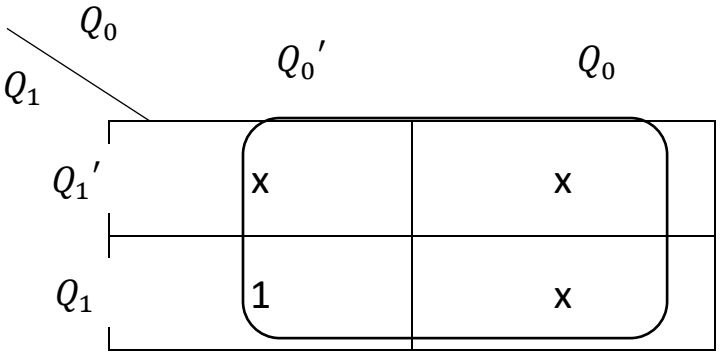
## Boolean Expression and K-map



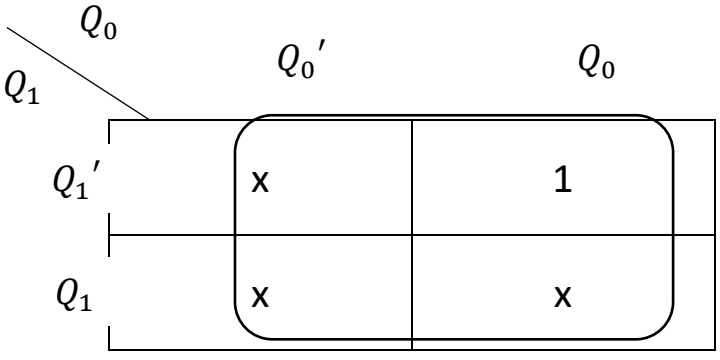

$J_1 = Q_0$




$J_0 = Q_1'$

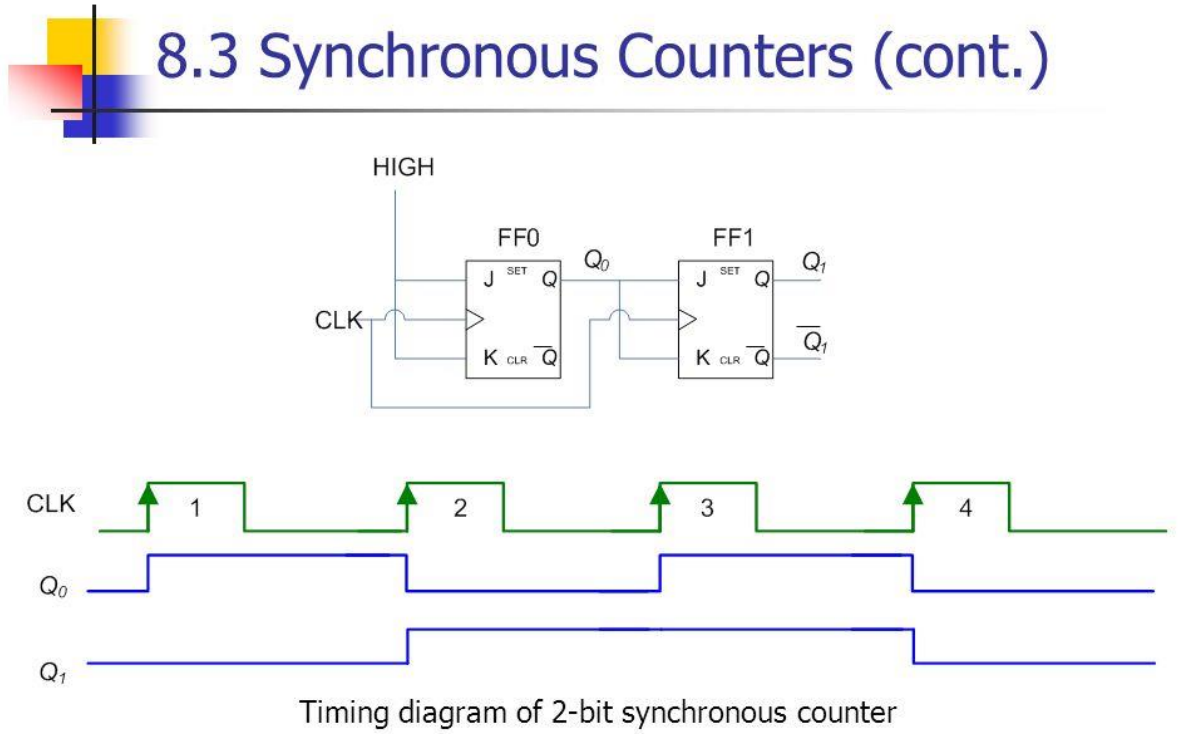



$K_1 = 1$




$K_0 = 1$

## Circuit Diagram and Timing Diagram




## CONCLUSION