Nondestructive Readout Memory Characteristics of Silicon Nanowire Biristors

Doohyeok Lim, Minsuk Kim, Yoonjoong Kim, Jinsun Cho, and Sangsig Kim

***Abstract*— In this paper, we demonstrate nondestructive readout memory characteristics of a bistable resistor (biristor) with an n^+-p-n^+ Si nanowire (SiNW) channel on a bendable substrate. The SiNW channel is fabricated using a top–down route, which is compatible with the current complementary metal-oxide-semiconductor technology. The SiNW biristor shows the outstanding memory characteristics such as a retention time of 10 s and a current sensing margin of ~23-μA at room temperature. These memory characteristics originate from a positive feedback process resulting from impact ionization near the p-n junction. Moreover, the positive feedback mechanism is comprehensively investigated using device simulation.**

***Index Terms*— Bistable resistor (biristor), capacitor-less, one-transistor dynamic random access memory (1T-DRAM), positive feedback, silicon nanowire (SiNW).**

I. Introduction

CONVENTIONAL one-transistor/one-capacitor dynamic random access memory (1T/1C DRAM) cells are reaching the limit of scaling down the capacitor. Recently, capacitor-less 1T-DRAM has been proposed as a next-generation type of DRAM owing to the absence of an external capacitor. Capacitor-less 1T-DRAM exploits the excess charge inside the floating body, which results in bistable current–voltage (I–V) characteristics [1]–[3]. 1T-DRAMs can be classified according to the method of generating the carriers. Okhonin *et al.* [4] proposed the metal-oxide-semiconductor field-effect transistor (MOSFET) operation mode with the floating body effect. In the MOSFET mode operation, impact ionization occurs, and excess holes exist in the floating body. More recently, the bipolar junction transistor (BJT) operation mode of capacitor-less 1T-DRAM was introduced [5]. The BJT operation mode significantly improves both data retention time and current sensing margin. However, both methods suffer from the gate oxide degradation caused by impact ionization.

Most previous studies on capacitor-less 1T-DRAM have been based on three-terminal devices that are modulated by a control terminal, such as a gate [6], [7]. Recently, a bistable resistor (biristor) was proposed for a two-terminal memory device, which prevents the gate dielectric degradation induced by hot carriers [8]–[13]. The biristor is equivalent to an open-base BJT or a gateless MOSFET. Moreover, the biristor is widely known to show bistable I–V characteristics such as a single-transistor latch [14] or open-base BJT [15]. Therefore, the biristor is preferred for long-term endurance compared to three-terminal 1T-DRAM devices. However, there is a concern about the readout characteristics owing to the recombination process from the gateless structure. The previously reported biristor based on silicon nanowires (SiNWs) shows the limited readout time [8]. Although the potential well in the SiNWs enables accumulation of the excess carriers, the state is unstable because there is no neutral region. Hence, we propose the biristor using a partially depleted SiNW in this paper, in order to enhance the readout characteristics. Our partially depleted SiNW enables a simple fabrication of the gateless structure unlike the complicated fabrication steps of SiNWs with silicon-on-insulator substrates. In addition, the SiNW can be simply transferred into bendable substrates [16]. Therefore, the development of biristors with partially depleted NWs has become an attractive research area. The electrical characteristics of a biristor realized on a bendable substrate with an n^+-p-n^+ partially depleted SiNW are investigated in this paper.

II. Experiment

A symmetrically doped n^+-p-n^+ SiNW was fabricated from a (100)-oriented p-type bulk-Si wafer with a resistivity of 5–10 $\Omega \cdot$cm using a fully CMOS-compatible top–down route. The Si trench was fabricated on a bulk-Si wafer through an anisotropic dry-etching process with the formation of SiO_2 and Si_3N_4 layers. The Si wafer was anisotropically etched in a tetramethylammonium hydroxide [TMAH, $(CH_3)_4NOH$] solution to form the inverted triangular SiNW. To dope the base regions of the SiNW, BF_2^+ ions with a dose of 8×10^{12} cm^{-2} were implanted as p-type dopants at ion energies of 15 keV via masked ion implantation. For the collector and emitter regions of the SiNW, heavily doped

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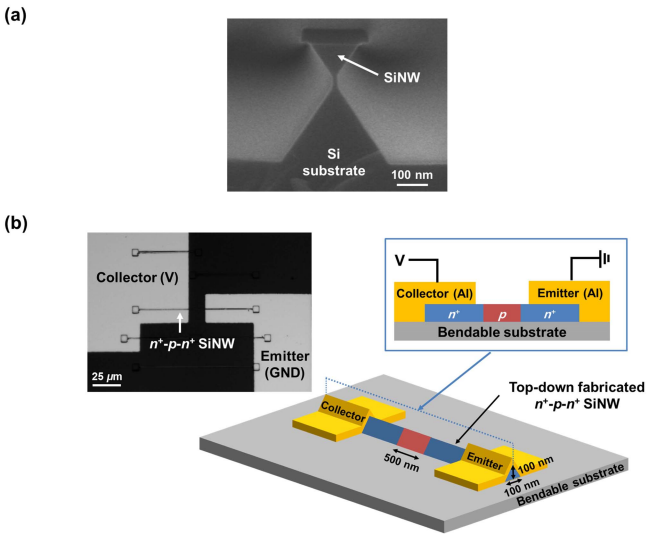

Fig. 1. (a) SEM image of a SiNW. (b) Optical microscope image and schematic of the bistable resistor.

n-regions were formed by ion implantations of As^+ ions at a dose of 5×10^{15} cm^{-2} at 80 keV. The wafer was first annealed at 900 °C for 60 min in nitrogen ambient and subsequently annealed at 1000 °C for 10 s in a rapid thermal annealing system to ensure that the implanted dopants had uniform diffusion. The fabricated SiNW was transferred into a polyethersulphone plastic substrate using a direct transfer method [17]. Aluminum collector and emitter electrodes were formed on top of the SiNW using photolithography and thermal evaporation.

All electrical measurements were carried out using a semiconductor-parameter analyzer (Agilent-HP4155C) and a system sourcemeter (Keithley-2636B) at room temperature ($T \approx 300$ K). The morphologies of the SiNW on a bulk-Si wafer were observed by scanning electron microscopy (SEM: S-4300, Hitachi) analysis.

III. Results and Discussion

Fig. 1(a) displays the cross-sectional SEM image of the n^+-p-n^+ SiNW on a bulk-Si substrate taken after crystallographic wet etching. The SiNW is formed during the crystallographic wet etching because the etch rate of the (111) plane is much slower than that of the (100) and (110) planes using the TMAH solution. The SiNW has an inverted triangular shape with a height and width of ~100 nm. The dimensions of the SiNW base are large enough to preserve the excess holes in the floating body. Schematic and optical microscope image of a SiNW biristor on a bendable substrate are shown in Fig. 1(b). A top–down fabricated n^+-p-n^+ SiNW with a p-region length of 500 nm is used as an active channel material to implement the biristor. The collector and emitter electrodes are connected to the collector voltage (V_C) and the ground potential (GND), respectively.

The basic operating principle of a positive feedback process in the SiNW biristor is depicted in Fig. 2. The positive feedback process is generated by impact ionization in the SiNW biristor. When V_C is high enough to trigger the impact ionization near the base–collector junction, it generates

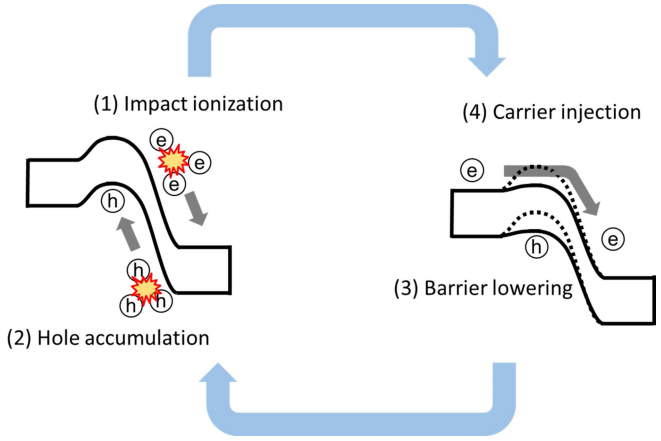

Fig. 2. Positive feedback processes generated by the impact ionization.

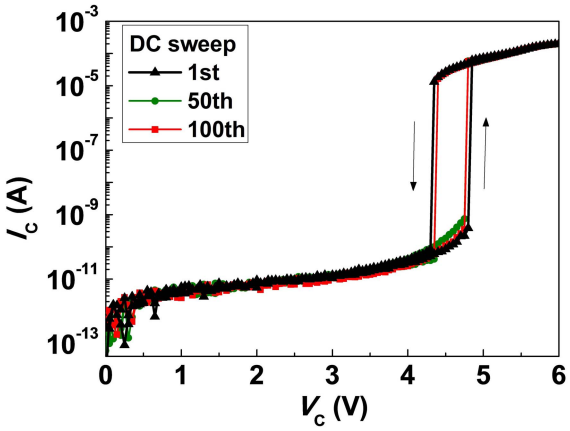

Fig. 3. Hysteric I–V characteristics of the biristor device.

electron/hole pairs. The created holes are accumulated in the floating p-type base region of the SiNW, and thereby lead to increased potential of the base region. Furthermore, the increased potential from the accumulation of holes induces a barrier reduction and provides more electrons for impact ionization. More generated holes injected into the base region result in further increase in the body potential, leading to the formation of the positive feedback process. The potential difference due to the hole accumulation drives the emitter-to-base p-n junction into forward bias. The emitter is a heavily doped n-type, so electrons can be injected from the emitter into the floating base region owing to the forward bias. A fraction of the injected electrons can diffuse across the base region into the collector under a reverse bias. Therefore, the collector current (I_C) is amplified from the current gain (β), multiplication factor (M), and base current (I_B) [15]; that is,

$$I_C = \frac{M \cdot \beta}{1 - (M - 1) \cdot \beta} I_B. \quad (1)$$

In this positive feedback process, instability appears as the denominator $1 - (M - 1) \cdot \beta$ approaches zero.

Fig. 3 shows the typical hysteric I–V characteristics of the biristor. As the collector voltage (V_C) is swept upward, I_C gradually increases. The positive feedback process then causes an abrupt increase in the current, which corresponds to the "latch-up" phenomenon, when the voltage level satisfies $(M - 1) \cdot \beta = 1$. In addition, the "latch-down" phenomenon,

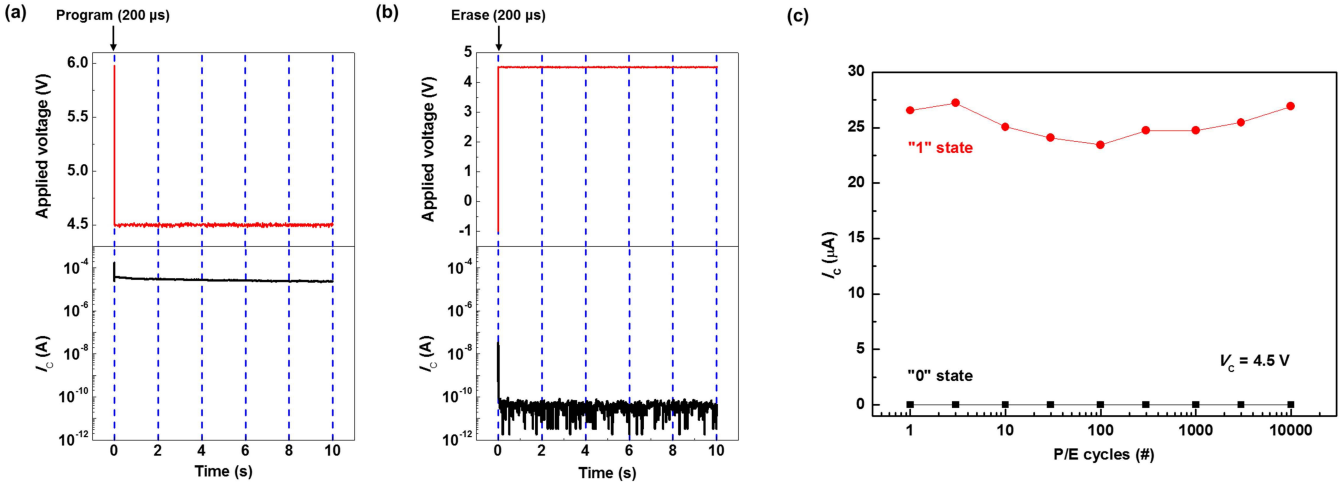

Fig. 4. (a) Retention characteristics of the biristor device in "1" state. The programming voltage is 6 V for 200 μs. The reading process is carried out to verify the change of the current at a fixed V_C of 4.5 V. (b) Retention characteristics in the "0" state. The erasing voltage is -1 V for 200 μs. In reading, V_C is set to 4.5 V. (c) Endurance characteristics as a function of the number of programming and erasing cycles.

the abrupt decrease in the current, is seen in Fig. 3 as V_C is downwardly swept. Therefore, counterclockwise hysteresis is observed in the experimental data, which also shows that the latch-up voltage (V_{up}) at a forward sweep is higher than the latch-down voltage (V_{down}) for a reverse sweep. The presence or absence of excess holes leads to different values of M and β, which are important parameters for the positive feedback process; thus, there are two latch voltages that satisfy $(M-1)\cdot\beta = 1$, i.e., V_{up} and V_{down}. This implies that the device does not turn OFF until the voltage drops below the value of V_{down}. Therefore, the device shows bistable I–V characteristics between $V_{\text{down}} = 4.35$ V and $V_{\text{up}} = 4.80$ V, which can be utilized to read the "0" and "1" memory states. Furthermore, the uniform characteristics of the biristor with dc sweeping cycles are exhibited in Fig. 3. The data is collected from the 1st, 50th, and 100th I–V sweeps. The distribution of current depending on the voltage is relatively narrow, suggesting that high uniformities are achieved for the latch-up/down states. This indicates that the generation and elimination of the positive feedback loop in the SiNW biristor are clear under the appropriate voltages. Thus, our SiNW biristor exhibits the excellent uniformity in the operational voltages for memory applications.

Next, we demonstrate the memory characteristics of our biristor. Fig. 4 shows the read retention and endurance characteristics at room temperature. To program, impact ionization is introduced to generate excess holes for the positive feedback process; thus, 6 V is applied to V_C for 200 μs, as shown in Fig. 4(a). In the erase operation, the recombination is used to remove the excess holes in the base region at $V_C = -1$ V for 200 μs in Fig. 4(b). After programming/erasing operations, the reading process is performed by sensing the difference in current at $V_C = 4.5$ V. Modern pulse generators, which provide a pulsewidth of a few nanoseconds, cannot offer constant voltage owing to the limitation of the total sampling amount. Accordingly, a pulsewidth of 200 μs is exploited to obtain the long read retention characteristics using the system sourcemeter (Keithley-2636B). The experimental result shows that the "1" and "0" states stably persist until 10 s with the current sensing margin of $\sim$23 μA. This indicates that the generation of the positive feedback loop remains in the read "1" state. The accumulated holes, which are generated by the program operation, sustain the positive feedback loop at the read voltage. In the read "0" state, the holes are not enough to form the positive feedback loop because of the recombination process by the erase operation. Therefore, the positive feedback loop is not generated or eliminated without the program/erase operations at the read voltage. Whereas conventional 1T/1C DRAM requires limited reading times below 1 ms [18], our device shows nondestructive reading characteristics. In addition, the device exhibits a very high sensing current margin, which does not need a sense amplifier to identify the data state. To evaluate the reliability for the SiNW biristors, endurance examination was performed, as shown in Fig. 4(c). During the endurance test, the programming voltage of 6 V and the erasing voltage of -1 V are applied for 200 μs. The reading process is also carried out to verify the change of the current for a V_C of 4.5 V. The current sensing margin is well maintained, even after 10^4-cycle P/E operations. The biristor shows the reliable endurance characteristics, which is free from the oxide degradation caused by impact ionization.

A simulation was carried out with a 2-D structure using a device simulator (Silvaco Atlas, version 5.20.2.R) to elucidate the operating mechanism [19]. The dimensional parameters are similar to those of the experimental device. In addition, the models used in Atlas device simulation tool include the concentration dependent Shockley-Read-Hall model, parallel electric-field-dependent mobility model, Kane band-to-band tunneling model, band gap narrowing, energy balance model, and Toyabe impact ionization model. Fig. 5(a) shows the simulation results for the contour plot of the impact ionization rate in the write "1" state. The peak of the impact ionization rate is near the base–collector junction. The energy band diagrams in the read "1" and read "0" states are depicted in Fig. 5(b). In the read "0" state, the electrons cannot inject

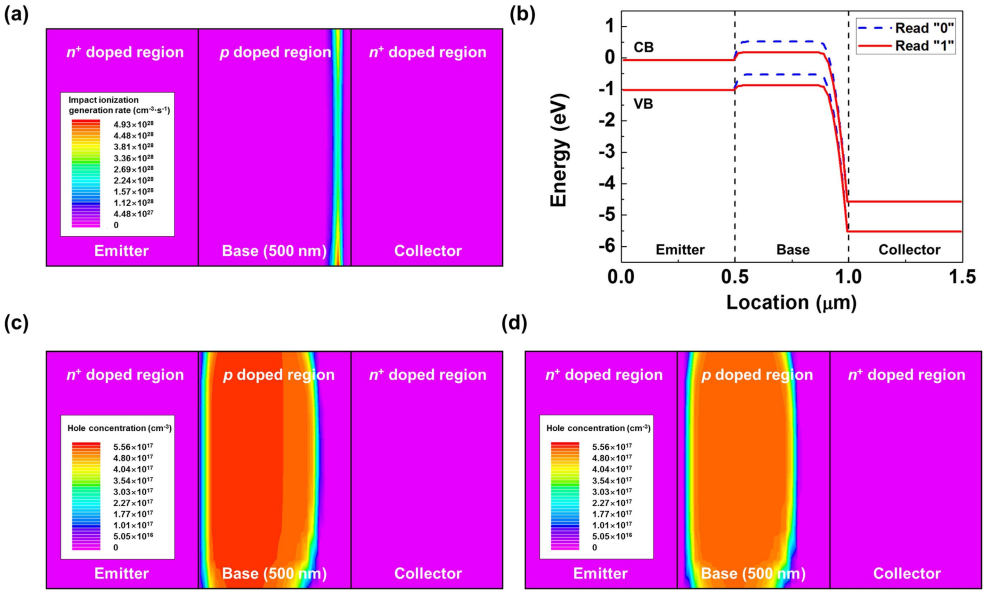

Fig. 5. Simulation results of the biristor using a device simulator. (a) Contour plot of the impact ionization rate in the write "1" state (V_C = 6 V). (b) Energy band diagram in the read states (V_C = 4.5 V). Contour of hole concentrations in (c) read "1" state and (d) read "0" state (V_C = 4.5 V).

toward the collector owing to the height of the potential barrier in the base region. However, they can be injected to the collector through the lowering of the potential barrier in the read "1" state. The potential barrier height is controlled by the excess holes in the base region. The simulated contour plots of hole concentrations in the two different states are shown in Fig. 5(c) and (d). After the programming, the excess holes generated by impact ionization in the base region persist during the reading process. However, the hole concentration is relatively similar to the original doping concentration in the read "0" state; thus, the device provides nondestructive reading characteristics.

To further investigate the operation speed of the biristors, computer simulations were conducted depending on the program/erase pulse widths. As presented in Fig. 6, the simulation result shows that the operation speed of 200 μs provides the retention time of 10 s, which is comparable to the experimental results. Moreover, the programming/erasing voltages are applied with different pulse times ranging from 200 μs to 5 ns. Although the programming and erasing times get shorter, the biristor shows the nondestructive readout memory characteristics with a high current sensing margin.

Table I shows the comparison between the memory characteristics of the biristor and the conventional 1T/1C DRAM. The program/erase speed of the biristor is 5 ns, which is comparable to the conventional 1T/1C DRAM (<10 ns). However, the leakage power of the biristor is higher than that of the conventional 1T/1C DRAM due to the high operation voltage. It is inevitable that we experimentally demonstrate the functionality of the memory characteristics at a relatively high operation voltage owing to the physical limitation of our photolithography equipment. The further base length scale-down leads to the reduction in the operation voltage [20]. As long as the length of the base region is scaled down, the biristor can overcome the concerns about the power consumption.

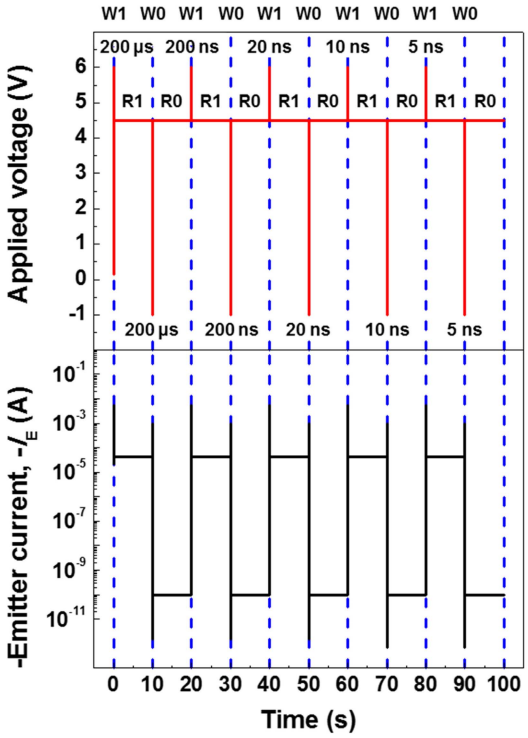

Fig. 6. Simulated timing diagrams of the biristor operation.

The mechanical bendability of our SiNW biristor on the bendable substrate is investigated. To evaluate the flexible properties of our SiNW biristor, we investigate the electrical characteristics while the device is in various bent states. The bending test is performed by bending the bendable substrate mechanically along the channel transport direction to achieve the tensile and compressive surface states. The applied strain of 0.6% is obtained by the following expression:

$$\text{Strain}(\%) = 100 \times \frac{t_{\text{substrate}} + R_{\text{SiNW}}}{2 \times R_c} \quad (2)$$

TABLE I
COMPARISON OF THE MEMORY PERFORMANCE

	Program/erase speed	Leakage power
Conventional 1T/1C DRAM	< 10 ns	0.005 pJ
This work (biristor)	5 ns	382.5 pJ

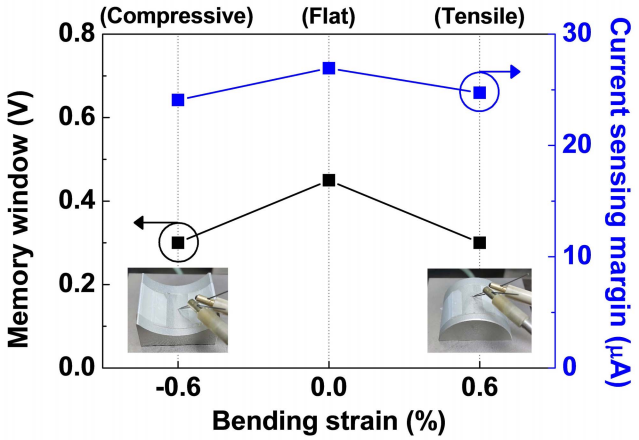

Fig. 7. Variation in the memory characteristics of the biristor under strains of ±0.6%. Inset: optical images of the downwardly and upwardly bent devices on a bending stage.

where the substrate thickness ($t_{\text{substrate}}$), the radius of the SiNW (R_{SiNW}), and the radius of curvature (R_c) are 200 μm, 150 nm, and 18 mm, respectively [21]. Fig. 7 shows the variations in the memory characteristics of the SiNW biristor in the flat- and bent-substrate states. Compared to the flat state, the memory window and the current sensing margin in the upwardly and downwardly bent states are slightly degraded. The tensile and compressive strain would have an influence on the positive feedback loop. The tensile and compressive strains lead to band splitting and suppression of hole accumulation in the base region [22]. The suppression of hole accumulation affects the feedback amplification mechanism and changes the memory characteristics. In spite of the strain effect on the positive feedback loop, our SiNW biristor in the bent state has no problem with the memory performance.

IV. CONCLUSION

We demonstrate the memory characteristics of a CMOS-compatible biristor with an n^+-p-n^+ SiNW channel on a bendable substrate. The bistable current–voltage characteristics are achieved by the positive feedback process. Our biristor exhibits the excellent memory characteristics, including a retention time of 10 s with a current sensing margin of ~23 μA. The nondestructive reading characteristics with a very high sensing margin indicate that the biristor can overcome the limited reading time of conventional 1T/1C DRAM. Furthermore, the two-terminal device structure enables a simple fabrication process and better reliability, which is free from oxide degradation by impact ionization. This paper demonstrates the promise of biristors for application in capacitor-less 1T-DRAM.

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