CPU

COPROCESSOR

DRAM CTRLR

32 MB DRAM

FLASH

SRAM

WAIT STATE

WAITIN	ADDW	WAIT STATES
ON	ON	4
ON	OFF	3
OFF	ON	3
OFF	OFF	2

DRAM CONFIGURATION JUMPERS

GRYPHON

mc68030 retrocomputer

CPU/Memory | Sheet 1 of 4 | Rev 1.0

Paul D. Fincato 2012-2014 | 22 August 2014 | B

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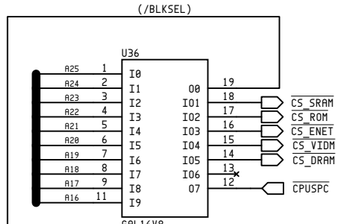
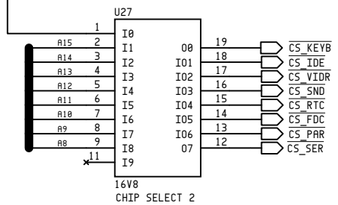
CHIP SELECT 1

```
GAL16V8
CSEL1.1

A25  A24       A23  A22        A21      A20      A19     A18     A17    GND
A16  /CPUSPC   NC   /CSDRAM   /CSVRAM  /CSENET  /CSROM  /CSRAM  /BLKSEL VCC


BLKSEL = CPUSPC * /A25 * /A24 * /A23 * /A22 * /A21 *  A20 * /A19 * /A18 * /A17 * /A16
CSROM  = CPUSPC * /A25 * /A24 * /A23 * /A22 * /A21 * /A20 * /A19
CSRAM  = CPUSPC * /A25 * /A24 * /A23 * /A22 * /A21 * /A20 *  A19
CSENET = CPUSPC * /A25 * /A24 * /A23 * /A22 * /A21 *  A20 * /A19 * /A18 * /A17 *  A16
CSVRAM = CPUSPC * /A25 * /A24 * /A23 * /A22 *  A21
CSDRAM = CPUSPC *  A25
```



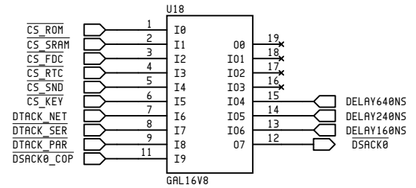
CHIP SELECT 2

```
GAL16V8
CSEL2.1

/BLKSEL A15    A14    A13    A12    A11    A10     A9      A8       GND
NC     /CSSER  /CSPAR /CSFDC /CSRTC /CSSND /CSVIDR /CSIDE  /CSKEYB  VCC


CSSER  =  BLKSEL * /A15 * /A14 * /A13 * /A12 * /A11 * /A10 * /A9 * /A8
CSPAR  =  BLKSEL * /A15 * /A14 * /A13 * /A12 * /A11 * /A10 * /A9 *  A8
CSFDC  =  BLKSEL * /A15 * /A14 * /A13 * /A12 * /A11 * /A10 *  A9 * /A8
CSRTC  =  BLKSEL * /A15 * /A14 * /A13 * /A12 * /A11 * /A10 *  A9 *  A8
CSSND  =  BLKSEL * /A15 * /A14 * /A13 * /A12 * /A11 *  A10 * /A9 * /A8
CSVIDR =  BLKSEL * /A15 * /A14 * /A13 * /A12 *  A11 * /A10 * /A9 * /A8
CSIDE  =  BLKSEL * /A15 * /A14 * /A13 * /A12 *  A11 * /A10 * /A9 *  A8
CSKEYB =  BLKSEL * /A15 * /A14 * /A13 * /A12 * /A11 *  A10 * /A9 *  A8
```



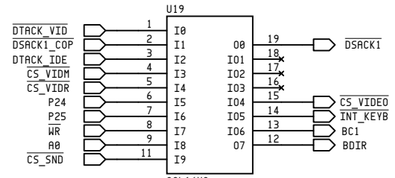
DSACK0 LOGIC

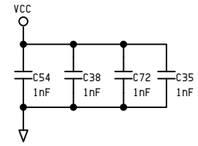
```
GAL16V8
DTACK0.1

/ROM   /RAM  /FDC  /RTC  /SND  /KEY  DSNET  /DSER /DPAR  GND
/DSCOP /DS0  DLA   DLB  DLC    /DA   /DB    NC    NC     VCC

DA  =  ROM * DLA
     + RAM * DLA
     + FDC * DLB
     + RTC * DLC
     + SND * DLC
     + KEY * DLC
     + /DSNET

DB  = DSER
    + DPAR
    + DSCOP

DS0 = DA + DB
```



DSACK1 / MISC DECODE

```
GAL16V8
DTACK1.1

/DVID  /DCOP DIDE  /CSVM  /CSVR  P24  P25  /WR  A0    GND
/CSSND /BDIR /BC1  /INTKB /CSVID NC   NC   NC  /DS1  VCC

DS1 =  DVID + DCOP + /DIDE ; DSACK1

CSVID = CSVM + CSVR        ; VIDEO

INTKB = P24 + P25          ; KEYB INT

BDIR = CSSND * WR          ; SOUND CS
BC1 =  CSSND * A0
```





MEMORY MAP

DEVICE	BASE ADDRESS HEX	SIZE (BYTES) DEC	HEX
ROM	00000000-0007FFFF	524288	00080000
SRAM	00080000-000FFFFF	524288	00080000
SERPORT	00100000-001000FF	256	00000100
PARPORT	00100100-001001FF	256	00000100
FDC	00100200-001002FF	256	00000100
RTC	00100300-001003FF	256	00000100
SOUND	00100400-001004FF	256	00000100
KEYBD	00100500-001005FF	256	00000100
---	00100600-001009FF		
VIDREG*	00100A00-00100AFF	256	00000100
IDE*	00100B00-00100BFF	256	00000100
---	00100C00-0010FFFF		
ETHNET	00110000-0011FFFF	65536	00010000
---	00120000-001FFFFF		
VIDRAM*	00200000-003FFFFF	2097152	00200000
---	00400000-01FFFFFF		
DRAM#	02000000-03FFFFFF	33554432	02000000
---	04000000-FFFFFFFF		

*16 bit device / #32 bit device

IDE is base address for drive 0
Drive 1 is base + 128

BYTE DECODE

```
GAL16V8
BDECD.1

A0 A1   SIZ0 SIZ1 RW   NC NC NC NC GND
NC /UUD /UMD /LMD /LLD NC NC NC NC VCC

UUD = RW + /A0 * /A1

UMD = RW
    + A0  * /A1
    + /A1 * /SIZ0
    + /A1 *  SIZ1

LMD = RW
    + /A0 * A1
    + /A1 * /SIZ0 * /SIZ1
    + /A1 *  SIZ0 *  SIZ1
    + /A1 *  A0   * /SIZ0

LLD = RW
    + A0    *  A1
    + A0    *  SIZ0 * SIZ1
    + /SIZ0 * /SIZ1
    + A1    *  SIZ1


DESCRIPTION:

Byte select logic on 32 bit bus
MC68030 User's manual section 12-13
Figure 12-7
```

DRAM INTERFACE

```
GAL16V8
DRMGLU.1

BCLK /CS    /AS NC /DTACK  NC  /ADDW  CLK    NC     GND
/OE  /STERM /DC NC /DB    /DA   NC   /ENCAS  /AREQ  VCC

AREQ  = /AS   * /CS *  CLK
        + /AREQ * /CS * /CLK

ENCAS = /AREQ * /CS * DC
        + /AREQ * /CS * /CLK

DC =  /AS * /CS * /DB * /CLK
      + /AS * /CS * /DC * CLK

STERM = /AS * /CS * /DA * DB * /CLK * /ADDW
      + /AS * /CS * /DTACK * DB * /CLK * ADDW
      + /STERM * CLK

DA.R  = /AREQ * /CS * /DTACK * DB * /ADDW

DB.R  = /AREQ * /CS * /DTACK * /DA * DB * /ADDW
      + /AREQ * /CS * /DTACK * DB * ADDW


DESCRIPTION:

DP8422V DRAM Controller Interface logic
National Application Note AN-537
"Interfacing the DP8420A/21A/22A to the 68030 Microprocessor"
Page 3

PDF -
converted from National PLAN format
removed EXST from equations (External STERM)
```

COPROCESSOR DECODE

```
GAL16V8
COPRO.1

CLK  AS  FC2  FC1 FC0 A19 A18 A17 A16  GND
A15 /CS /CLKD A14 A13 NC  NC  NC  CPU  VCC

CS =  FC2 *  FC1 * FC0
   * /A19 * /A18 * A17 * /A16
   * /A15 * /A14 * A13
   * /CLK

   +  FC2 *  FC1 * FC0
   * /A19 * /A18 * A17 * /A16
   * /A15 * /A14 * A13
   * /AS

   +  FC2 *  FC1 * FC0
   * /A19 * /A18 * A17 * /A16
   * /A15 * /A14 * A13
   * /CLKD

CLKD = CLK

; PDF - added for peripheral chipselect1 logic
CPU = FC2 * FC1 * FC0


DESCRIPTION:

MC68882 chip select logic
MC68030 User's manual section 12-8
Figure 12-4
```

NOTES:

8422V PROGRAMMING

TI DP8422V Datasheet Ref. Page 9 section 3.2.2

Chip select access programming. Reset causes /DISRFSH to assert and FF to assert /ML.
The first write of CPU on boot MUST provide 8422 programming data with program word on address bus, asserting /CS_DRAM
Upon write completion FF will negate /ML and write cycle terminates via normal /STERM. 8422 will be ready for
normal operation.

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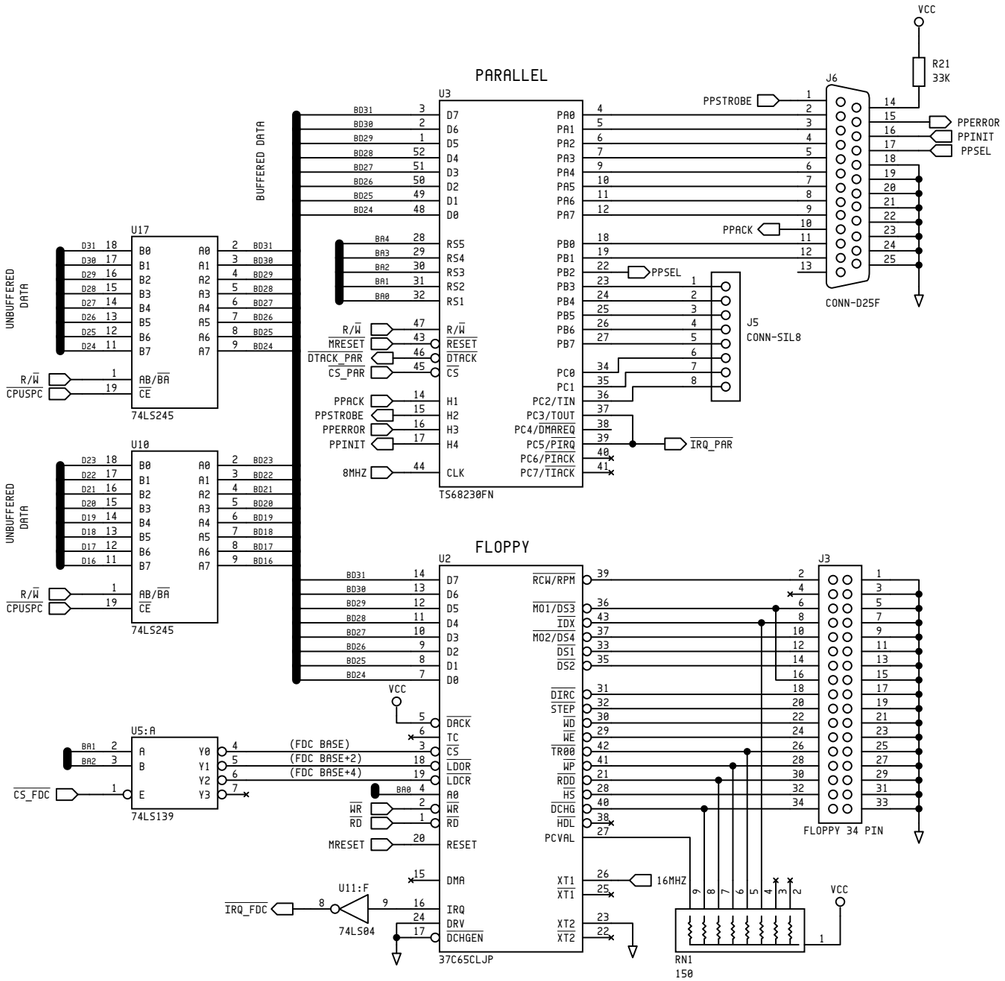
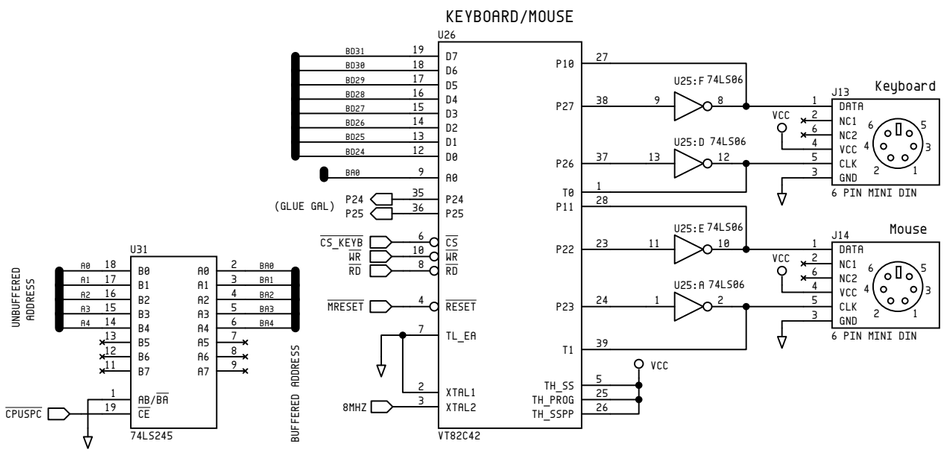
PARALLEL

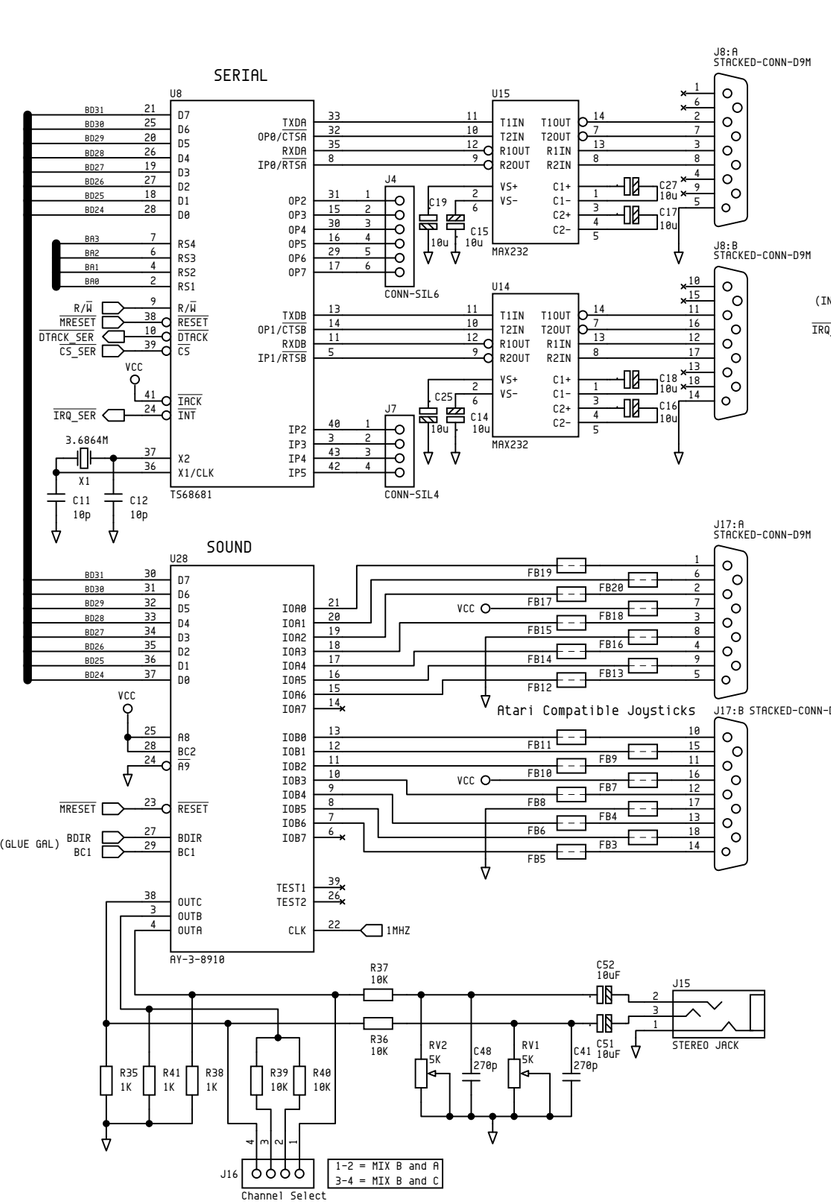


FLOPPY

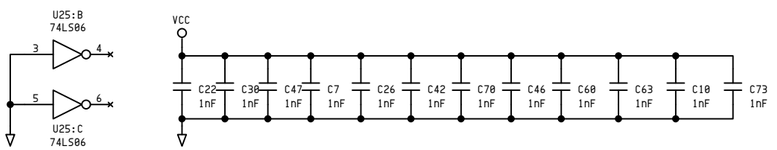
KEYBOARD/MOUSE



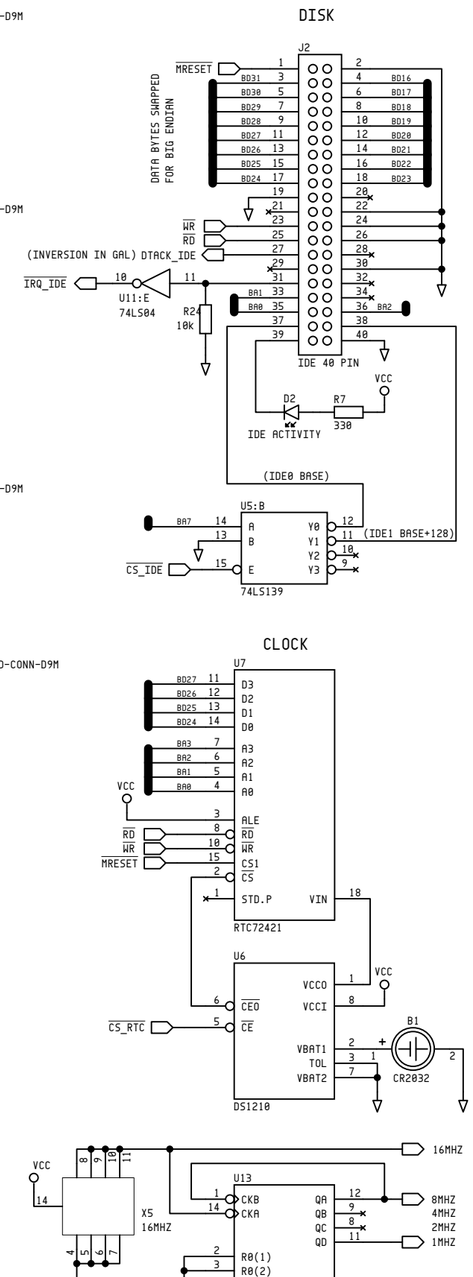
SERIAL



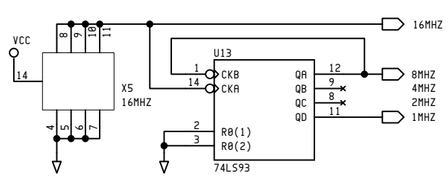
SOUND



DISK



CLOCK



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Peripherals	Sheet 3 of 4	Rev 1.0
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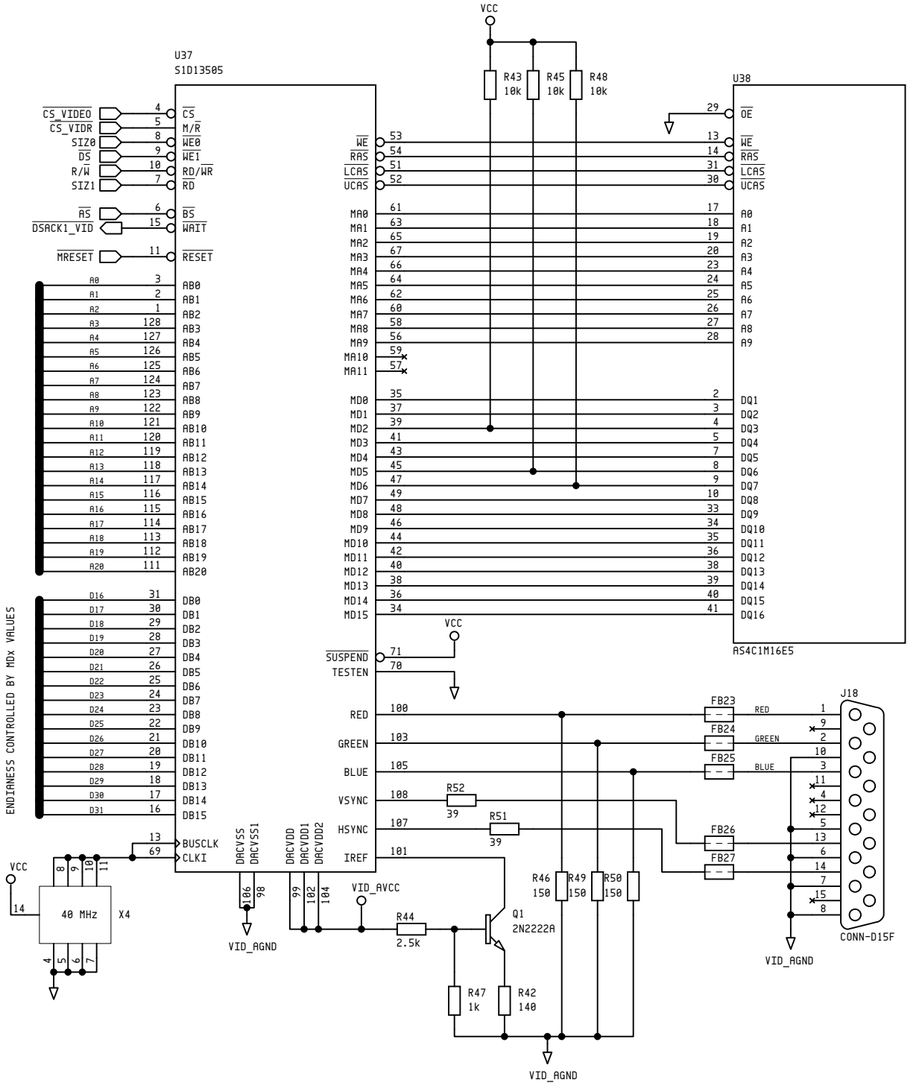
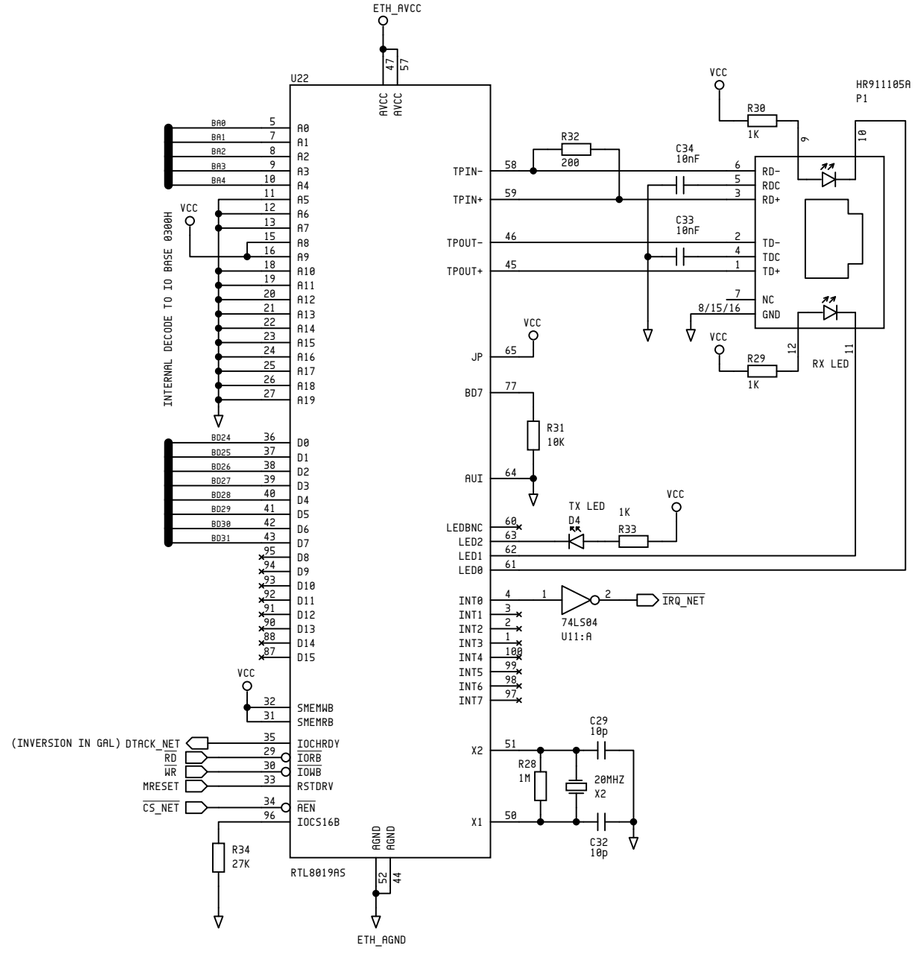
VIDEO



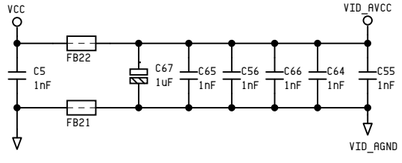
ETHERNET

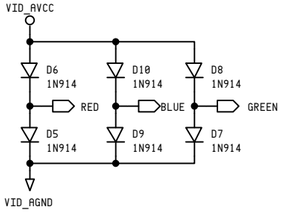


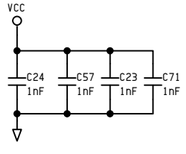
S1D13505 CONFIGURATION

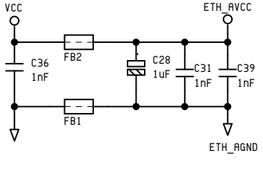
	16 BIT HOST	MC68K BUS2	MC68K BUS2	MC68K BUS2	BIG ENDIAN	WAIT# - WAIT HIGH	SYMMETRIC 1MB	SYMMETRIC 1MB		SUSPEND# INPUT	GPO POLARITY	PRIMARY BUS INTF	BUSCLK 1:1 CLK
MD	0	1	2	3	4	5	6	7	8	9	10	11	12
VALUE	0	0	(1)	0	0	(1)	(1)	0	X	0	0	0	0

0 = INTERNAL PULLDOWN









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