CHARUSAT
CHAROTAR UNIVERSITY OF SCIENCE AND TECHNOLOGY

MICROPROCESSOR ARCHITECTURES AND ASSEMBLY LANGUAGE PROGRAMMING

Chapter – 7

80286 Processor

DEPSTAR

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Intel family of microprocessor, bus and memory sizes

Microprocessor	Data bus width	Address bus width	Memory size
8086	16	20	1M
80186	16	20	1M
80286	**16**	**24**	**16M**
80386 DX	32	32	4G
80486	32	32	4G
Pentium 4 & core 2	64	40	1T

Features of 80286

- The Intel 80286 is a high-performance 16-bit microprocessor.
- It has been specially designed for multiuser and multitasking systems.
- Various versions of 80286 are available that run on 12.5 MHz,10 MHz and 8MHz clock frequencies.
- 80286 is upwardly compatible with 8086 in terms of instruction set.
- (That is the 8086,8088,80186,80286 CPU family all contain the same instruction set)

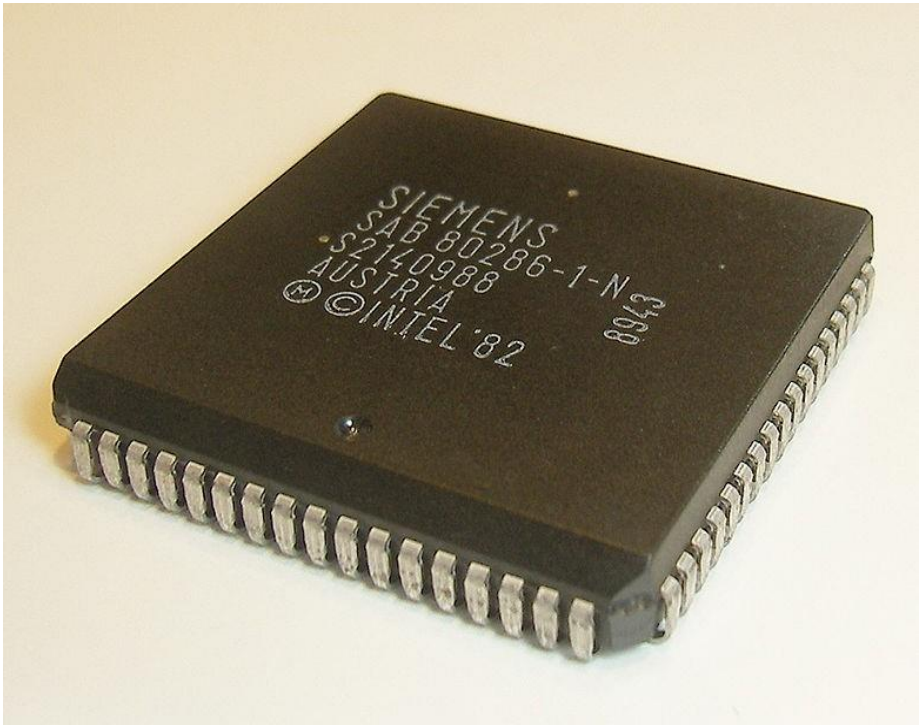
Features of 80286

- The memory management which is an important task of the operating system is now supported by a hardware unit called memory management unit.
- The 80286 is the first CPU to incorporate the integrated memory management unit.
- It has four-level memory protection and support for virtual memory and operating system
- It is available in variety of pin packages such as 68-pin PLCC (Plastic Leaded Chip Carrier), Ceramic LCC (Leadless Chip Carrier), and PGA(Pin Grid Array).

Features of 80286

- It has 24 address lines and 16 data lines.
- There are two operating modes for 80286
  - The real address mode
  - The protected virtual memory address mode
- In real address mode the processor can address up to 1MB of physical memory.
- The virtual address mode is for multiuser/multitasking system. In this mode of operation the memory management unit can manage up to 1GB of virtual memory.

- In virtual address mode one user cannot interface with the other. Also users cannot interface with operating system. These features are called protection.



- Intel 80286 has 2 operating modes.

1. Real address mode.
2. Protected Virtual address mode.

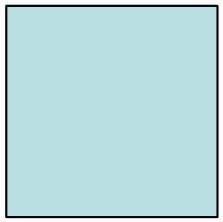
1.Real Address Mode :

- 80286 just act as a faster version of 8086
- And program for 8086 can be executed without modification in 80286

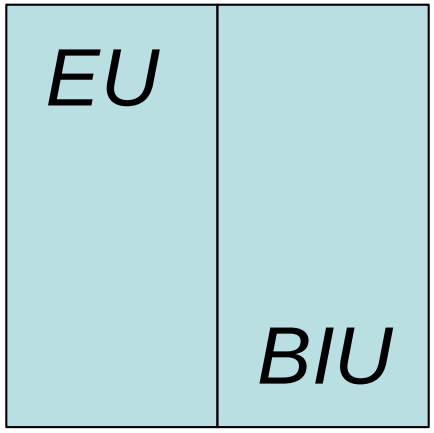
2.Protected Virtual Address Mode:

- 80286 supports multitasking
- Able to run several program at the same time
- Able to protect memory space for another program

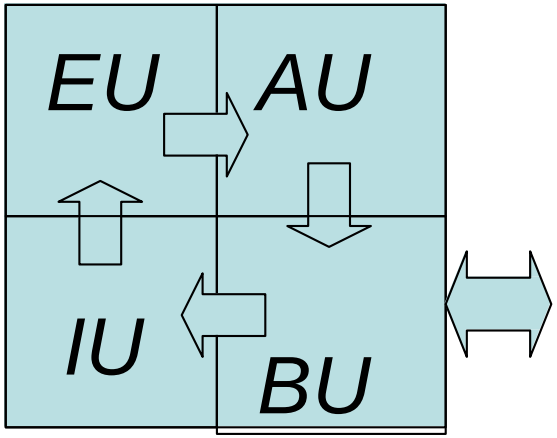
Architecture of 80286 Microprocessor



8085

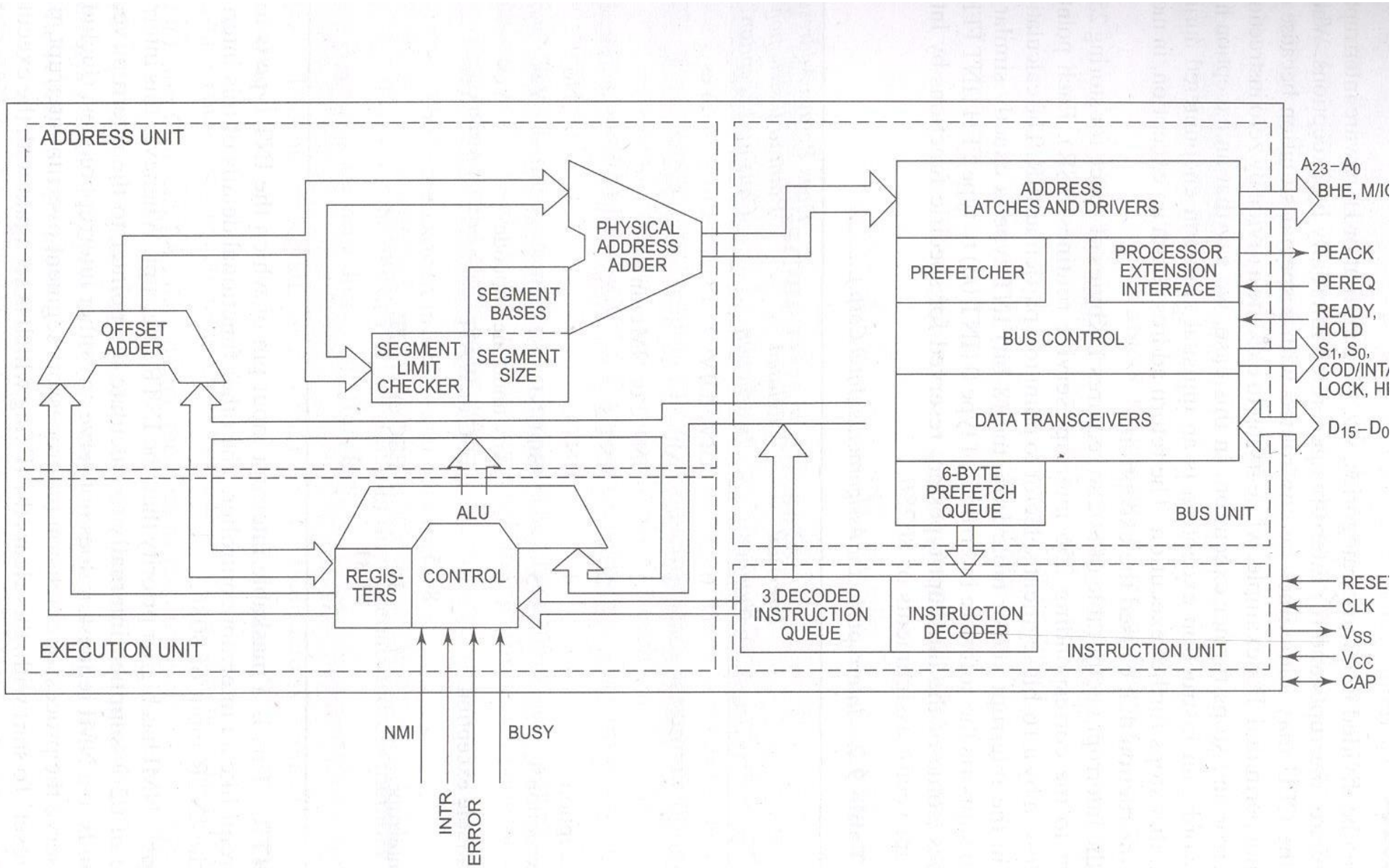


8086



80286

Architecture of 80286 Microprocessor



- The CPU, central processing unit of 80286 microprocessor, consists of 4 functional block:
  - Address Unit
  - Bus Unit
  - Instruction Unit
  - Execution Unit

Address Unit

- Calculate the physical addresses of the instruction and data that the CPU want to access
- Address lines derived by this unit may be used to address different peripherals.
- Physical address computed by the address unit is handed over to the BUS unit
- Once the execution of the instruction is performed then the result of the operation i.e., the desired data is send to the register bank through the data bus.

Bus Interface Unit

- Performs all memory and I/O read and write operations.
- Take care of communication between CPU and a coprocessor.
- Transmit the physical address over address bus A0 – A23.
- Prefetcher module in the bus unit performs this task of prefetching.
- Bus controller controls the prefetcher module.
- Fetched instructions are arranged in a 6 – byte prefetch queue.

Instruction Unit

- Receive arranged instructions from 6 byte prefetch queue.
- Instruction decoder decodes up to 3 prefetched instruction and are latched them onto a decoded instruction queue.

- Output of the decoding circuit drives a control circuit in the Execution unit.

Execution unit

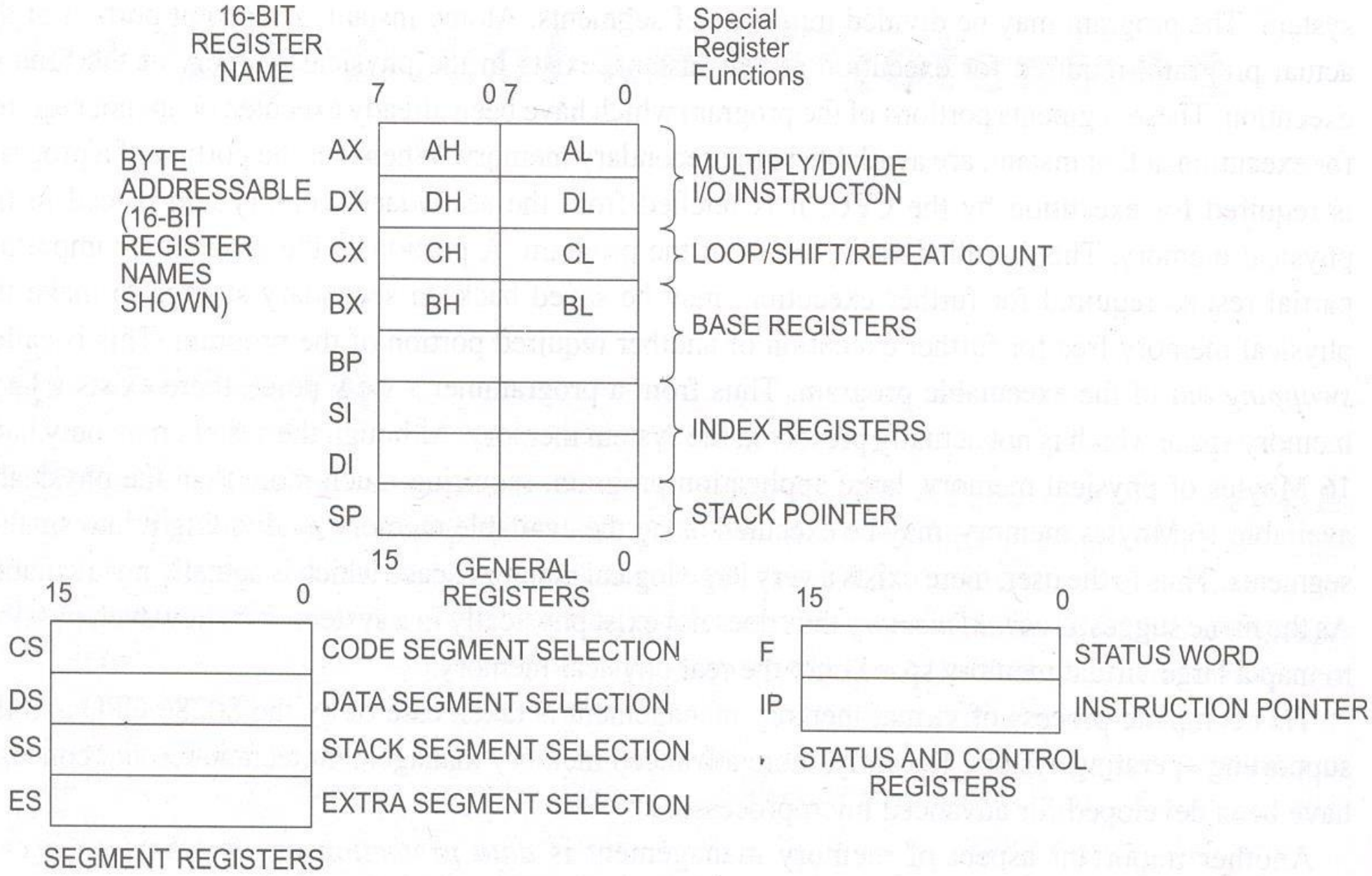
- EU executes the instructions received from the decoded instruction queue sequentially.
- Contains Register Bank.
- contains one additional special register called Machine status word (MSW) register --- lower 4 bits are only used.
- ALU is the heart of execution unit.
- After execution ALU sends the result either over data bus or back to the register bank.

Register organization of 80286

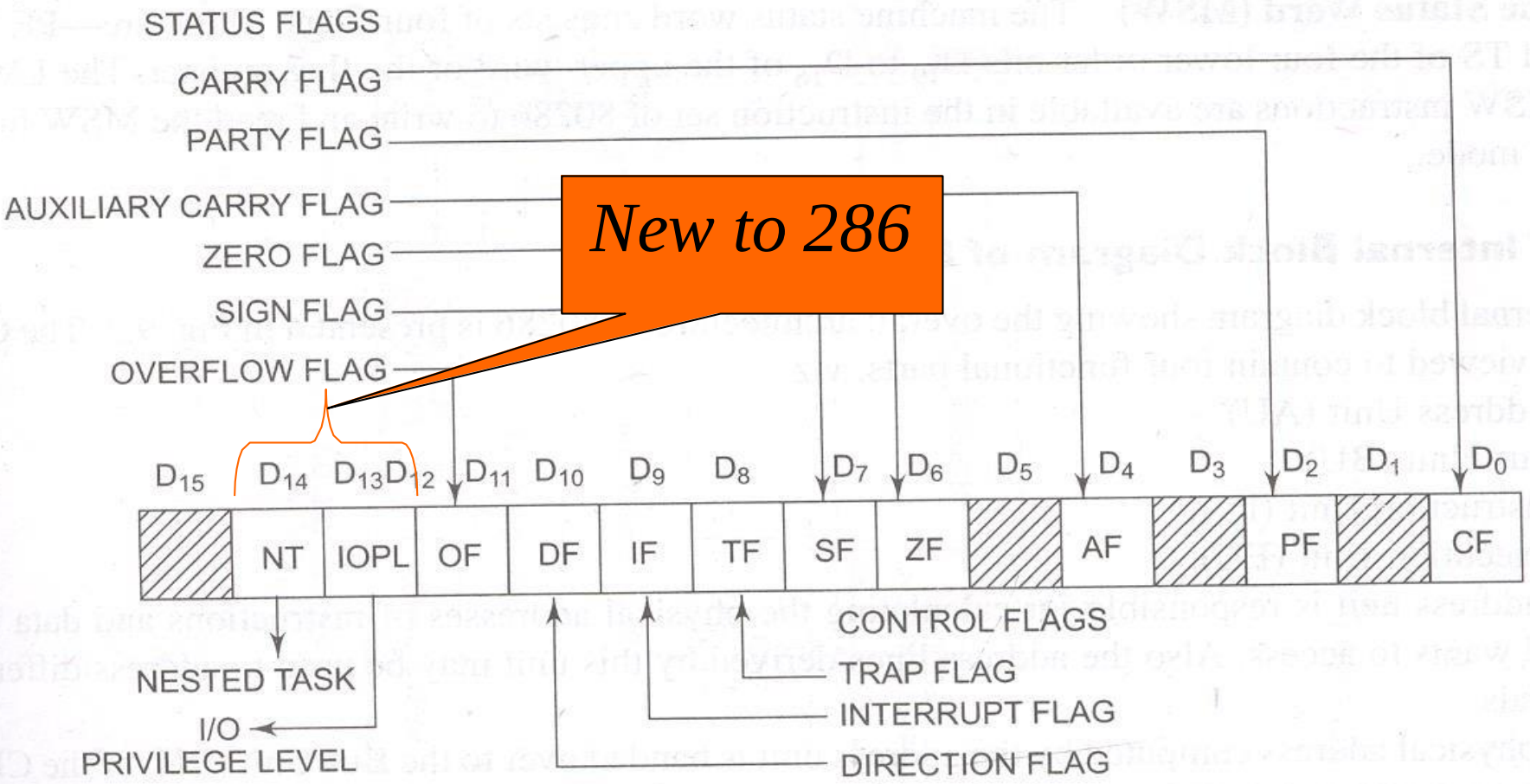
- The 80286 CPU contains the same set of registers, as in 8086.
  - Eight 16-bit general purpose registers.
  - Four 16 bit segment registers.
  - One Flag register.
  - One Instruction pointer.

    plus

- one new 16-bit machine status word (MSW) register


16-BIT REGISTER NAME
Special Register Functions
7 0 7 0
BYTE ADDRESSABLE (16-BIT REGISTER NAMES SHOWN)
AX AH AL
DX DH DL
CX CH CL
BX BH BL
BP
SI
DI
SP
MULTIPLY/DIVIDE I/O INSTRUCTON
LOOP/SHIFT/REPEAT COUNT
BASE REGISTERS
INDEX REGISTERS
STACK POINTER
15 0
GENERAL REGISTERS
15 0
CS CODE SEGMENT SELECTION
DS DATA SEGMENT SELECTION
SS STACK SEGMENT SELECTION
ES EXTRA SEGMENT SELECTION
SEGMENT REGISTERS
15 0
F STATUS WORD
IP INSTRUCTION POINTER
STATUS AND CONTROL REGISTERS

Flag Register



➢ IOPL – Input Output Privilege Level flags (bit D12 and D13)

- IOPL is used in protected mode operation to select the privilege level for I/O devices. If the current privilege level is higher or more trusted than the IOPL, I/O executed without hindrance.
- If the IOPL is lower than the current privilege level, an interrupt occurs, causing execution to suspend.
- Note that IPOL 00 is the highest or more trusted; and IOPL 11 is the lowest or least trusted.

➢ NT – Nested task flag (bit D14)

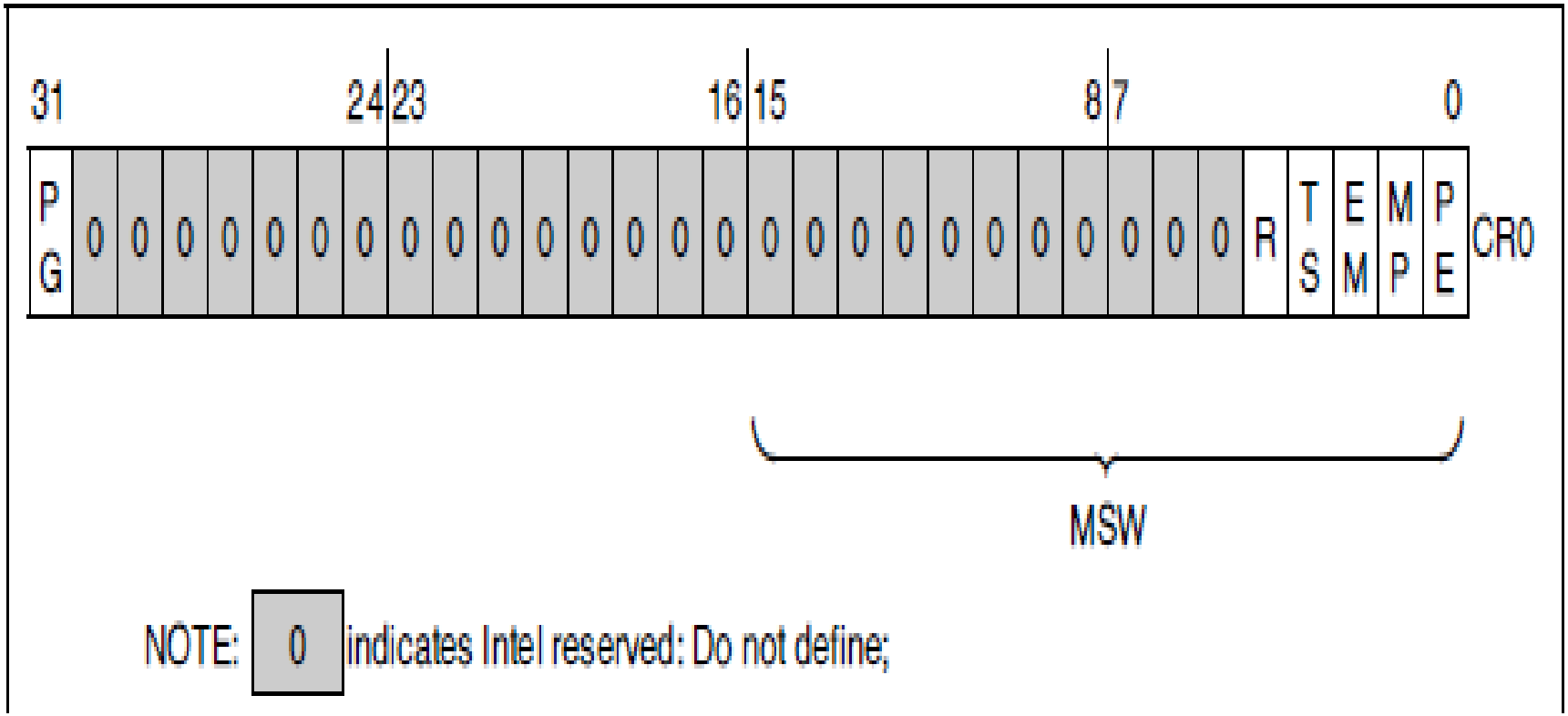
- When set, it indicates that one system task has invoked another through a CALL instruction .
- For multitasking this can be manipulated to our advantage

Machine Status Word Register

- Consist of four flags
  - Protection Enable
  - Monitor Processor Extension
  - Processor Extension Emulator
  - Task Switch

- LMSW & SMSW instruction are available in the instruction set of 80286 to write and read the MSW in real address mode.

Machine Status Word...



➢ PE - Protection enable

- Protection enable flag places the 80286 in protected mode, if set. this can only be cleared by resetting the CPU.
- Switches processor between protected and real mode

➢ MP – Monitor processor extension

- flag allows WAIT instruction to generate a processor extension.

➢ EM – Emulate processor extension flag,

- Indicates whether coprocessor functions are to be emulated
- if set , causes a processor extension absent exception and permits the emulation of processor extension by CPU.

➢ TS – Task switch

- if set, this flag indicates the next instruction using extension will generate exception 7, permitting the CPU to test whether the current processor extension is for current task.

80286
Memory Organization

- Same as 8086
- Uses odd and even banks

INSTRUCTION SET

- Same as 8086 with some additional instructions

Additional Instructions of Intel 80286

Sl no	Instruction	Purpose
1.	CLTS	Clear the task – switched bit
2.	LDGT	Load global descriptor table register
3.	SGDT	Store global descriptor table register
4.	LIDT	Load interrupt descriptor table register
5.	SIDT	Store interrupt descriptor table register
6.	LLDT	Load local descriptor table register
7.	SLDT	Store local descriptor table register
8.	LMSW	Load machine status register
9.	SMSW	Store machine status register

Sl no	Instruction	Purpose
10.	LAR	Load access rights
11.	LSL	Load segment limit
12.	SAR	Store access right
13.	ARPL	Adjust requested privilege level
14.	VERR	Verify a read access
15.	VERW	Verify a write access

CLTS

- The clear task – switched flag instruction clears the TS (Task - switched) flag bit to a logic 0.

LAR

- The load access rights Instruction reads the segment descriptor and place a copy of the access rights byte into a 16 bit register.

LSL

- The load segment limit instruction. Loads a user – specified register with the segment limit.

VERR

- The verify for read access instruction verifies that a segment can de read.

VERW

- The verify for write access instruction is used to verify that a segment can be written.

ARPL

- The Adjust request privilege level instruction is used to test a selector so that the privilege level of the requested selector is not violated.