

Date:

EXPERIMENT – 1**AIM:**

Study of logic gates (AND, OR, NOT, NAND, NOR, EX-OR) using ICs

APPARATUS:

Sr. No.	Component	Specification	Quantity
1	AND Gate	IC 7408	2
2	OR Gate	IC 7432	2
3	NOT Gate	IC 7404	2
4	Two input NAND Gate	IC7400	3
5	Three input NAND Gate	IC7410	2
6	NOR Gate	IC7402	3

SIMULATION WEBSITE: <https://www.tinkercad.com/>

THEORY:

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output.

OR, AND & NOT are basic gates. NAND, NOR, X-OR are known as universal gates. Basic gates can be obtained from all this gates.

AND Gate:

The AND gate performs a logical multiplication commonly known as AND function. The output is high only when both the inputs are either one high or one low. When both the inputs are high the output is low level.

OR Gate:

The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high and the output is low level when both the inputs are low.

NOT Gate:

The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high.

NAND Gate:

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any

one of the input is low. The output is low level when the inputs are high.



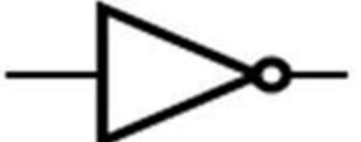



NOR Gate:

The NOR gate is contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

EX-OR Gate:

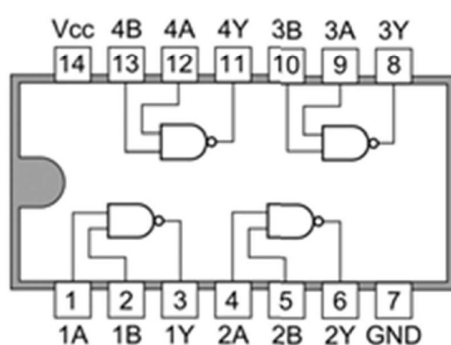
The output is high when any one of the input is high. The output is also low when both the inputs are low and both inputs are high.

Digital Logic Gate Symbols

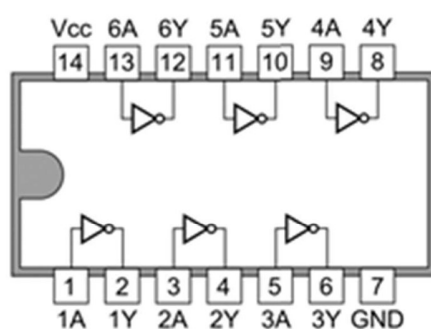
GATE	SYMBOL	NOTATION	TRUTH TABLE																		
<u>AND</u>		$A \cdot B$	<table><tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr><tr><th>A</th><th>B</th><th>A AND B</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	INPUT		OUTPUT	A	B	A AND B	0	0	0	0	1	0	1	0	0	1	1	1
INPUT		OUTPUT																			
A	B	A AND B																			
0	0	0																			
0	1	0																			
1	0	0																			
1	1	1																			
<u>OR</u>		$A + B$	<table><tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr><tr><th>A</th><th>B</th><th>A OR B</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	INPUT		OUTPUT	A	B	A OR B	0	0	0	0	1	1	1	0	1	1	1	1
INPUT		OUTPUT																			
A	B	A OR B																			
0	0	0																			
0	1	1																			
1	0	1																			
1	1	1																			
<u>NOT</u>		\overline{A}	<table><tr><th>INPUT</th><th>OUTPUT</th></tr><tr><th>A</th><th>NOT A</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table>	INPUT	OUTPUT	A	NOT A	0	1	1	0										
INPUT	OUTPUT																				
A	NOT A																				
0	1																				
1	0																				
<u>NAND</u>		$\overline{A \cdot B}$	<table><tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr><tr><th>A</th><th>B</th><th>A NAND B</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	INPUT		OUTPUT	A	B	A NAND B	0	0	1	0	1	1	1	0	1	1	1	0
INPUT		OUTPUT																			
A	B	A NAND B																			
0	0	1																			
0	1	1																			
1	0	1																			
1	1	0																			
<u>NOR</u>		$\overline{A + B}$	<table><tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr><tr><th>A</th><th>B</th><th>A NOR B</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	INPUT		OUTPUT	A	B	A NOR B	0	0	1	0	1	0	1	0	0	1	1	0
INPUT		OUTPUT																			
A	B	A NOR B																			
0	0	1																			
0	1	0																			
1	0	0																			
1	1	0																			
<u>XOR</u>		$A \oplus B$	<table><tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr><tr><th>A</th><th>B</th><th>A XOR B</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	INPUT		OUTPUT	A	B	A XOR B	0	0	0	0	1	1	1	0	1	1	1	0
INPUT		OUTPUT																			
A	B	A XOR B																			
0	0	0																			
0	1	1																			
1	0	1																			
1	1	0																			

LOGIC GATES USING IC:**IC's PIN DIAGRAMS:**

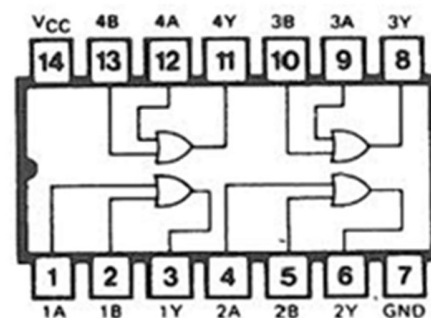
7400 Quad 2-input NAND Gates



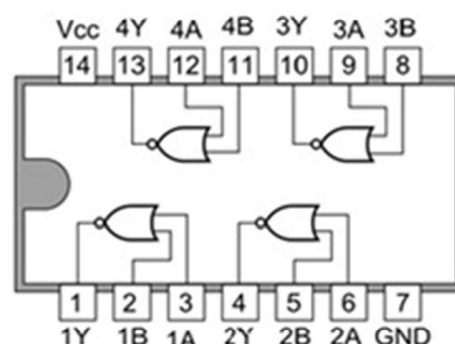
7404 Hex Inverters



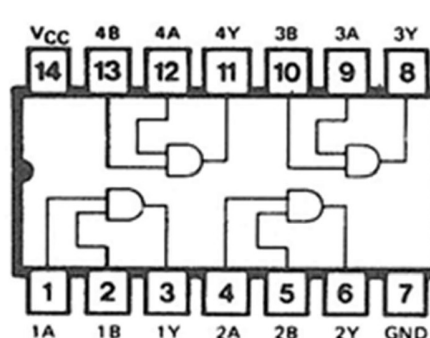
7432 OR Gates



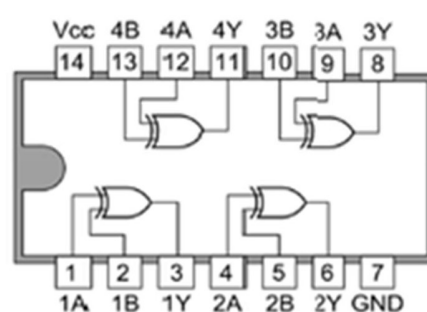
7402 Quad 2-input NOR Gates



7408 AND Gates



7486 Quad 2-input ExOR Gates



PROCEDURE:

- Do the connection as per IC Pin diagram. Connect Vcc (Pin 14) and Ground (Pin 7) with Power supply properly.
- Apply Logical inputs as per truth table with considering Positive Logic (0V for 0 input and 5V for 1 input).
- Observe and record the output voltage using DMM or test whether LED is on or off using LED tester in observation table.
- Verify the working of gates by comparing the truth table and observation table.
- Repeat all the steps for each gate and complete the observation table.

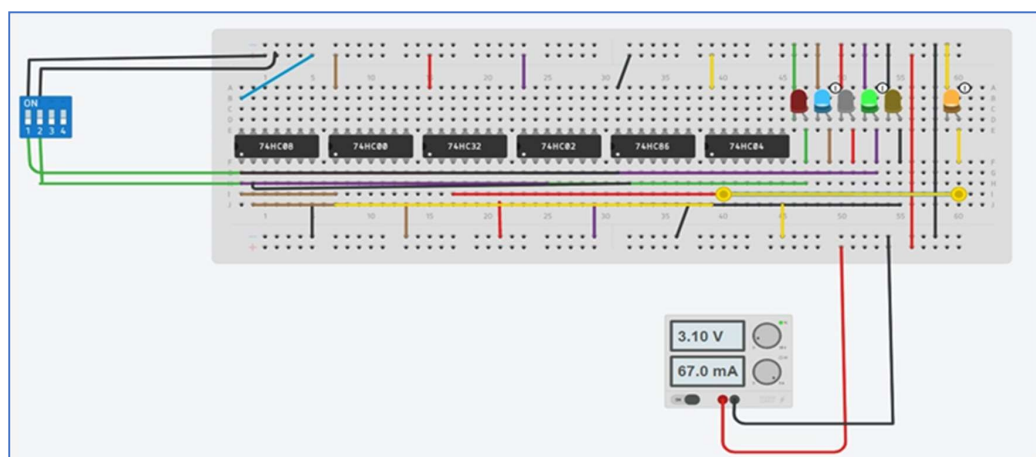
OBSERVATION TABLE:

Logic gates using IC:

Input A	Input B	Output of Gates				
		AND	OR	NAND	NOR	X-OR
0(0v)	0(0v)	0	0	1	1	0
0(0v)	1(5v)	0	1	1	0	1
1(5v)	0(0v)	0	1	1	0	1
1(5v)	1(5v)	1	1	0	0	0

For NOT Gate:

Input A	Output
0(0v)	1
1(5v)	0

OBSERVATION:**CONCLUSION:**

By performing this practical we can learn about various kind of gates and logical circuits. We also learn to simulate circuits in Simulation Software or website.

Obtained Marks:

Faculty Sign:

Date:

ASSIGNMENT:

1. Draw and write logic gate's symbols, functions, truth tables and IC's Pin diagrams.
2. List out various vendors or company names who are manufacturing various ICs.
3. What are different logic families using which logic gates ICs are manufactured?
4. Draw circuit diagrams of NAND and NOR gates using TTL and CMOS logic families and compare performance of both.

ANS - 2

Different company names who manufacture various ICs

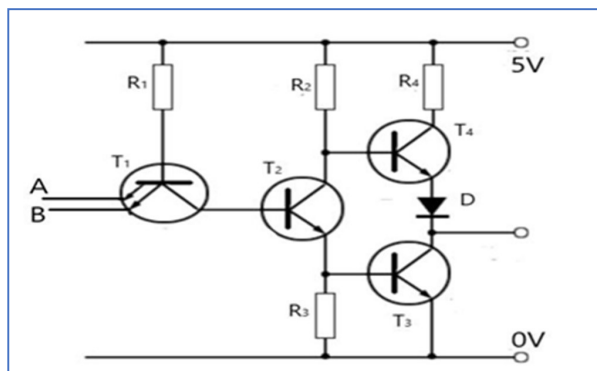
- TEXAS INSTRUMENTS DIP CD4026BE, For CMOS seven-segment counter IC. ...
- Isd1820py Dip-14 Chip 8 To 20 Second. ...
- Avago SMD Electronic Ic Chip, For Electronics, HCPL-3150. ...
- 74244 OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS IC. ...
- Non BGA ICs. ...
- Sm4005a Ic For Panel Tcon Chips Sm4005 Sm4005a Qfn-48.

ANS - 3

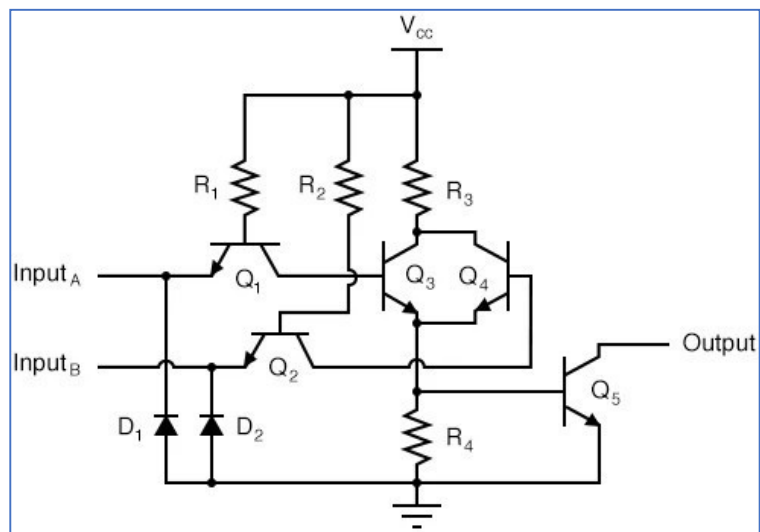
TTL - Transistor-Transistor Logic: Standard logic family; used for the longest time. ECL - Emitter Coupled Logic: Suitable for systems requiring high-speed operations. MOS - Metal Oxide Semiconductor Logic: Suitable for systems with high component density.

ANS - 4

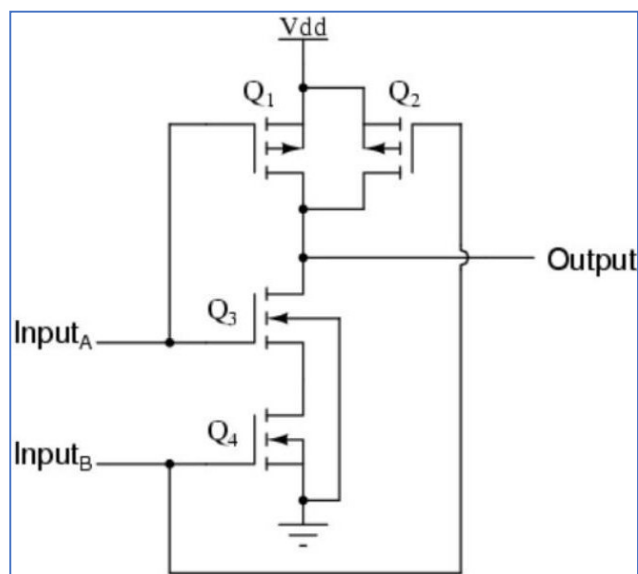
- TTL NAND :



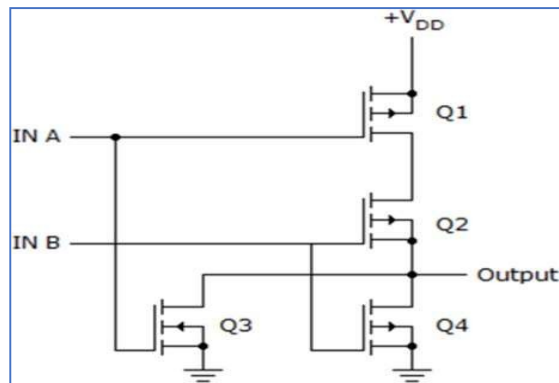
- TTL NOR :



- CMOS NAND :



- CMOS NOR:



The **advantage of the CMOS over the TTL chips** is that the CMOS has a higher **density of logic gates** within the same material. TTL chips **consume more power** as compared to the power consumed by the CMOS chips even at rest. The power consumption of the CMOS depends on various factors and is variable. The **clock rate** is one of the major factors for power consumption. Higher clock values will result in higher power consumption. When making the comparisons, a single gate in CMOS chip would consume the 10nW of power whereas an equivalent gate on the TTL chip will consume approximately 10mW power. The difference is substantially high and this is why the **CMOS chips are always preferred over the TTL chips**