# UNIT 5 COMPUTER ARITHMETIC

#### Unsigned & Signed (Magnitude, 1's & 2's Complement) Numbers

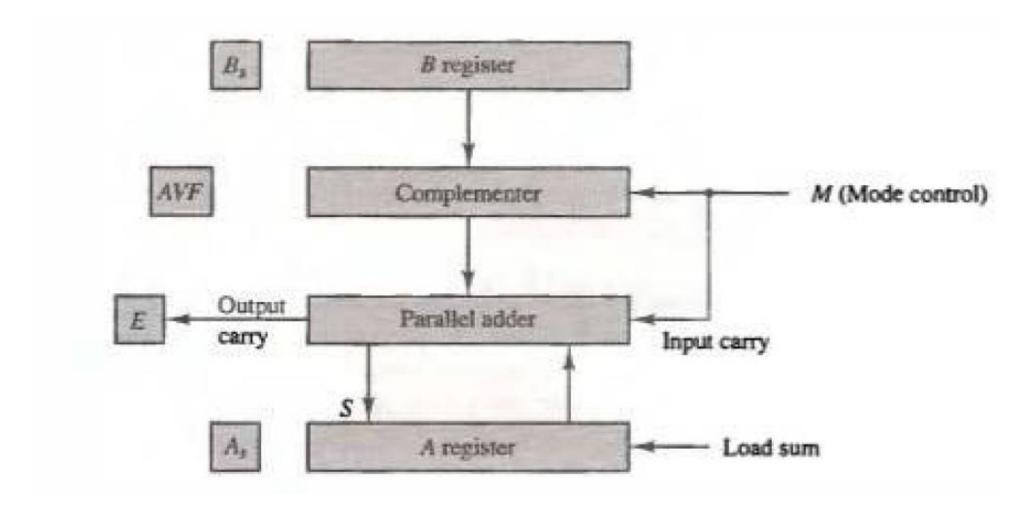
Desimal	Unsigned	Signed			
Decimal		Signed Magnitude	Signed 1's Complemet	Signed 2's Complemet	
40	101000	0101000	0101000	0101000	
-40	-	1101000	1010111	1011000	
8	1000	01000	01000	01000	
-8	-	11000	10111	11000	
14	1110	01110	01110	01110	
-14	-	11110	10001	10010	
13	1101	01101	01101	01101	
-13	-	11101	10010	10011	
Diname	Unsigned	Signed			
Binary		Signed Magnitude	Signed 1's Complemet	Signed 2's Complemet	
10110	22	-6	-9	-10	
10010	18	-2	-13	-14	
10001	17	-1	-14	-15	
10011	19	-3	-12	-13	
1011000	88	-24	-39	-40	
1010111	87	-23	-40	-41	

#### Addition & Subtraction of Signed-Magnitude Numbers

TABLE 10-1 Addition and Subtraction of Signed-Magnitude Numbers

	A 4 4	Subtract Magnitudes		
Operation	Add Magnitudes	When $A > B$	When $A < B$	When $A = B$
(+A) + (+B)	+(A + B)			
(+A) + (-B)	,	+(A-B)	-(B-A)	+(A-B)
(-A)+(+B)		-(A-B)	+(B-A)	+(A-B)
(-A)+(-B)	-(A + B)			
(+A)-(+B)		+(A-B)	-(B-A)	+(A-B)
(+A)-(-B)	+(A + B)			
(-A)-(+B)	-(A + B)			
(-A)-(-B)		-(A - B)	+(B-A)	+(A-B)

## Hardware Implementation



#### Flowchart for Add & Subtract Operation

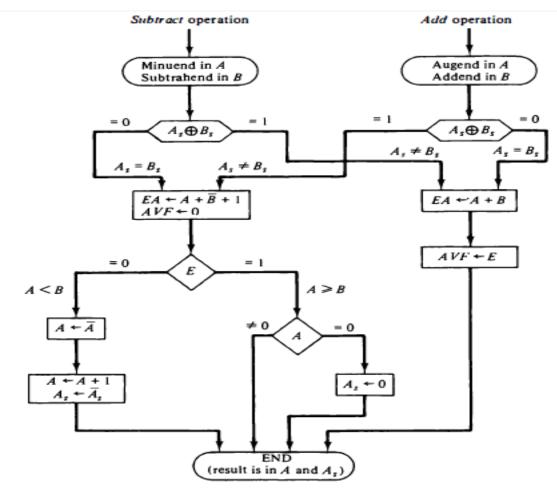
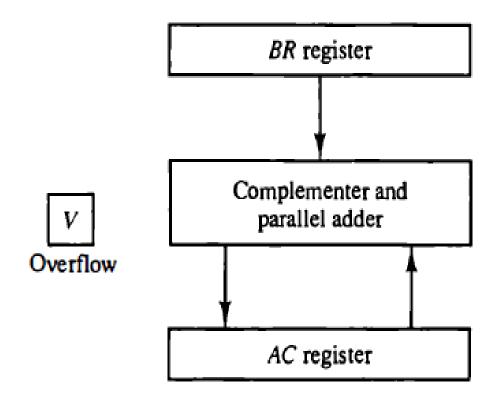


Figure 10-2 Flowchart for add and subtract operations.

#### Addition & Subtraction of Signed-2'S Complement Numbers

Figure 10-3 Hardware for signed-2's complement addition and subtraction.



#### Addition & Subtraction of Signed-2'S Complement Numbers

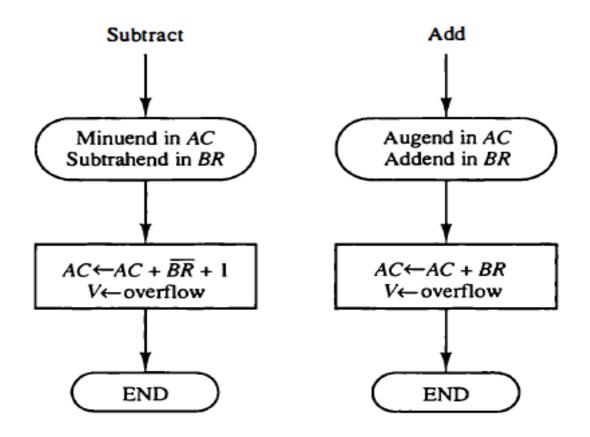
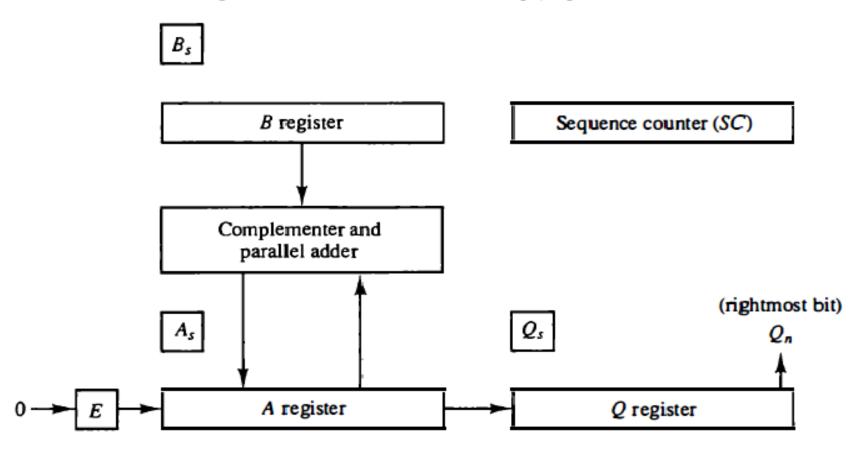


Figure 10-4 Algorithm for adding and subtracting numbers in signed-2's complement representation.

#### Multiplication Algorithms

Figure 10-5 Hardware for multiply operation.



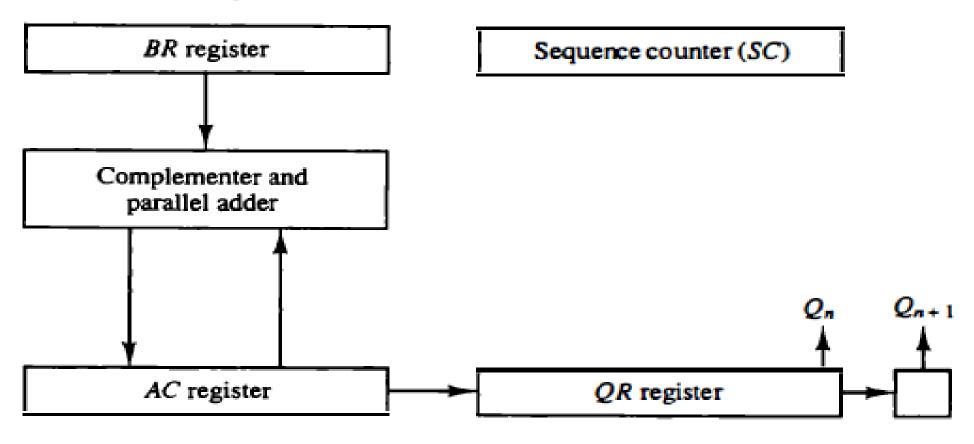
## Multiplication Algorithms

Multiply operation Multiplicand in BMultiplier in Q  $A_s \leftarrow Q_s \oplus B_s$  $Q_s \leftarrow Q_s \oplus B_s$  $A \leftarrow 0, E \leftarrow 0$   $SC \leftarrow n - 1$  $Q_{n}$  $EA \leftarrow A + B$  $SC \leftarrow SC - 1$ **≠** 0 = 0END (product is in AQ)

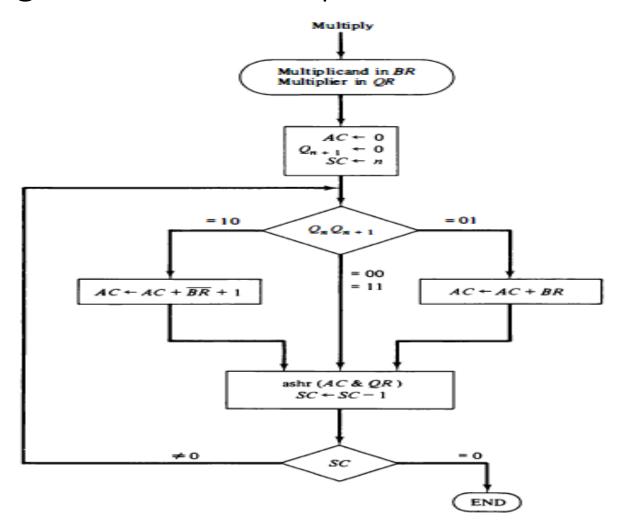
Figure 10-6 Flowchart for multiply operation.

#### Hardware for Booth Algorithm

Figure 10-7 Hardware for Booth algorithm.

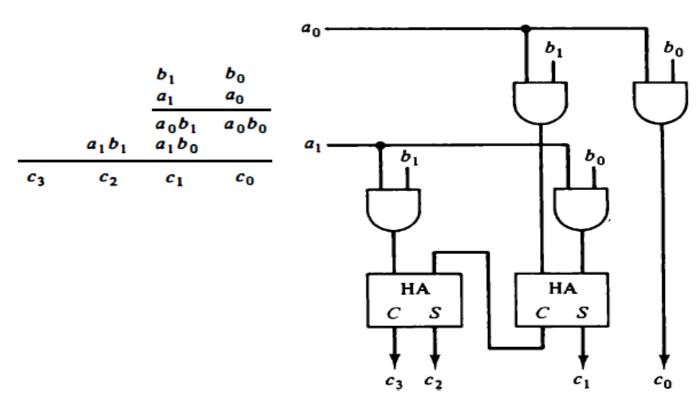


## Booth Algorithm for Multiplication

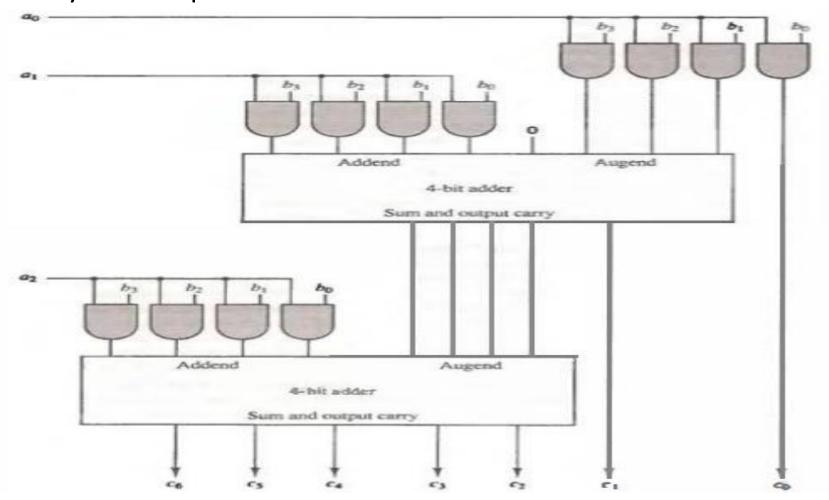


## Array Multiplier

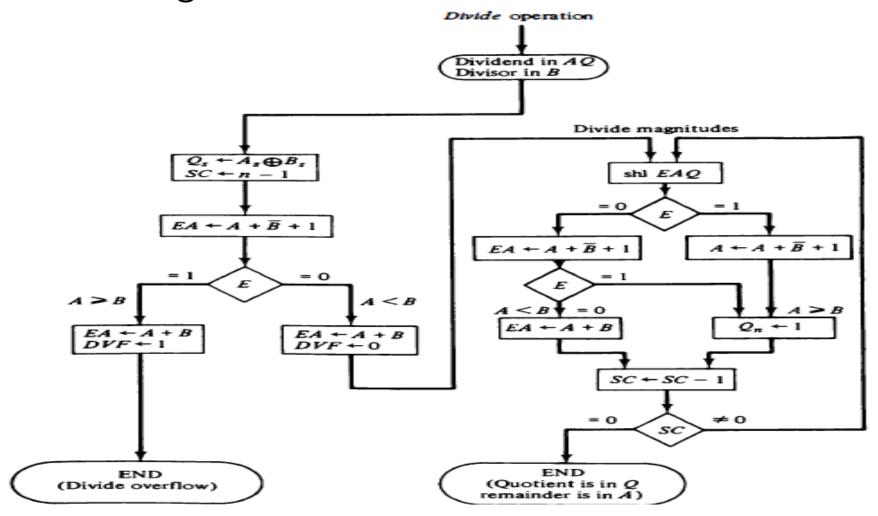
Figure 10-9 2-bit by 2-bit array multiplier.



# Array Multiplier



## Division Algorithm



#### Floating Point Arithmetic

#### **Addition & Subtraction**

- Check for zeros
- Align the mantissas
- Add or Subtract the mantissas
- Normalize the result

#### Floating Point Arithmetic

#### Multiplication

- Check for zeros
- Add the exponents
- Multiply the mantissas
- Normalize the result

#### Floating Point Arithmetic

#### **Division**

- Check for zeros
- Initialize the registers and evaluate the sign
- Align the dividend
- Subtract the exponents
- Divide the mantissas