**Date:**

# EXPERIMENT NO. 5

***AIM: Design, Implement and verify operation of 2-bit magnitude comparator circuit.***

**APPARATUS:** connection wires, power supply, power project board, resistors, LED, ICs

| Sr.No. | Component | Specification | Quantity |
|---|---|---|---|
| 1 | AND Gate | IC 7408 | 1 |
| 2 | OR Gate | IC 7432 | 1 |
| 3 | NOT Gate | IC 7404 | 1 |
| 4 | XOR Gate | IC7486 | 1 |
| 5 | Three input AND Gate | IC7411 | 1 |

*SIMULATION WEBSITE:* ***https://www.tinkercad.com/***

**THEORY:**

Definition

A magnitude comparator is a combinational circuit that compares two numbers A & B to determine whether:

- A > B, or
- A = B, or
- A < B

Inputs

First *n*-bit number A

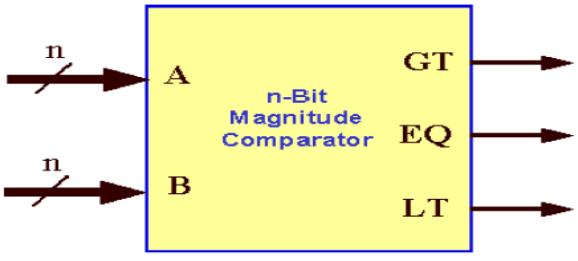
Second *n*-bit number B

Outputs

3 output signals (GT, EQ, LT), where:

1. GT = 1 IFF A > B
2. EQ = 1 IFF A = B
3. LT = 1 IFF A < B

Note: *Exactly One* of these 3 outputs equals 1, while the other 2 outputs are 0`s




4-bit magnitude comparator

Inputs: 8-bits (A ⇒ 4-bits , B ⇒ 4-bits)

A and B are two 4-bit numbers

- Let A = $A_3A_2A_1A_0$ , and
- Let B = $B_3B_2B_1B_0$
- Inputs have $2^8$ (*256*) possible combinations
- Not easy to design using conventional techniques

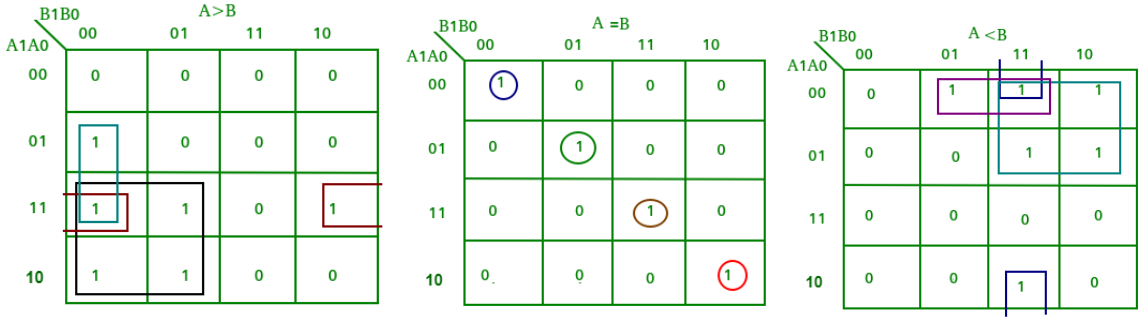
2-Bit Magnitude Comparator:

A comparator used to compare two binary numbers each of two bits is called a 2-bit Magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to, and greater than between two binary numbers.

The truth table for a 2-bit comparator is given below:

| INPUT | | | | OUTPUT | | |
|---|---|---|---|---|---|---|
| A1 | A0 | B1 | B0 | A<B | A=B | A>B |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |

From the above truth table K-map for each output can be drawn as follows:




A>B:A1B1’ + A0B1’B0’ + A1A0B0’

A=B: A1’A0’B1’B0’ + A1’A0B1’B0 + A1A0B1B0 + A1A0’B1B0’

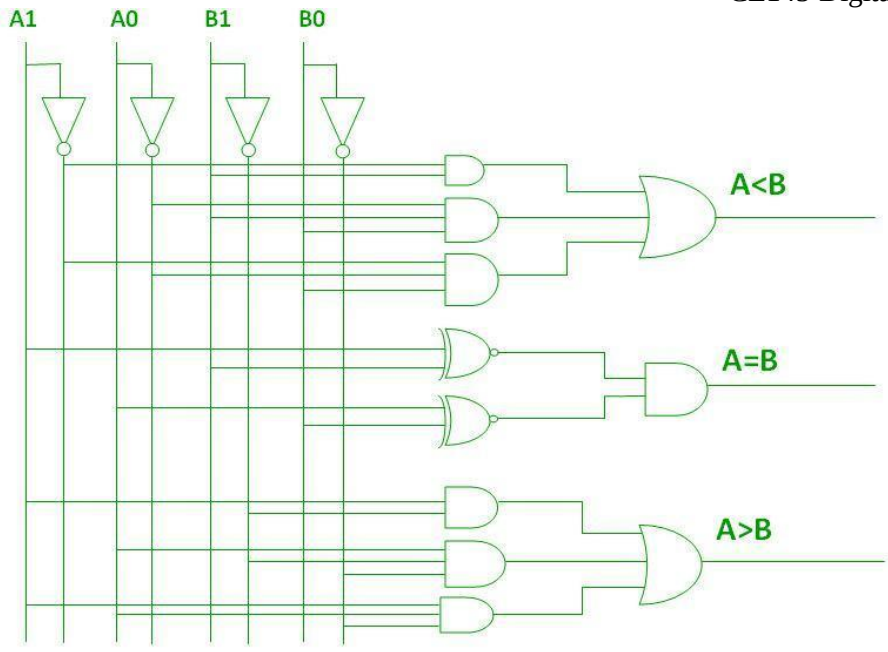
: A1’B1’ (A0’B0’ + A0B0) + A1B1 (A0B0 + A0’B0’)

: (A0B0 + A0’B0’) (A1B1 + A1’B1’)

: (A0 Ex-Nor B0) (A1 Ex-Nor B1)

A<B:A1’B1 + A0’B1B0 + A1’A0’B0

By using these Boolean expressions, we can implement a logic circuit for this comparator as given below:



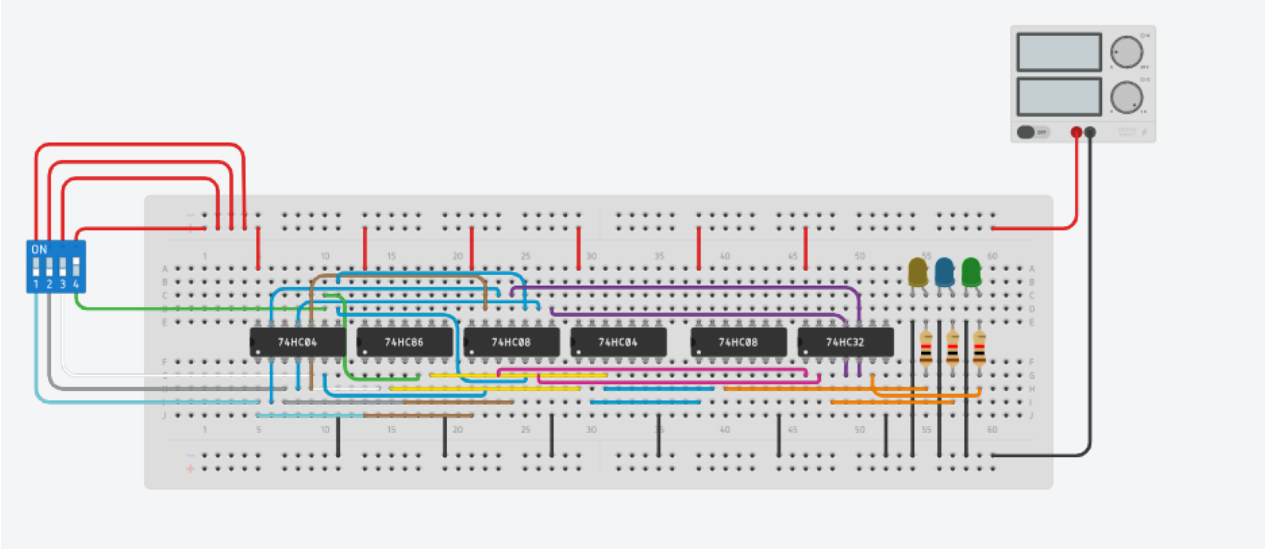

**PROCEDURE:**

i. Make connections as per logic circuit diagram.
ii. Apply proper input condition and observe the output information of led on/off.
iii. Apply all possible combinations of input and verify correctness of circuit output as per truth tables.

**OBSERVATION TABLE***:*

| Serial No. | $A_1$ | $A_0$ | $B_1$ | $B_0$ | A>B | A=B | A<B |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 3 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 4 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 5 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 6 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 7 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 8 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

**OBSERVATION:**



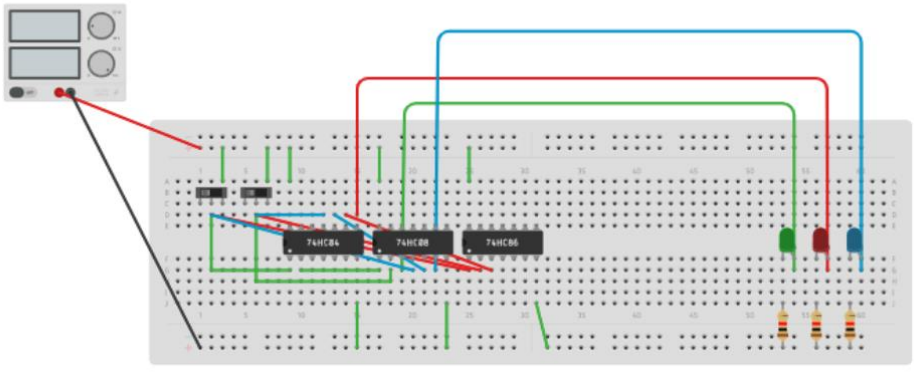

**Obtained Marks:**
**Faculty Sign:**
**Date:**

**ASSIGNMENT:**

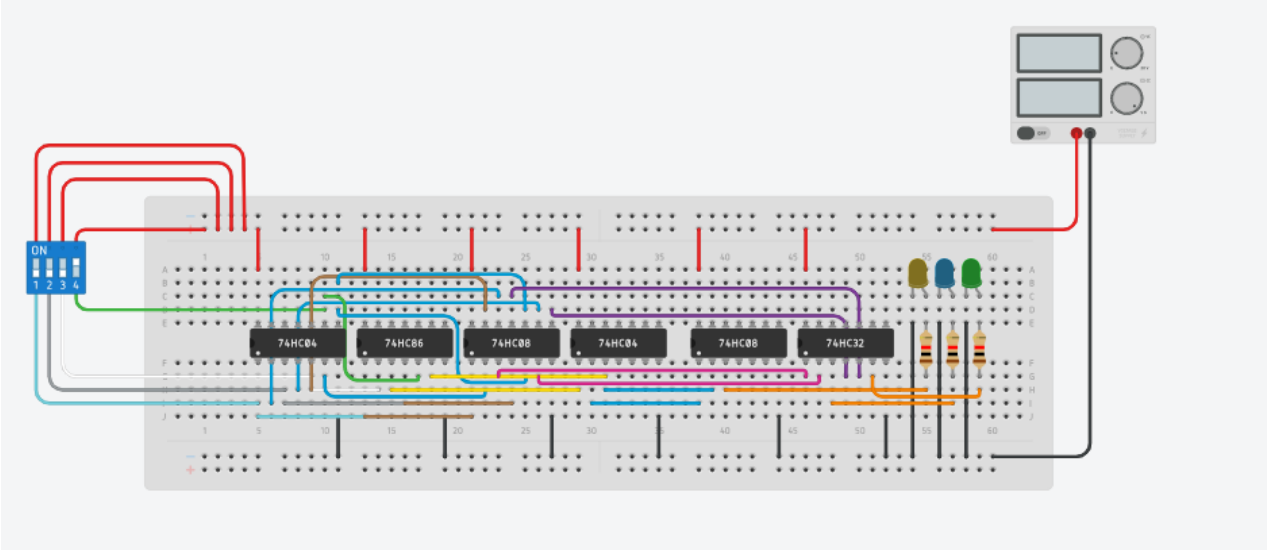
1. Simulate 1 bit and 2-bit magnitude comparator experiment on http://vlabs.iitb.ac.in/vlabs-dev/labs/digital-electronics/experiments/verify-truth-table-of-one-bit-and-two-bit-comparator-iitr/simulation.html and show results.

Ans.

1-bit magnitude comparator:



2-bit magnitude comparator:




2. Draw pin diagram of IC 7485 and explain how it can be used for 4 bit magnitude comparison.
Ans.