Digital Electronics

Chapter 3(part - 1)
Combinational Logic

Outline of Chapter 3(part - 1)

- 4.1 Introduction
- 4.2 Design Procedure
- 4.3 Adders
- 4.4 Subtractors
- 4.5 Analysis Procedure

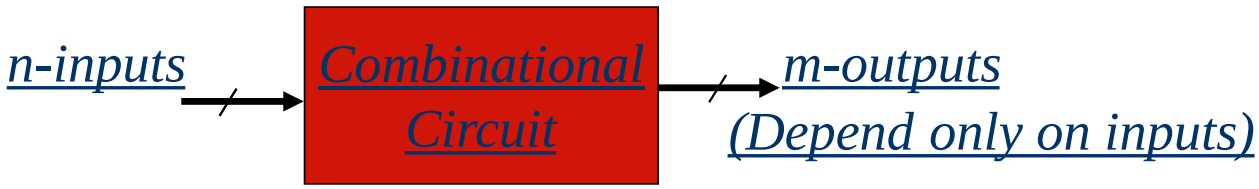
INTRODUCTION

- A combinational circuit consists of logic gates whose outputs, at any time, are determined by combining the values of the inputs.
- For n input variables, there are 2^n possible binary input combinations.
- For each binary combination of the input variables, there is one possible output.

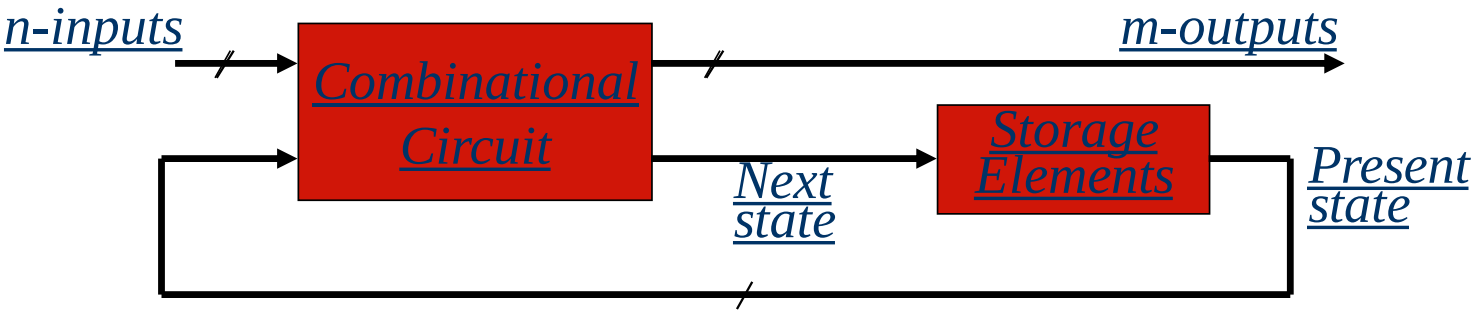
INTRODUCTION

- Hence, a combinational circuit can be described by:
  1. A truth table that lists the output values for each combination of the input variables, or
  2. *m* Boolean functions, one for each output variable.

INTRODUCTION



Combinational Circuit



Sequential Circuit

DESIGN PROCEDURE

- The procedure involves the following steps:

1. State the problem.
2. Determine no. of available input variables and required output variables.
3. Assign letter symbols to the input and output variables.
4. Derive the truth table that defines the required relationship between inputs and outputs.
5. Obtain simplified Boolean function for each output.
6. Draw the logic diagram.

ADDERS(HALF ADDER)

- A combinational circuit that performs the addition of two bits is called a half adder.
- The truth table for the half adder is listed below:

Table 4-3
Half Adder

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

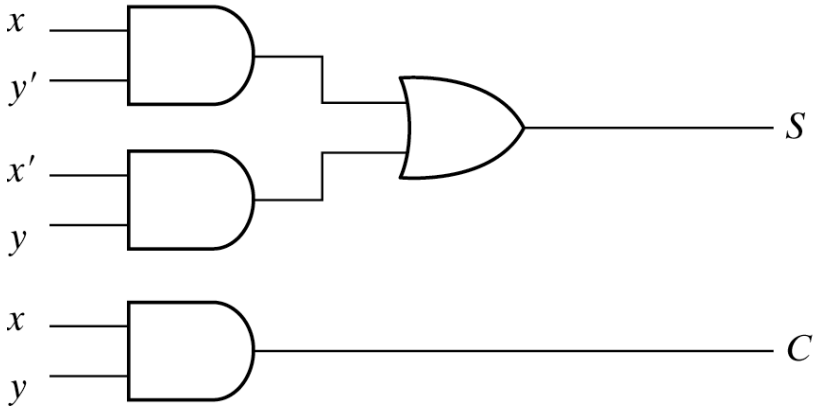
S: Sum
C: Carry

$S = x'y + xy'$

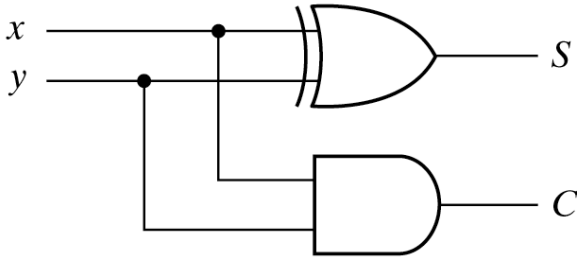
$C = xy$

ADDERS(HALF ADDER)

Implementation of HALF ADDER



(a) $S = xy' + x'y$
$C = xy$



(b) $S = x \oplus y$
$C = xy$

Fig. 4-5 Implementation of Half-Adder

ADDERS (FULL ADDER)

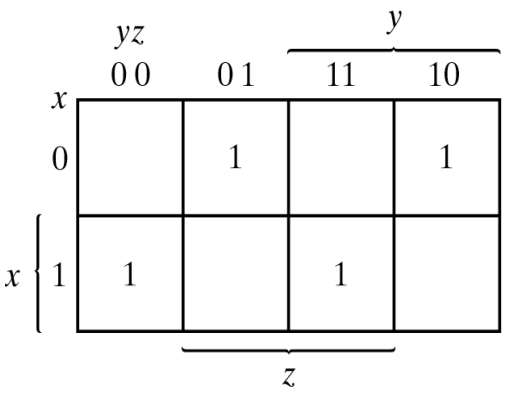
- One that performs the addition of three bits(two significant bits and a previous carry) is a full adder.

Table 4-4
Full Adder

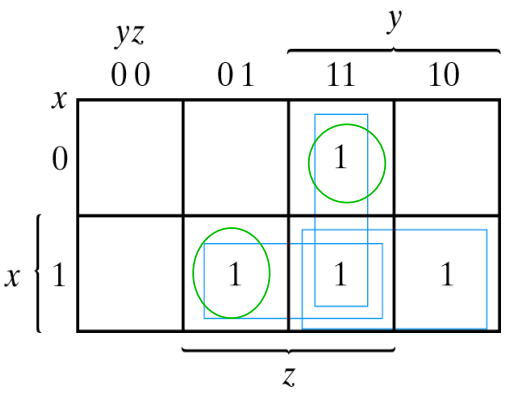
x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

ADDERS (FULL ADDER)

Simplified Expression



$S = x'y'z + x'yz' + xy'z' + xyz$



$C = xy + xz + yz$
$= xy + xy'z + x'yz$

Fig. 4-6 Maps for Full Adder

$$S = x'y'z + x'yz' + xy'z' + xyz$$

$$C = xy + xz + yz$$

ADDERS (FULL ADDER)

Full Adder Implementation in SOP

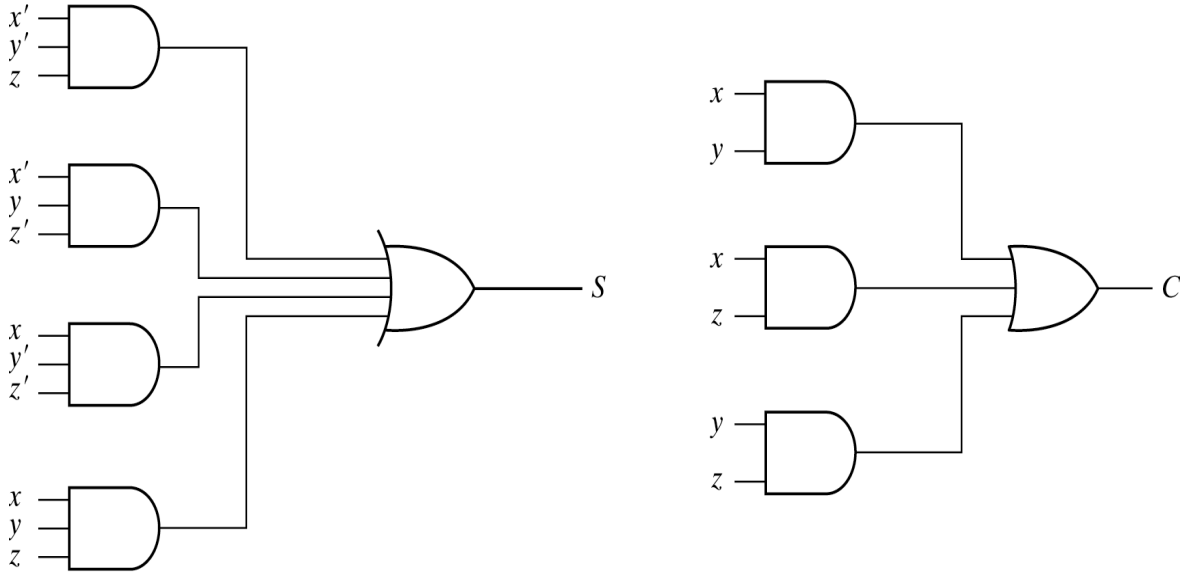


Fig. 4-7 Implementation of Full Adder in Sum of Products

ADDERS (FULL ADDER)

- Full-adder can also implemented with two half adders and one OR gate (Carry Look-Ahead adder).

$S = z \oplus (x \oplus y)$

$= z'(xy' + x'y) + z(xy' + x'y)'$

$= xy'z' + x'yz' + xyz + x'y'z$

$C = z(xy' + x'y) + xy = xy'z + x'yz + xy$

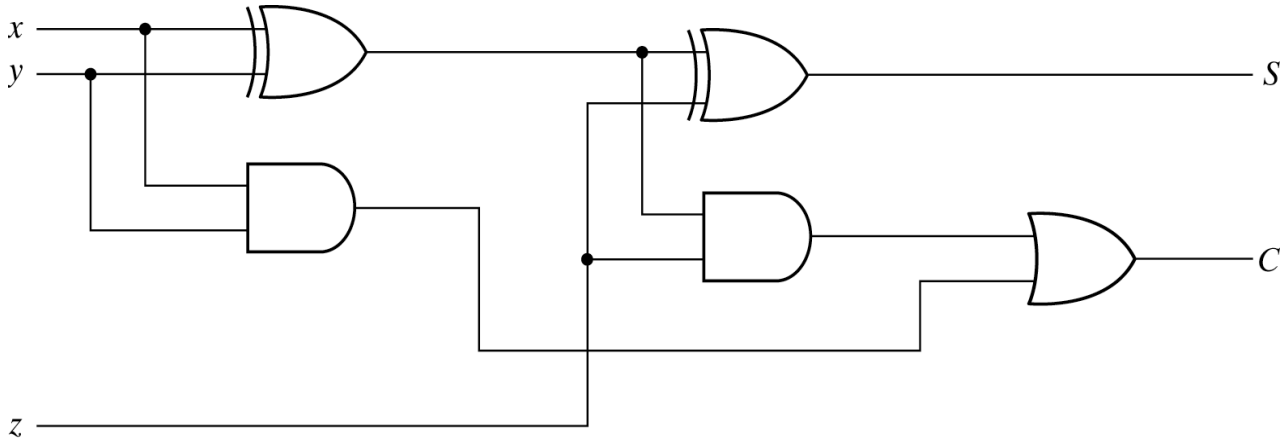


Fig. 4-8 Implementation of Full Adder with Two Half Adders and an OR Gate

SUBTRACTORS(HALF SUBTRACTOR)

- A combinational circuit that performs the subtraction of two bits is called a half subtractor.
- The truth table for the half subtractor is listed below:

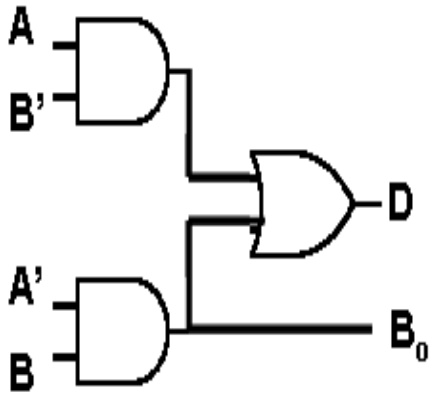
Input		Output	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Difference = A'B+AB'

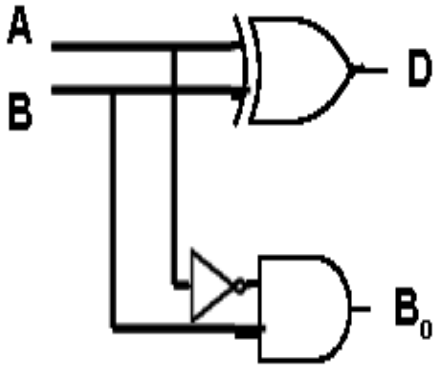
Borrow = A'B

SUBTRACTORS(HALF SUBTRACTOR)

Implementation of HALF SUBTRACTOR



(a)



(b)

D = A'B+AB'
B = A'B

D = A'B+AB'
B = A'B

SUBTRACTORS(FULL SUBTRACTOR)

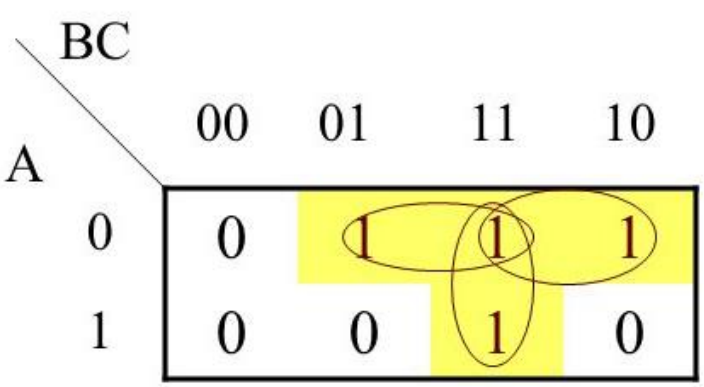
- One that performs the subtraction of three bits is a full subtractor.

Input			Output	
A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

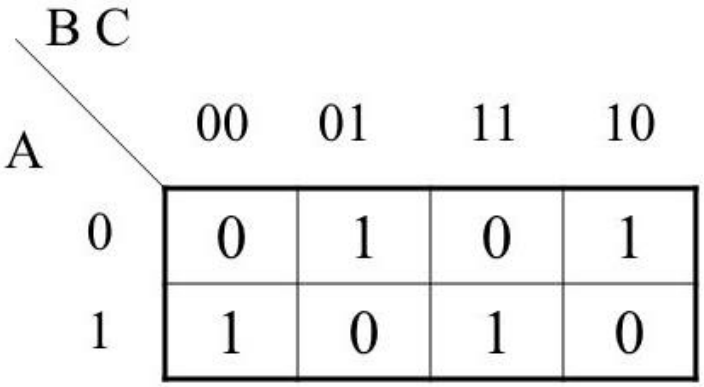
Truth table of full subtractor

SUBTRACTORS(FULL SUBTRACTOR)

Simplified Expression



For Borrow



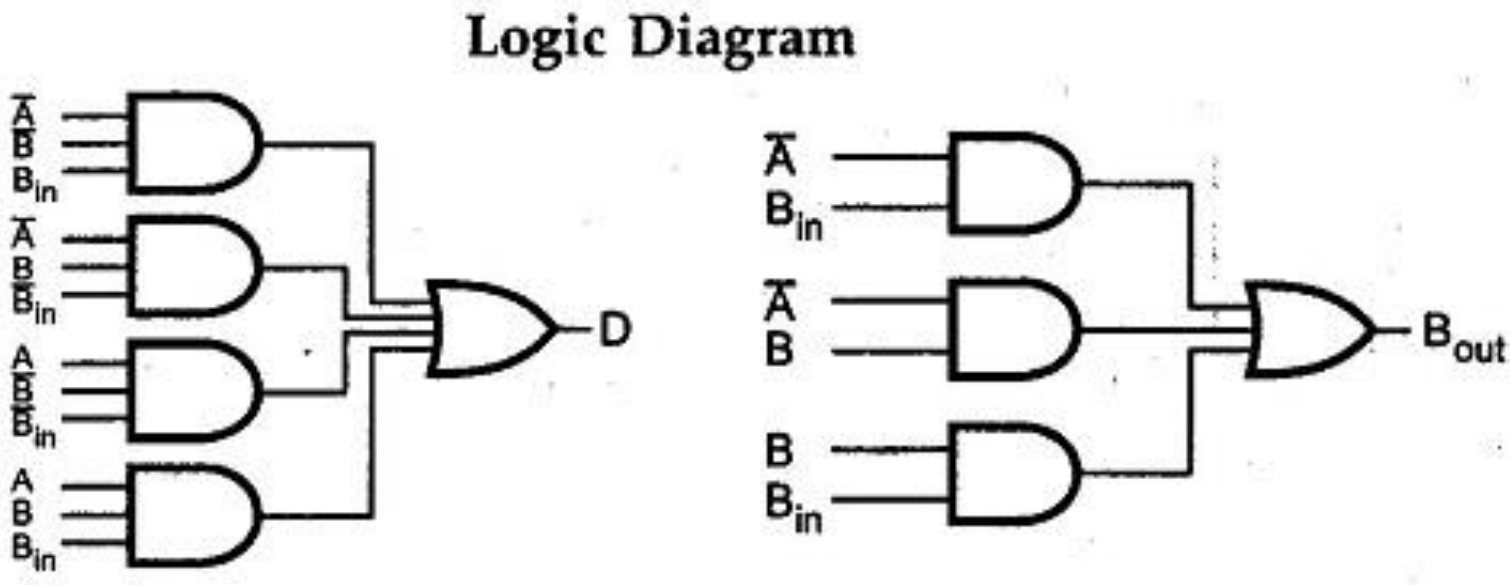
For Difference

D = A’B’C+A’BC’+AB’C’+ABC

C = A’C+A’B+BC

SUBTRACTORS(FULL SUBTRACTOR)

Full Subtractor Implementation in SOP



SUBTRACTORS(FULL SUBTRACTOR)

- Logic diagram of Full Subtractor has been shown in the figure below: