Chapter 4(part – 2)
Registers, Counters & the Memory Units

Registers

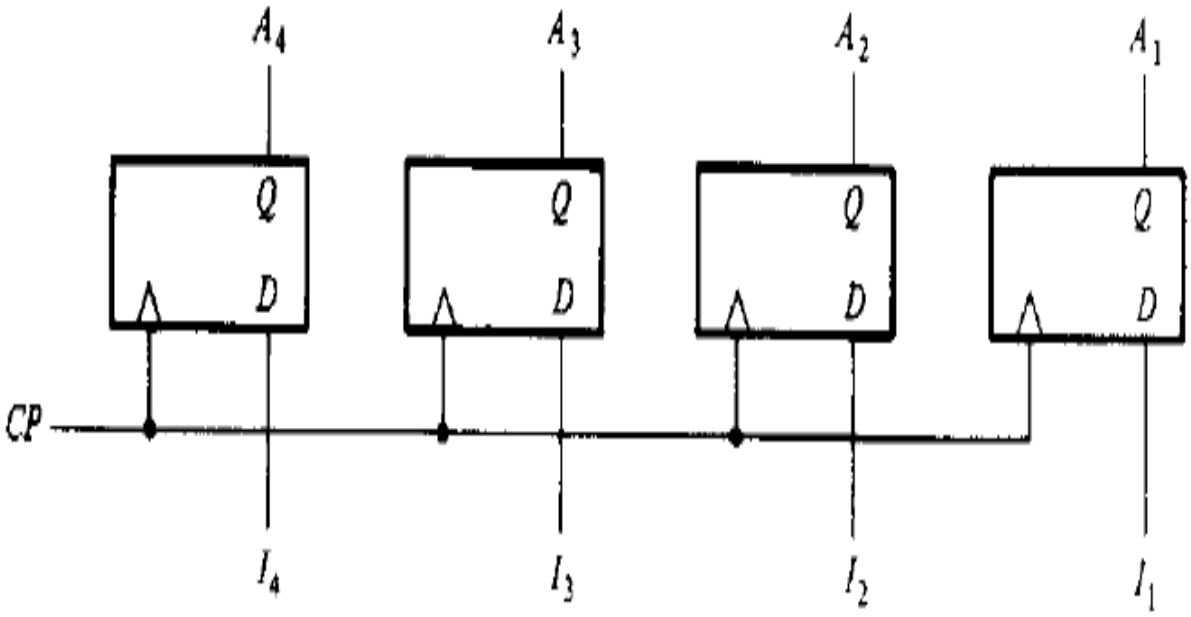


FIGURE 7-1

4-bit register

Register with Parallel Load

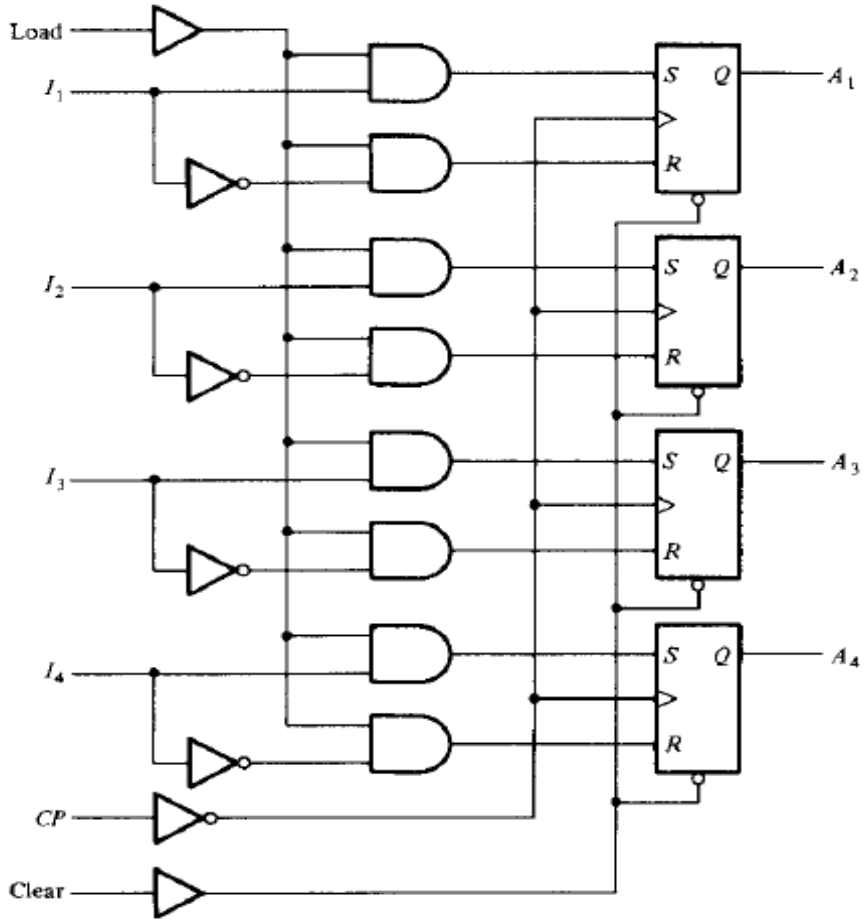


FIGURE 7-2
4-bit register with parallel load

Register with Parallel Load

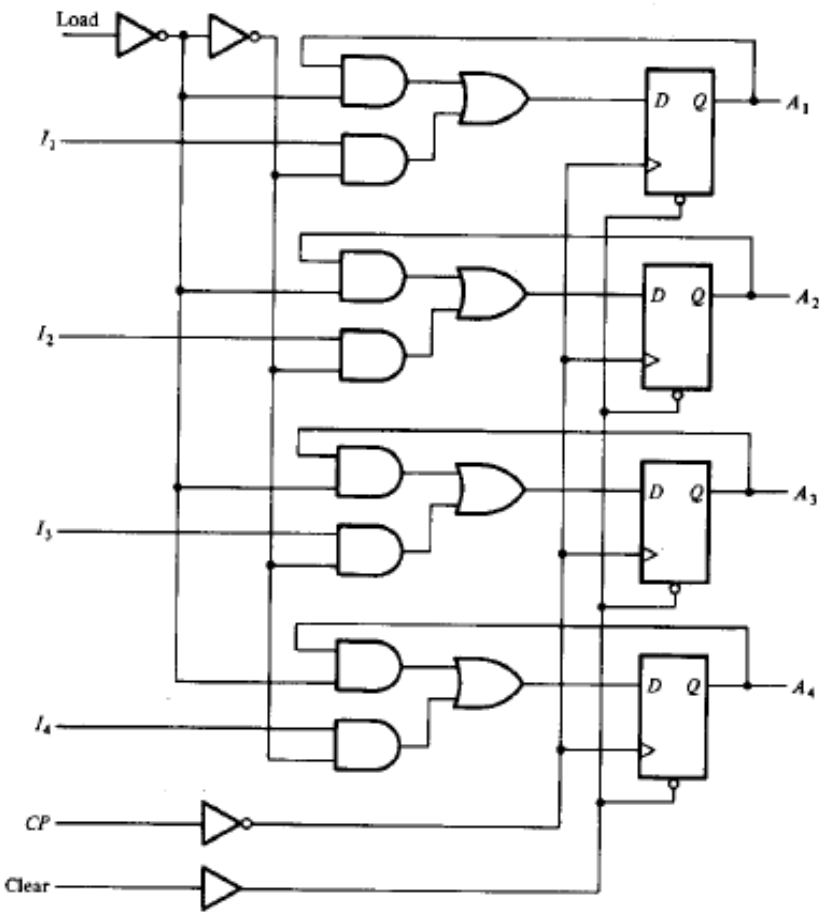


FIGURE 7-3
Register with parallel load using *D* flip-flops

Shift Register

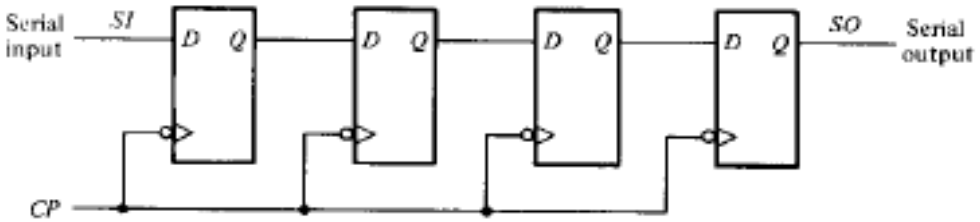
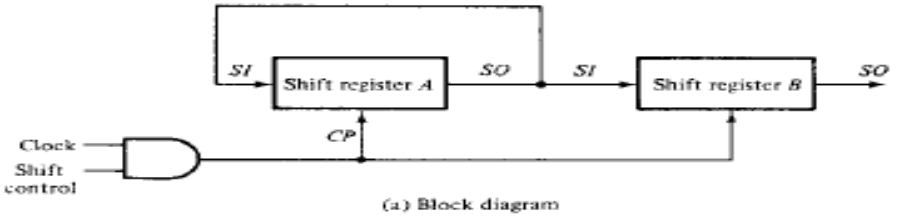


FIGURE 7-7
Shift register

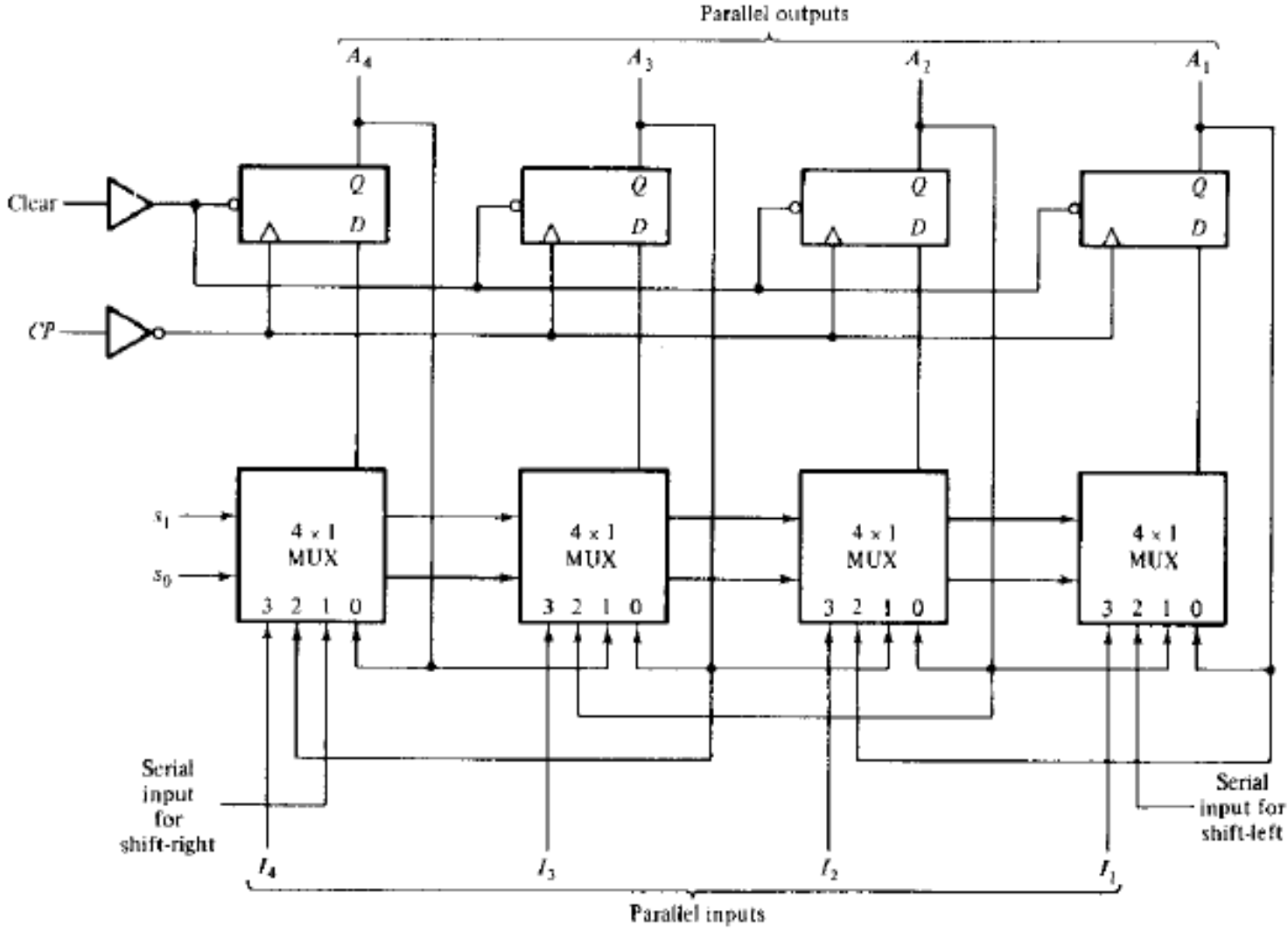


(a) Block diagram

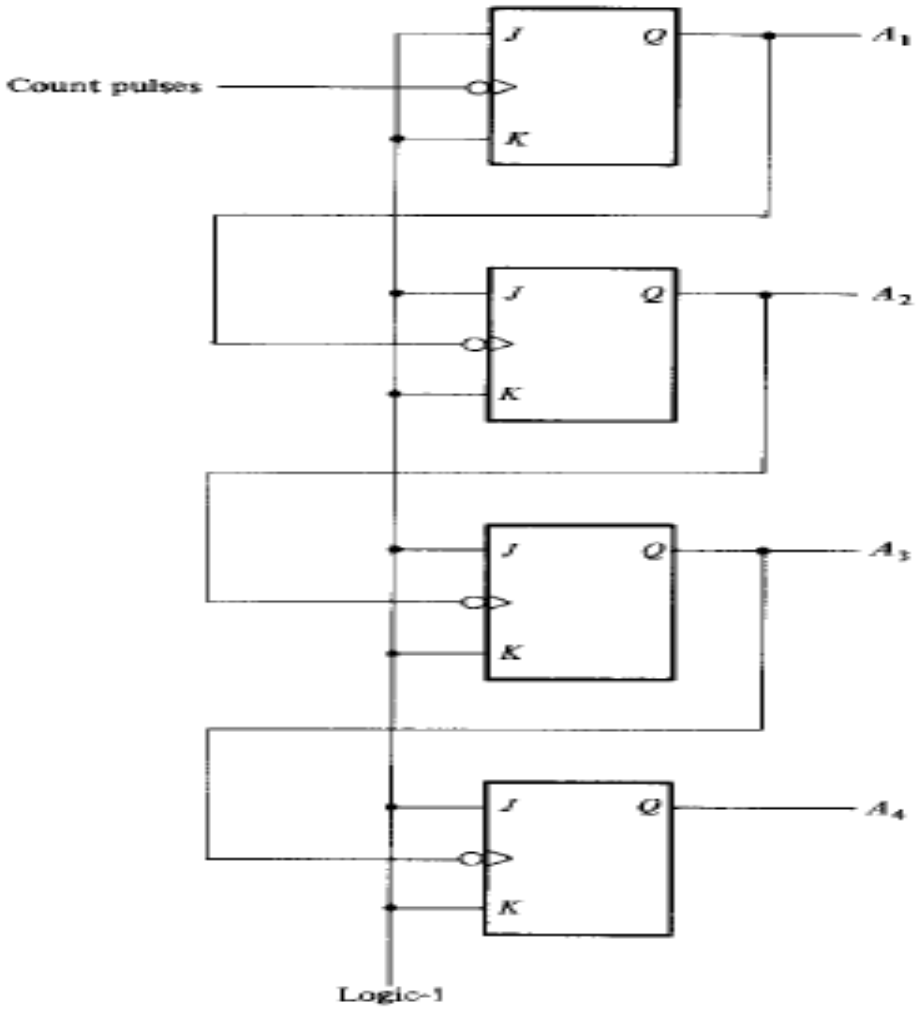
TABLE 7-1
Serial-Transfer Example

Timing Pulse	Shift Register *A*				Shift Register *B*				Serial Output of *B*
Initial value	1	0	1	1	0	0	1	0	0
After T_1	1	1	0	1	1	0	0	1	1
After T_2	1	1	1	0	1	1	0	0	0
After T_3	0	1	1	1	0	1	1	0	0
After T_4	1	0	1	1	1	0	1	1	1

4-Bit Bidirectional Shift Register with Parallel Load



4-Bit Binary Ripple Counter



4-Bit Binary Ripple Counter

TABLE 7-4
Count Sequence for a Binary Ripple Counter

Count Sequence					
A_4	A_3	A_2	A_1	Conditions for Complementing Flip-Flops	
0	0	0	0	Complement A_1	
0	0	0	1	Complement A_1	A_1 will go from 1 to 0 and complement A_2
0	0	1	0	Complement A_1	
0	0	1	1	Complement A_1	A_1 will go from 1 to 0 and complement A_2;
					A_2 will go from 1 to 0 and complement A_3
0	1	0	0	Complement A_1	
0	1	0	1	Complement A_1	A_1 will go from 1 to 0 and complement A_2
0	1	1	0	Complement A_1	
0	1	1	1	Complement A_1	A_1 will go from 1 to 0 and complement A_2;
					A_2 will go from 1 to 0 and complement A_3;
					A_3 will go from 1 to 0 and complement A_4
1	0	0	0	and so on . . .	

BCD Ripple Counter

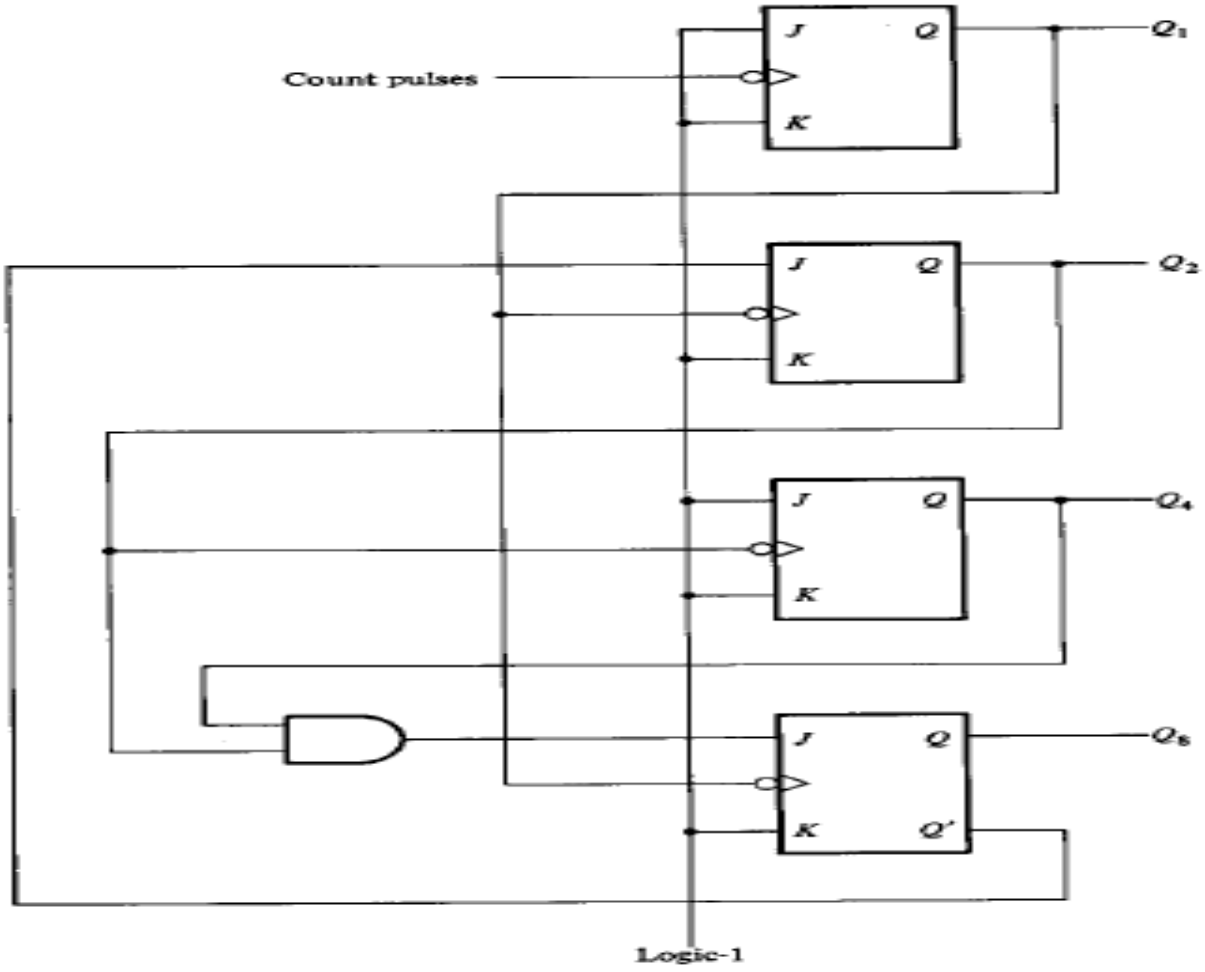
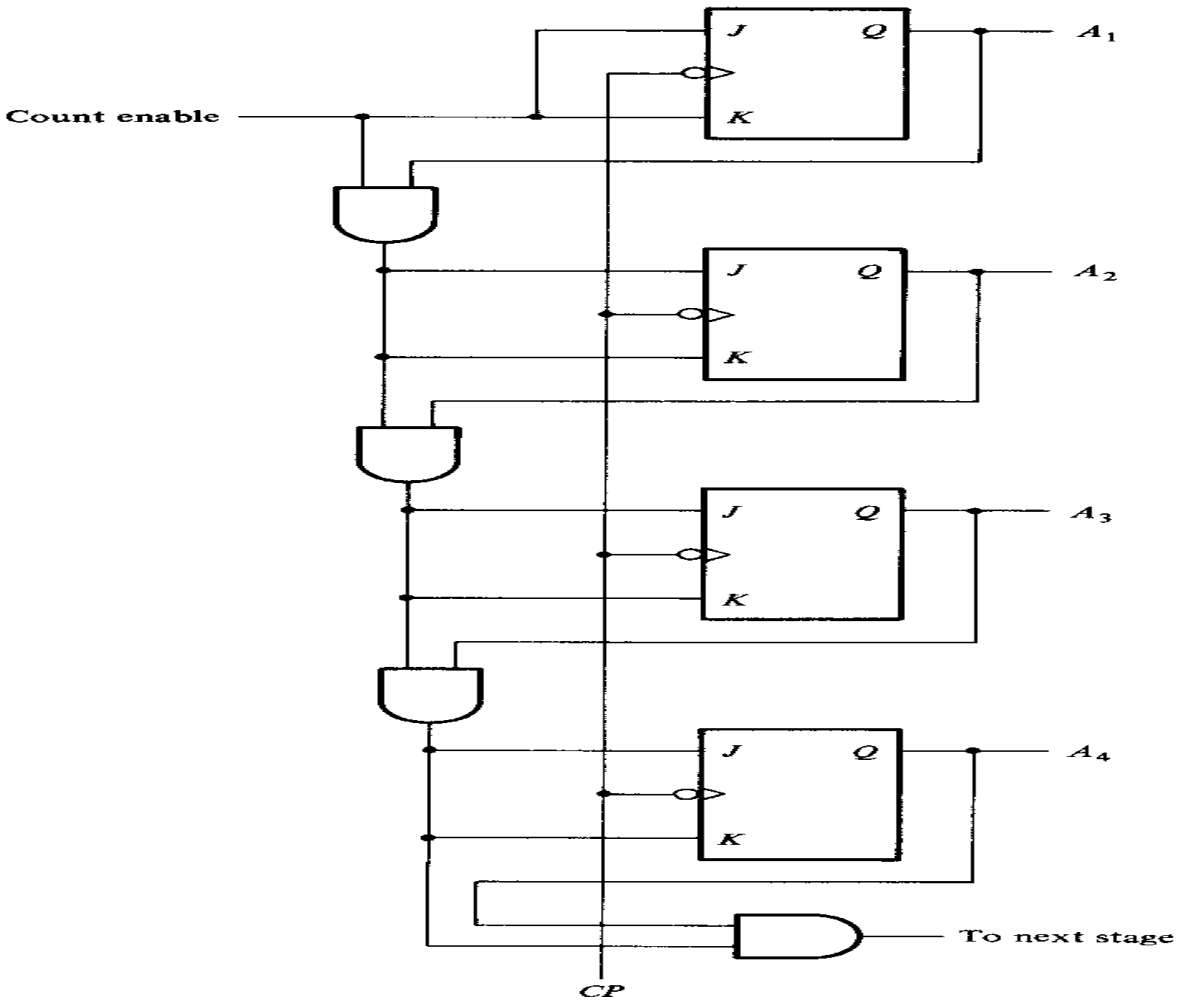
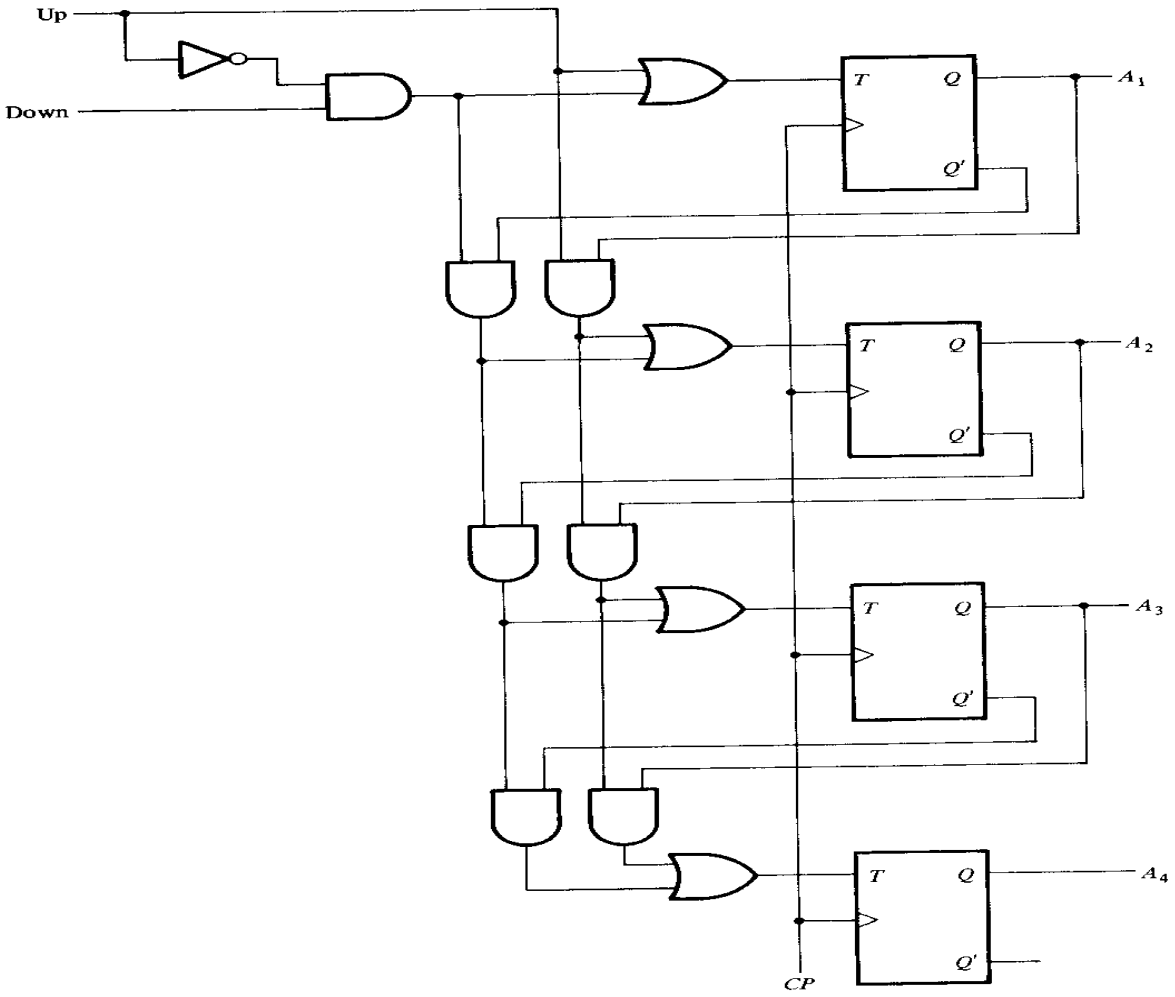


FIGURE 7-14
BCD ripple counter

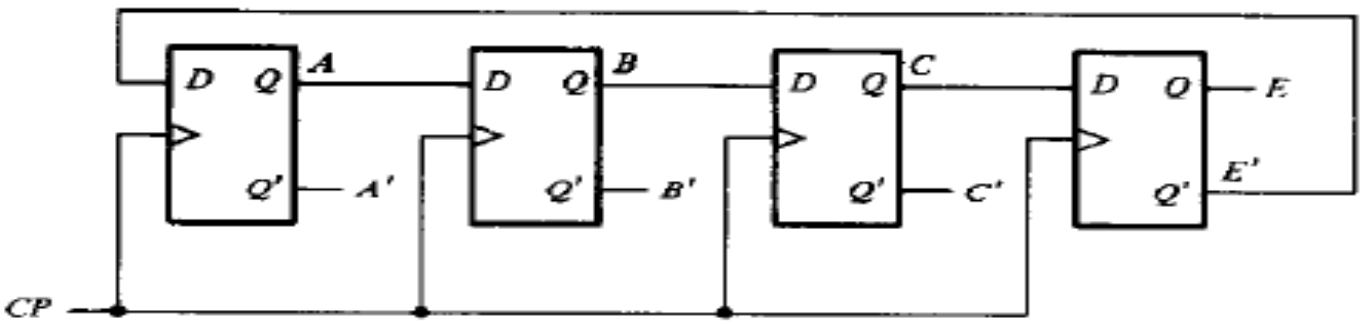
4 Bit Synchronous Binary Counter



4 Bit Binary Up Down Counter



Johnson Counter



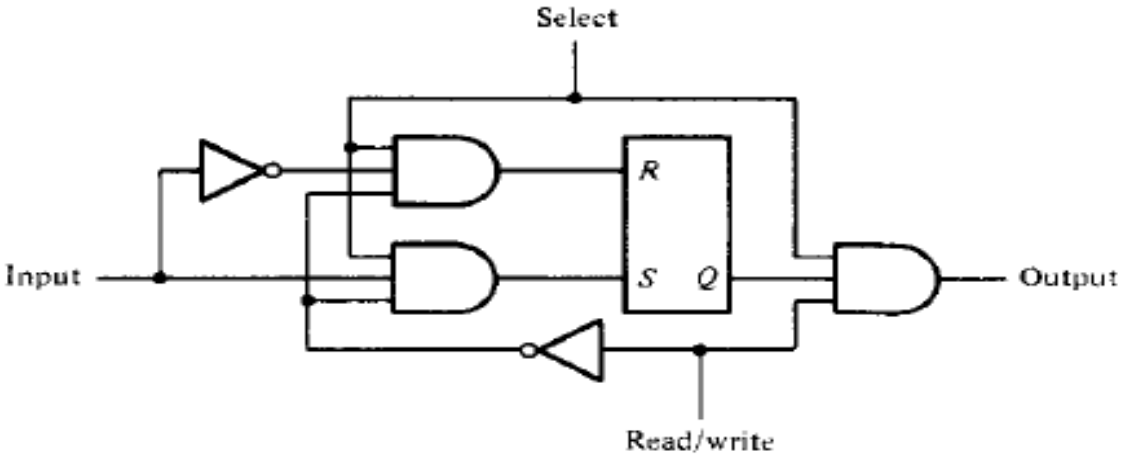
(a) Four-stage switch-tail ring counter

Sequence number	Flip-flop outputs A	B	C	E	AND gate required for output
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

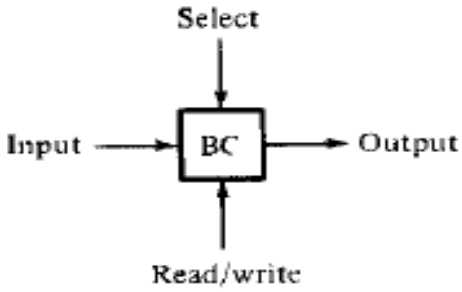
(b) Count sequence and required decoding.

FIGURE 7-23
Construction of a Johnson counter

Memory Cell (Binary Cell)



(a) Logic diagram



(b) Block diagram

FIGURE 7-26
Memory cell

Logical Construction of RAM (4 X 3)

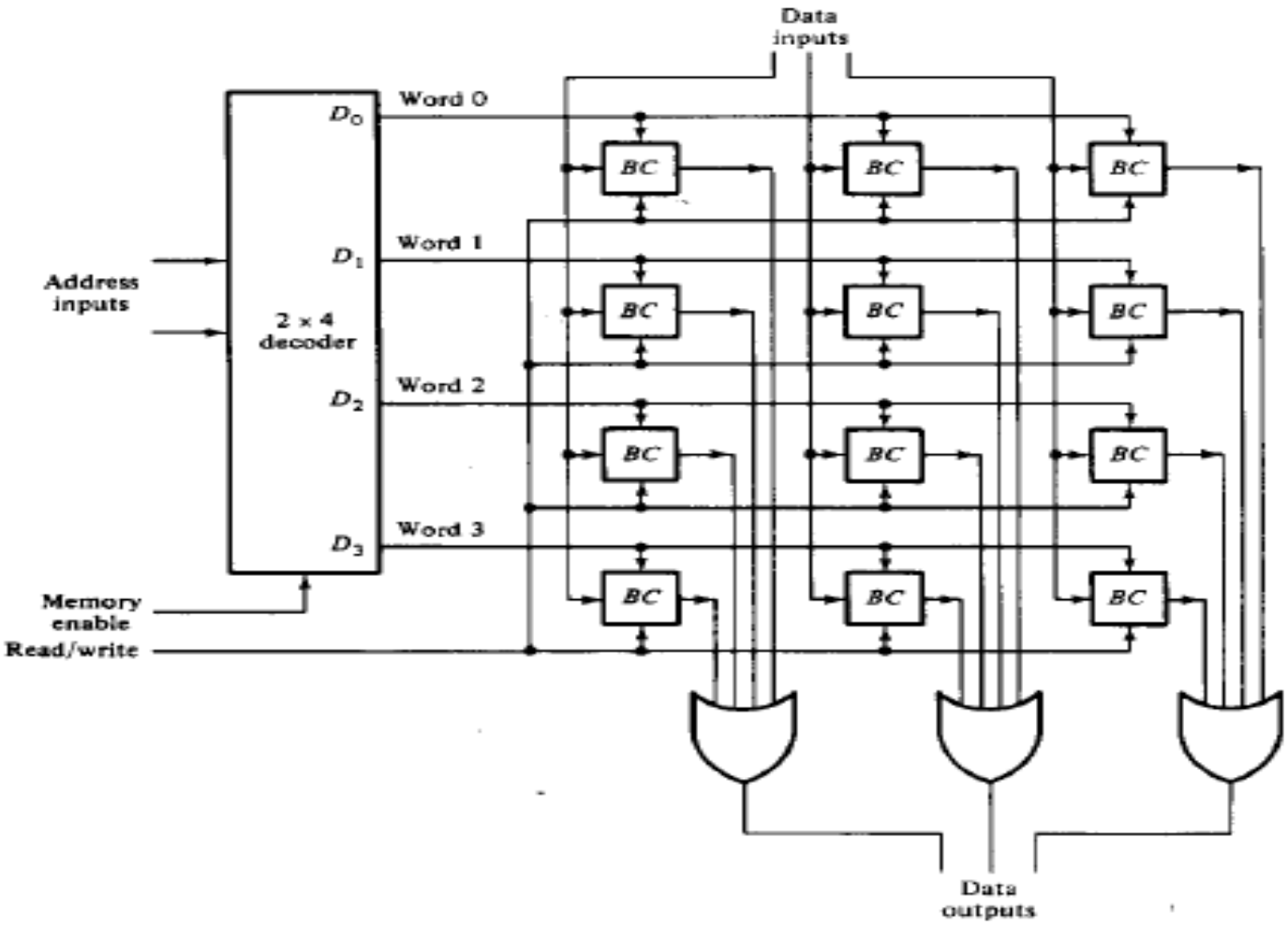


FIGURE 7-27
Logical construction of a 4 × 3 RAM

1K X 8 RAM

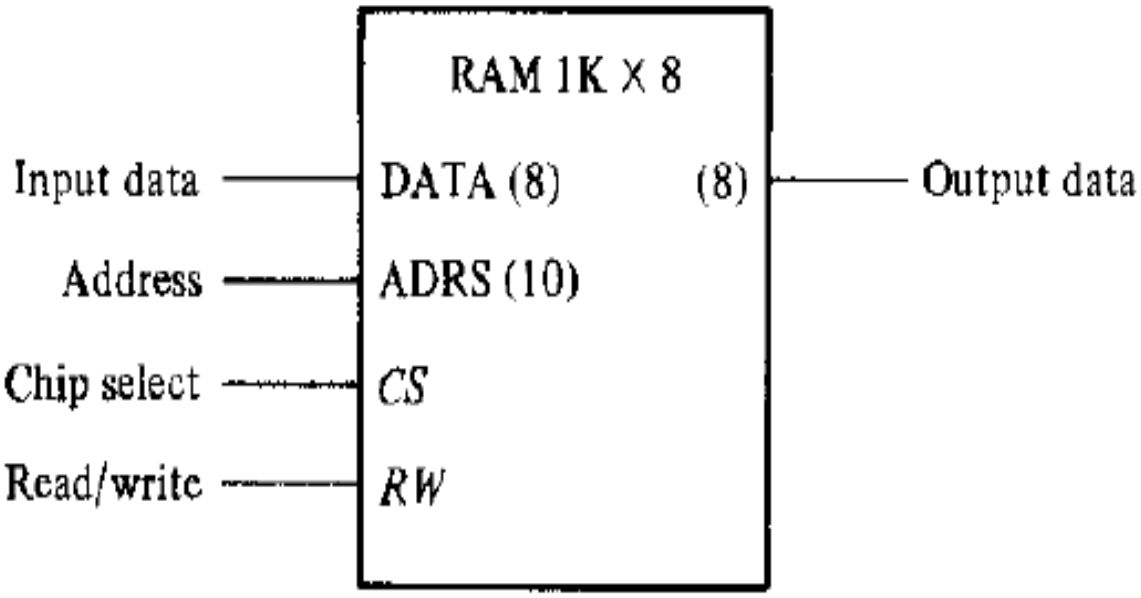
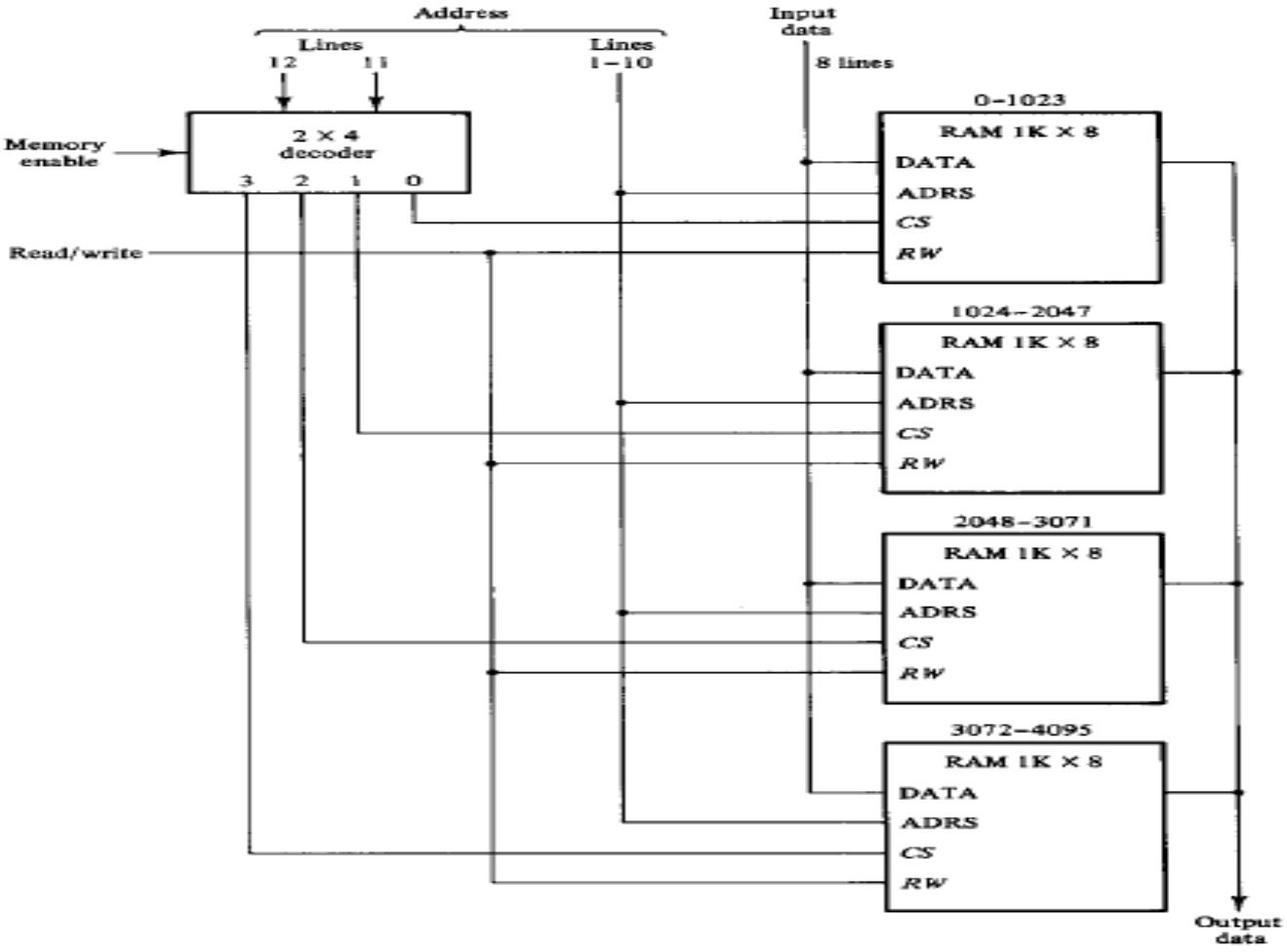


FIGURE 7-28

Block diagram of a 1K × 8 RAM chip.

4K X 8 RAM


Address
Lines
12 11
Lines
1–10
Input
data
8 lines
Memory
enable
2 × 4
decoder
3 2 1 0
Read/write
0–1023
RAM 1K × 8
DATA
ADRS
CS
RW
1024–2047
RAM 1K × 8
DATA
ADRS
CS
RW
2048–3071
RAM 1K × 8
DATA
ADRS
CS
RW
3072–4095
RAM 1K × 8
DATA
ADRS
CS
RW
Output
data

1K X 16 RAM

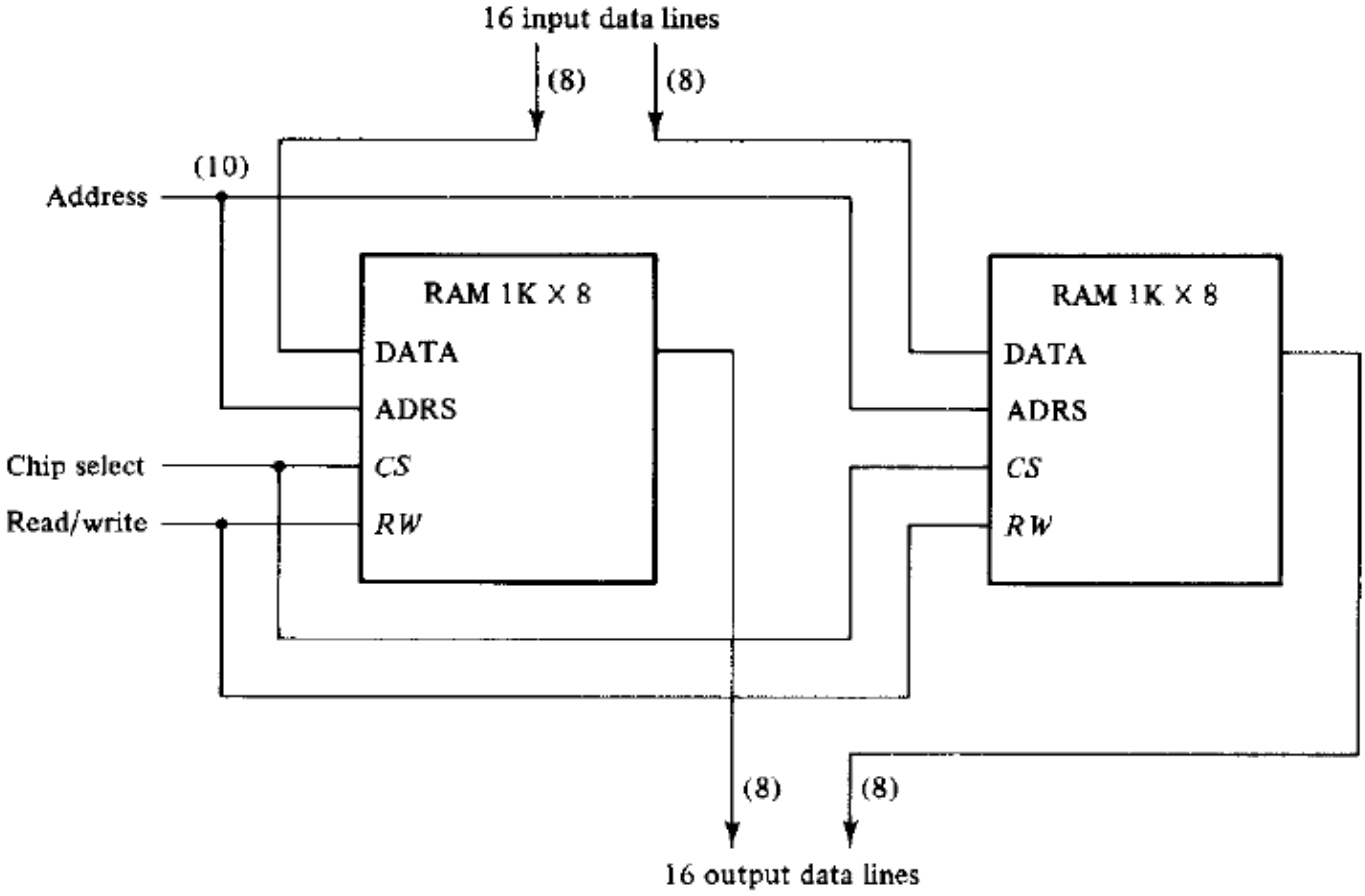


FIGURE 7-30
Block diagram of a 1K × 16 RAM.