Date:

EXPERIMENT NO. 7

AIM: Design, Implement & verify the operation of (I) 4:1 multiplexer and (II) 2 x 4 Decoder

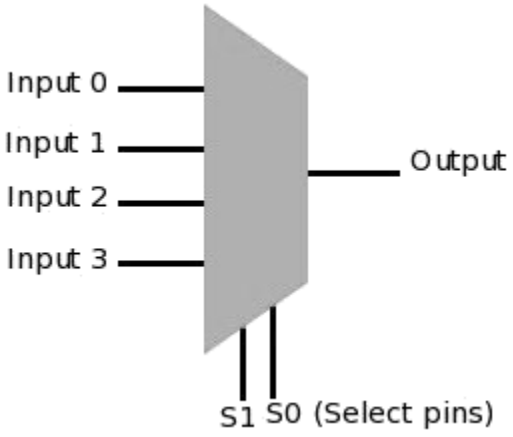
APPARATUS: Logic Gates (AND Gate, OR Gate, NOT Gate) (IC 7408, IC7432, IC 7404), Connecting wires, Bread Board, Power supply, LED, DMM.

SIMULATION WEBSITE: https://www.tinkercad.com/

THEORY:

4 x 1 Multiplexer

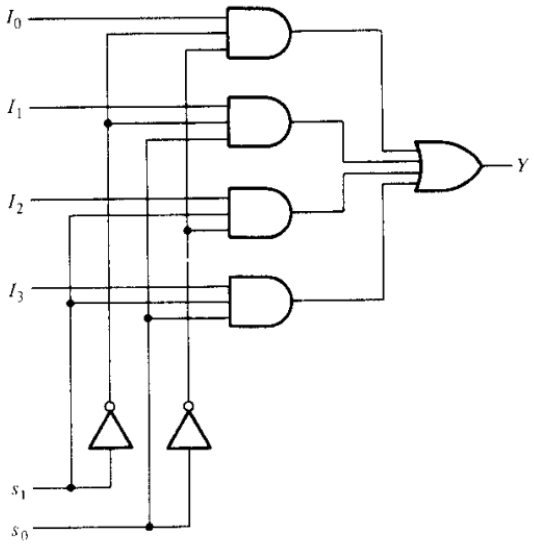
4x1 Multiplexer has four data inputs I3, I2, I1 & I0, two selection lines S1 & S0 and one output Y. The block diagram of 4x1 Multiplexer is shown in the following figure.One of these 4 inputs will be connected to the output based on the combination of inputs present at these two selection lines. Truth table of 4x1 Multiplexer is shown below.



Function Table:

Selection Lines		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Logic Diagram:



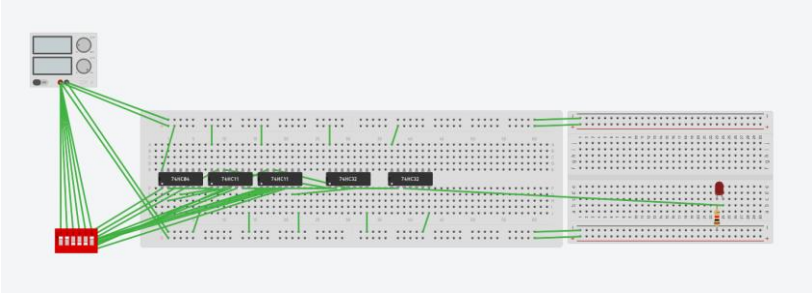
PROCEDURE:

i) Do the connection as per logic diagram.
ii) Apply proper input condition and observe the output information of led on/off.
iii) Compare theoretical data with observation and write conclusion.

OBSERVATION TABLE:

Serial No.	S0	S1	I0	I1	I2	I3	Output
1							
2							
3							
4							
5							
6							
7							
8							

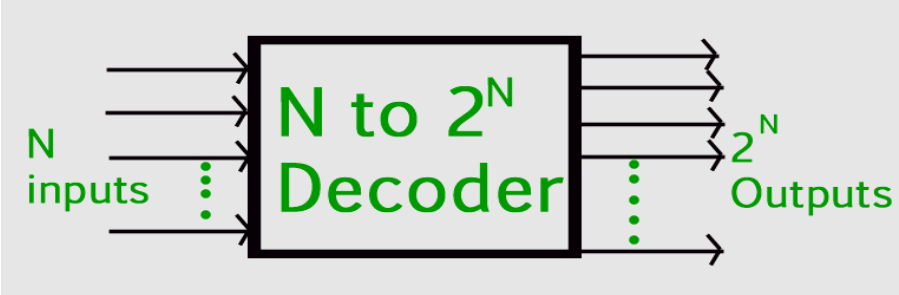
OBSERVATION:



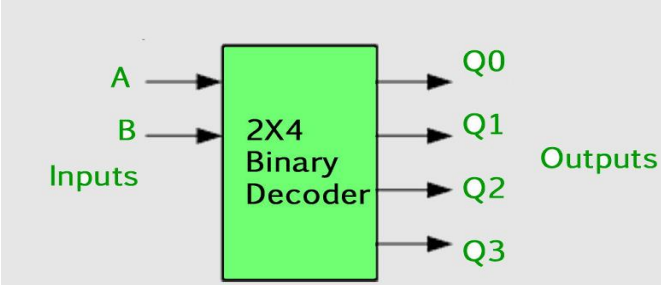
(ii) 2 to 4 binary decoder.

The name "Decoder" means to translate or decode coded information from one format into another, so a digital decoder transforms a set of digital input signals into an equivalent decimal code at its output

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.



The 2-to-4 line binary decoder depicted above consists of an array of four AND gates. The 2 binary inputs labelled A and B are decoded into one of 4 outputs, hence the description of 2-to-4 binary decoder. Each output represents one of the minterms of the 2 input variables, (each output = a minterm).

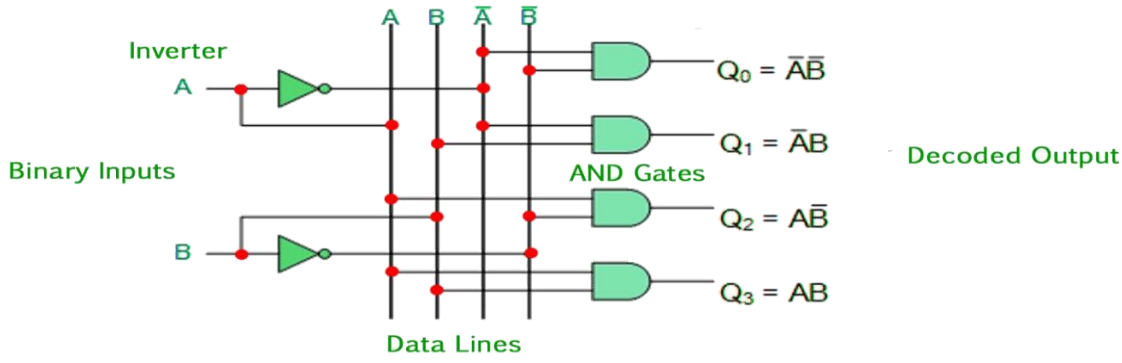


Function Table:

A	B	Q0	Q1	Q2	Q3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Boolean Functions: Q3= AB, Q2=AB', Q1=A'B, Q0=A'B'

Logic Diagram:



The binary inputs A and B determine which output line from Q0 to Q3 is "HIGH" at logic level "1" while the remaining outputs are held "LOW" at logic "0" so only one output can be active (HIGH) at any one time.

Therefore, whichever output line is "HIGH" identifies the binary code present at the input, in other words it "decodes" the binary input. Some binary decoders have an additional input pin labelled "Enable" that controls the outputs from the device.

This extra input allows the decoders outputs to be turned "ON" or "OFF" as required. Output is only generated when the Enable input has value 1; otherwise, all outputs are 0. Only a small change in the implementation is required: the Enable input is fed into the AND gates which produce the outputs.

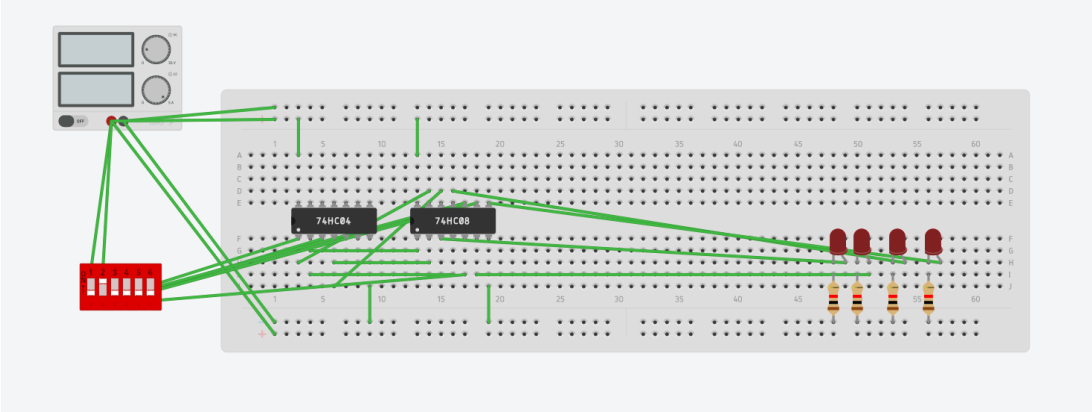
If Enable is 0, all AND gates are supplied with one of the inputs as 0 and hence no output is produced. When Enable is 1, the AND gates get one of the inputs as 1, and now the output depends upon the remaining inputs. Hence the output of the decoder is dependent on whether the Enable is high or low.

PROCEDURE:

i) Do the connection as per logic diagram.
ii) Apply proper input condition and observe the output information of led on/off.
iii) Compare theoretical data with observation and write conclusion.

OBSERVATION TABLE:

Serial No.	A	B	Q0	Q1	Q2	Q3
1						
2						
3						
4						



Obtai Marks:

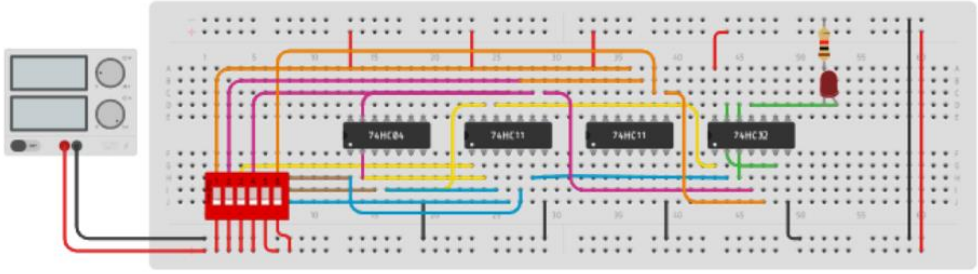
Faculty Sign:

Date:

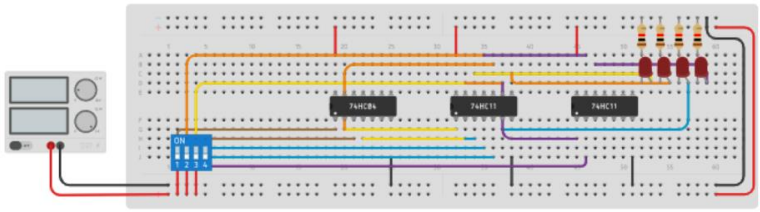
ASSIGNMENT:

1. Simulate 4 to 1 Multiplexer and 1 to 4 Demultiplexer experiment on http://vlabs.iitb.ac.in/vlabs-dev/labs/digital-electronics/experiments/implementation-of-multiplexer-demultiplexer-iitr/index.html and show results.

Ans. 4 to 1 multiplexer

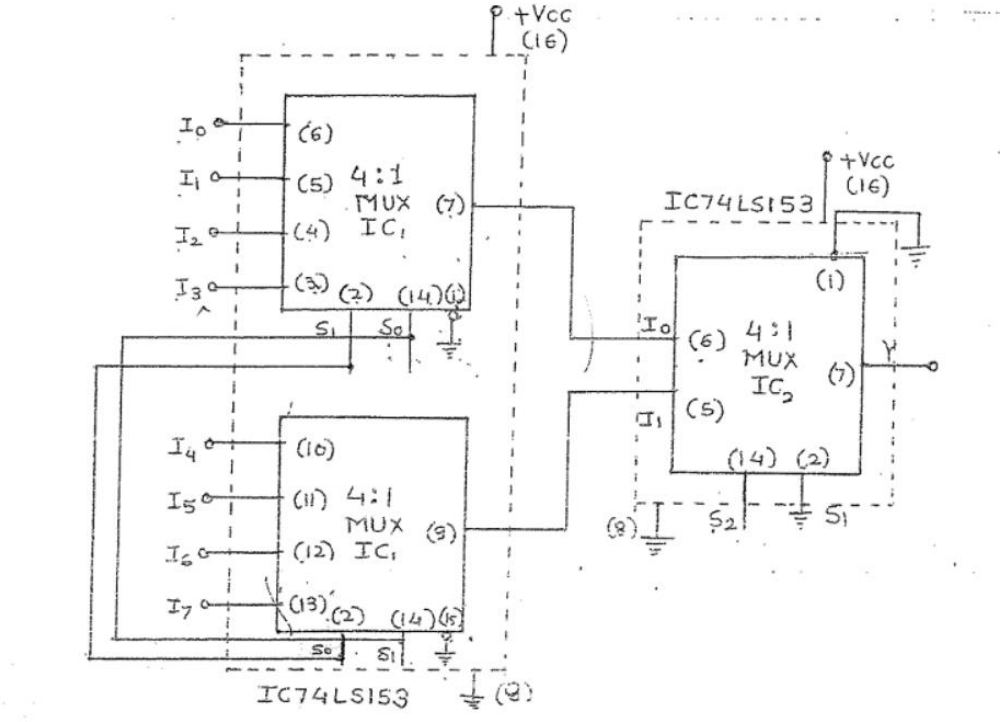


1 to 4 demultiplexer



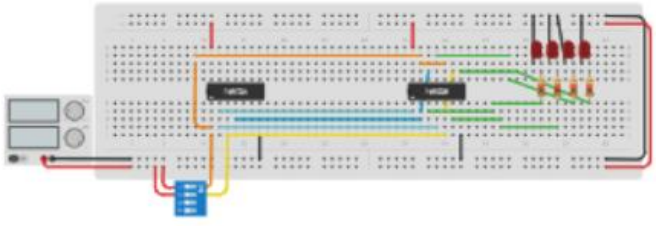
2. Draw pin diagram of IC 74LS151and explain how it can be used for 8 to 1 Multiplexing.

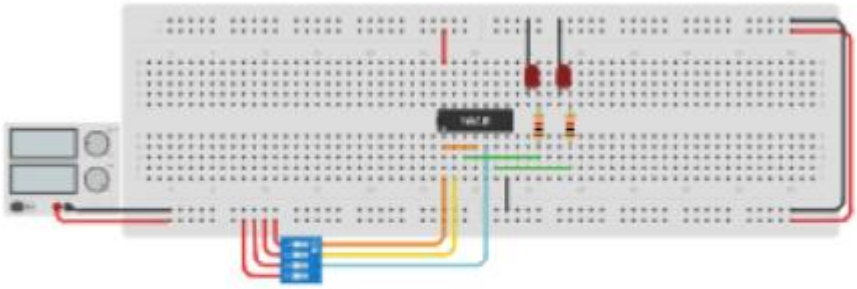
Ans.



3. Simulate 2 to 4 Decoder and 4 to 2 Encoder experiment on http://vlabs.iitb.ac.in/vlabs-dev/labs/digital-electronics/experiments/verification-decoder-demultiplexer-encoder-iitr/theory.html and show results.

Ans





4.Implement Full adder circuit with 3 to 8 decoder and OR gates.

Ans.