CHARUSAT
CHAROTAR UNIVERSITY OF SCIENCE AND TECHNOLOGY

MICROPROCESSOR ARCHITECTURES AND ASSEMBLY LANGUAGE PROGRAMMING

Chapter – 8

80186 Processor

DEPSTAR
Devang Patel Institute of Advance Technology and Research

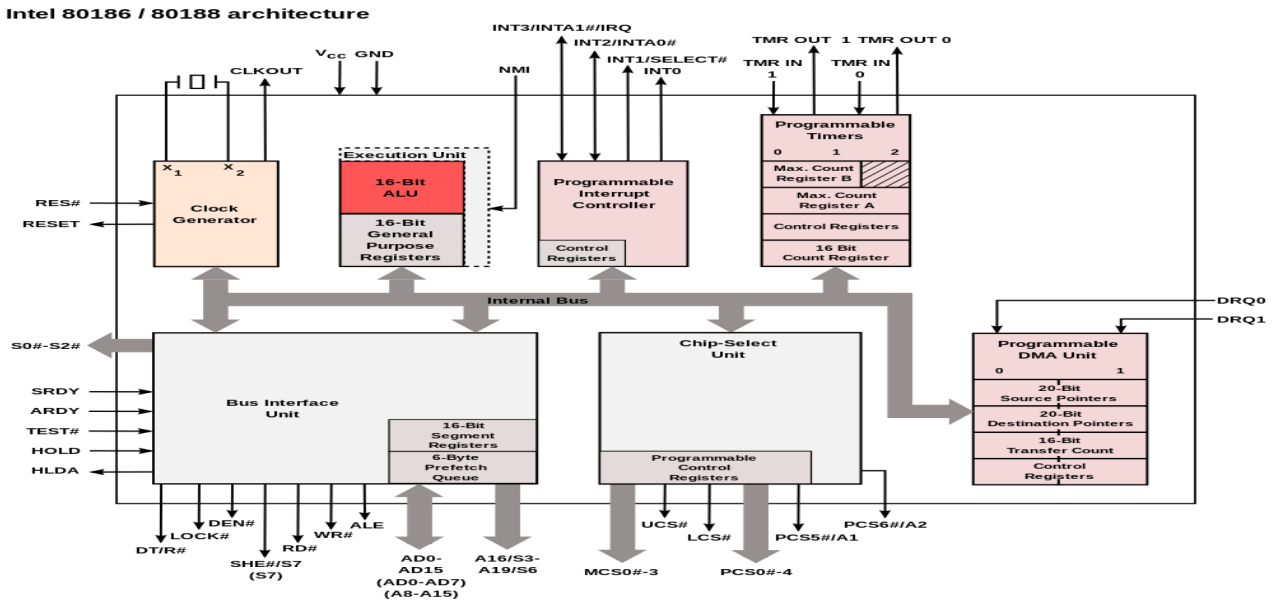
Basic Features

- The 80186 contains 16 – bit data bus
- The internal register structure of 80186 is virtually identical to the 8086
- About the only difference is that the 80186 contain additional reserved interrupt vectors and some very powerful built-in I/O features
- Double performance than 8086
- 80186=8086+several additional chips
- 16 bit data bus and 20 bit address bus
- Total addressable memory size 1 MB

Functional Block

- Bus Interface unit
- Execution unit
- Clock generator
- Programmable Interrupt Controller
- Timers:
- Programmable DMA Unit
- Programmable chip selection unit
- Power save/Power Down Feature
- Refresh Control Unit

Architecture of 80186



Clock Generator:

- The internal clock generator replaces the external 8284A clock generator used with the 8086 microprocessors. This reduces the component count in a system.
- The internal clock generator has three pin connections: X1, X2, and CLKOUT.
- The X1 (CLKIN) and X2 (OSCOUT) pins are connected to a crystal that resonates at twice the operating frequency of the microprocessor.
- In the 8 MHz version of the 80186/80188, a 16 MHz crystal is attached to X1 (CLKIN) and X2 (OSCOUT).
- The 80186/80188 is available in 6 MHz, 8 MHz, 12 MHz, 16 MHz, or 25 MHz versions.
- The CLKOUT pin provides a system clock signal that is one half the crystal frequency, with a 50% duty cycle.
- The CLKOUT pin drives other devices in a system and provides a timing source to additional microprocessors in the system.

Bus Interface unit

- Provides various functions, including generations of the memory and I/O address for the transfer of data between outside the CPU and EU
- Prefetch queue is used for prefetching instruction
- The 80186 has the same bus interface unit (BIU) and execution unit (EU) as the 8086.
- The 80186 is 68 pins lead-less package, so it has enough pins to send out both the minimum mode type signals RD and WR and the S0 – S3 status signals which can be connected to external bus controller ICs for maximum mode systems.
- It does not have a pin labelled MN/MX for switching minimum mode through maximum mode.

Programmable Interrupt Controller:

- The PIC arbitrates all internal and external interrupts and controls up to two external 8259A PICs. When an external 8259 is attached, the 80186 microprocessors function as the master and the 8259 functions as the slave.
- If the PIC is operated without the external 8259, it has five interrupt inputs: INTO–INT3 and NMI.
- But by connecting 8259 with CPU, we can increase the interrupt handling capability.
- 8259 combines the multi interrupt input sources into a single interrupt output.
- Interfacing of single PIC provides 8 interrupts inputs

Timers:

- The timer section contains three fully programmable 16-bit timers
- The timers 0 and 1 generate wave-forms for external use and driven by either the master clock of the 80186 or by an external clock
- The third timer, timer 2 is internal and clocked by the master clock only.
- The output of timer 2 generates an interrupt after a specified number of clocks and can provide a clock to the other timers. Timer 2 can also be used as a watchdog timer because it can be programmed to interrupt the microprocessor after a certain length of time.

Programmable DMA Unit:

- For the execution of a computer program, it requires the synchronous working of more than one component of a computer.
- For example, Processors – providing necessary control information, addresses…etc, buses – to transfer information and data to and from memory to I/O devices…etc. The interesting factor of the system would be the way it handles the transfer of information among processor, memory and I/O devices.
- Usually, processors control all the process of transferring data, right from initiating the transfer to the storage of data at the destination. This adds load on the processor and most of the time it stays in the ideal state, thus decreasing the efficiency of the system.
- To speed up the transfer of data between I/O devices and memory, DMA controller acts as station master.
- DMA controller transfers data with minimal intervention of the processor.

Programmable chip selection unit:

- The chip selection is a built-in programmable memory and I/O decoder.
- It has 6 output lines to select memory, 7 lines to select I/O.
- When an engineer needs to connect several devices to the same set of input wires (e.g., a computer bus), but retain the ability to send and receive data or commands to each device independently of the others on the bus, they can use a chip select.
- The chip select is a command pin on many integrated circuits which connects the pins on the device to the internal circuitry of that device.

Programmable chip selection unit:

- When the chip select pin is held in the inactive state, the chip or device is "deaf", and pays no heed to changes in the state of its other input pins; it holds its outputs in the high impedance state, so other chips can drive those signals.
- When the chip select pin is held in the active state, the chip or device assumes that any input changes it "hears" are meant for it, and responds as if it is the only chip on the bus. Because the other chips have their chip select pins in the inactive state, their outputs are high impedance, allowing the single selected chip to drive its outputs.

Power save/Power Down Feature:

- The power save feature allows the system clock to be divided by 4, 8, or 16 to reduce power consumption
- The power saving feature is started by software and exited by a hardware event such as an interrupt.
- The power down feature stops the clock completely.
- The power down mode is entered by execution of an HLT instruction and is exited by any interrupt.

Instruction and Instruction Set

- An instruction is the basic command, in other words it is the most simple programming command.
- Instruction set refers to the set of all the instructions that can be executed by a microprocessor.
- Instruction = Op-Code + Operands
- Op-Code identifies the action to be taken and operands specify source and destination.
- Op-Codes are also referred to as mnemonic, written in abbreviated form for ex: “mov” is used for copy the content from location to another location.
- Instructions can use CPU register(including accumulator), memory locations or I/O ports as per need.
- Simple instruction format :**op-code destination, source** like : mov ax, bx (comma separated.)

Instruction Set

– 80186 instruction set consists of the following instructions:

1. Data moving instructions.
2. Arithmetic - add, subtract, increment, decrement and compare.
3. Logic - AND, OR, exclusive OR, shift/rotate and test.
4. String manipulation - load, store, move, compare and scan for byte/word.
5. Control transfer - conditional, unconditional, call subroutine and return from subroutine.
6. Input/Output instructions.
7. Other - setting/clearing flag bits, stack operations, software interrupts, etc.

Instruction Set