Indian Institute of Information Technology, Nagpur

CMOS Design
Project
DC Signal Generator

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Project: Designing a DC Signal Generation Circuit using MicroWind.

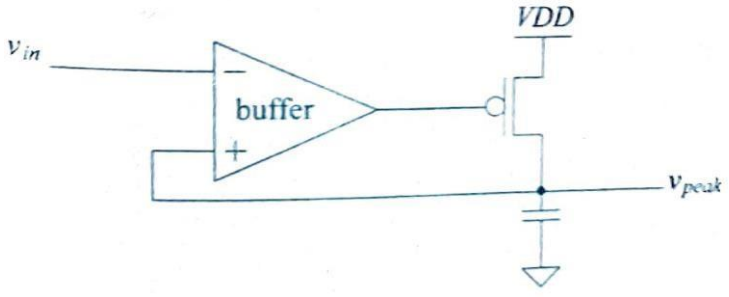
Theory:

DC Signal Generator

A DC Generator circuit is a analog circuit which converts a pulsating input into a constant DC output. For achieving this result we are using peak detectors made using CMOS peak detectors arranged in such a way that one detects peak of the pulse and other detects valleys of the pulse.

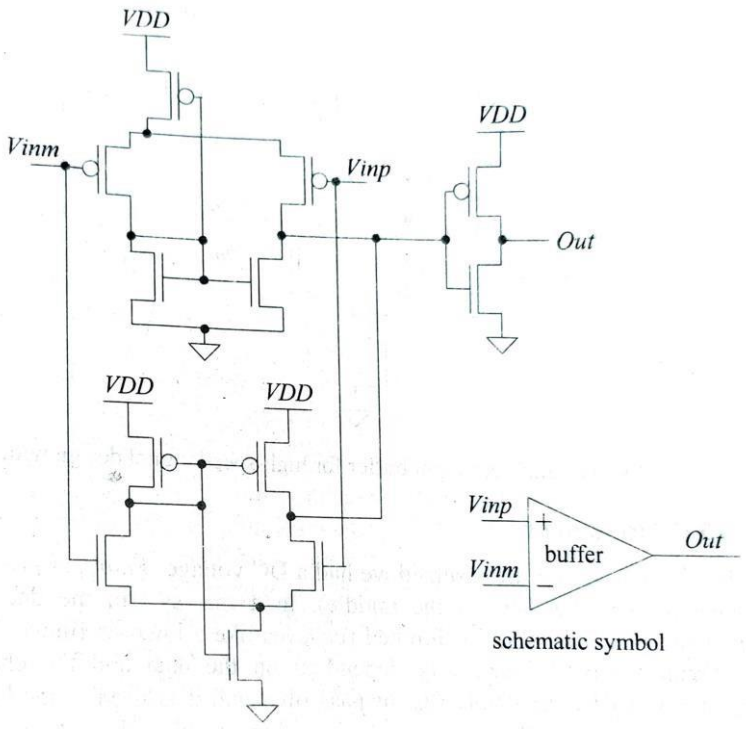
When the input Vin, goes above the voltage stored in the capacitor, Vpeak, the output of the buffer goes low, turning on the long-length MOSFET and pulling the output towards VDD. As Vpeak approaches Vin, the MOSFET starts to shut off. As a result the output voltage across the capacitor, Vpeak, corresponds to the peak voltage of the input signal. This peak detector can be used to generate a reference voltage that falls within the middle of the input data, Figure 5. The peak and valley detectors are used to find the minimum and maximum of the input signal. The Two resistors average the minimum voltages and feed the result (the DC average of the input) to the bottom buffer circuit. The resistors also are used to leak charge on off of the capacitor so that the averaging circuit can follow changes in the input data.

Figure 1: CMOS peak detector



Buffer:

Figure 2: Rail to Rail input/output buffer



Listing 1: Buffer

```
**Buffer
Vdd 1 0 dc 5V
Vinp 2 0 pulse (0 5 0 0 0 5ms 10ms)
Vinm 3 0 pulse (5 0 0 0 0 5ms 10ms)
m1 5 4 0 0 nmod w=40u l=1u
m2 4 2 5 0 nmod w=40u l=1u
m3 6 3 5 0 nmod w=40u l=1u
m4 4 4 1 1 pmod w=100u l=1u
m5 6 4 1 1 pmod w=100u l=1u
m6 7 7 0 0 nmod w=40u l=1u
m7 6 7 0 0 nmod w=40u l=1u
m8 7 2 8 1 pmod w=100u l=1u
```

```
m9 6 3 8 1 pmod w=100u l=1u
m10 8 7 1 1 pmod w=100u l=1u m11 9 6 0 0 nmod w=40u l=1u
m12 9 6 1 1 pmod w=100u l=1u
.model nmod nmos Vto=1V Kp=200u
.model pmod pmos Vto=−1V Kp=80u
.tran 0.01ms 200ms
.control
run
plot V(2)
plot V(3)
plot V(9)
.endc .end
```

Figure 3: Input pulses for buffer

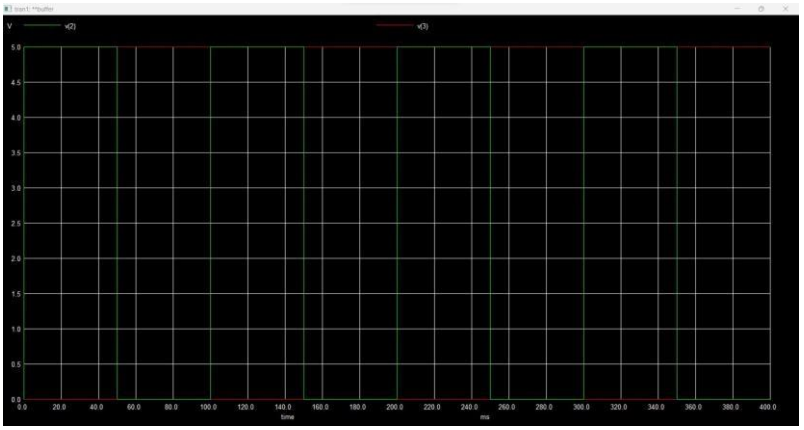
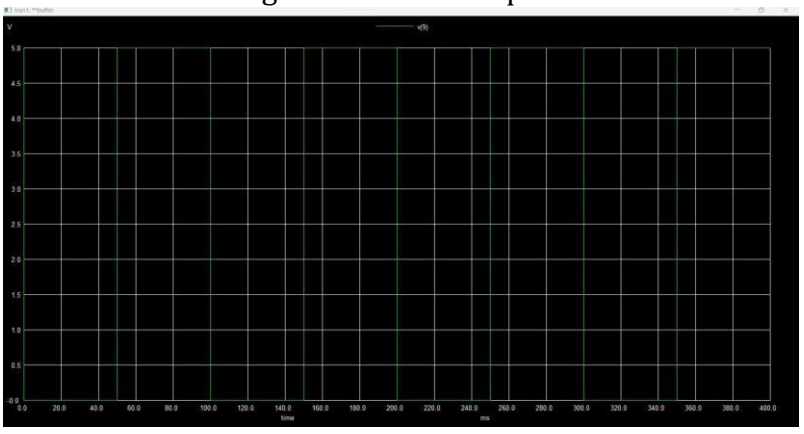
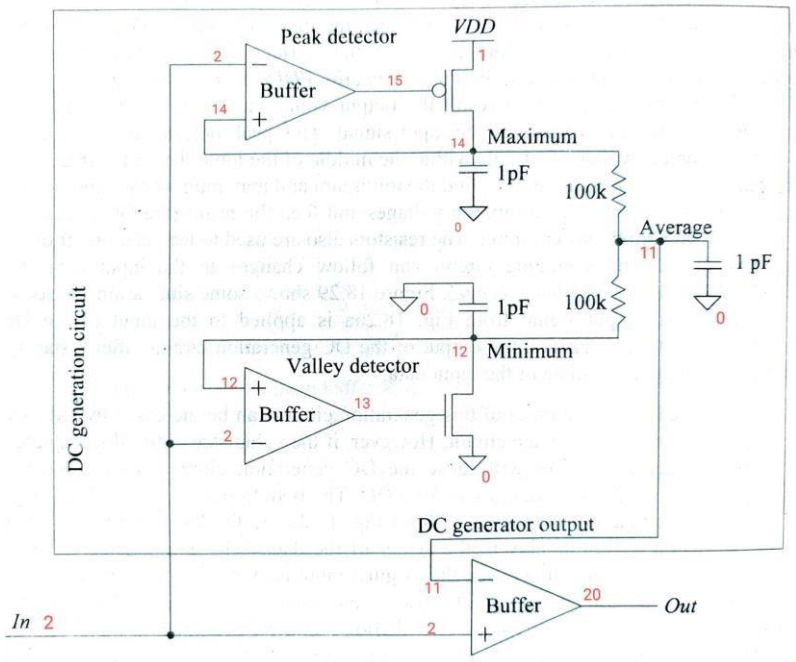


Figure 4: Buffer Output



DC Signal Generation Circuit

Figure 5: DC generation circuit



Layouts and Output:

Buffer Circuit :

Figure 8: Buffer Layout

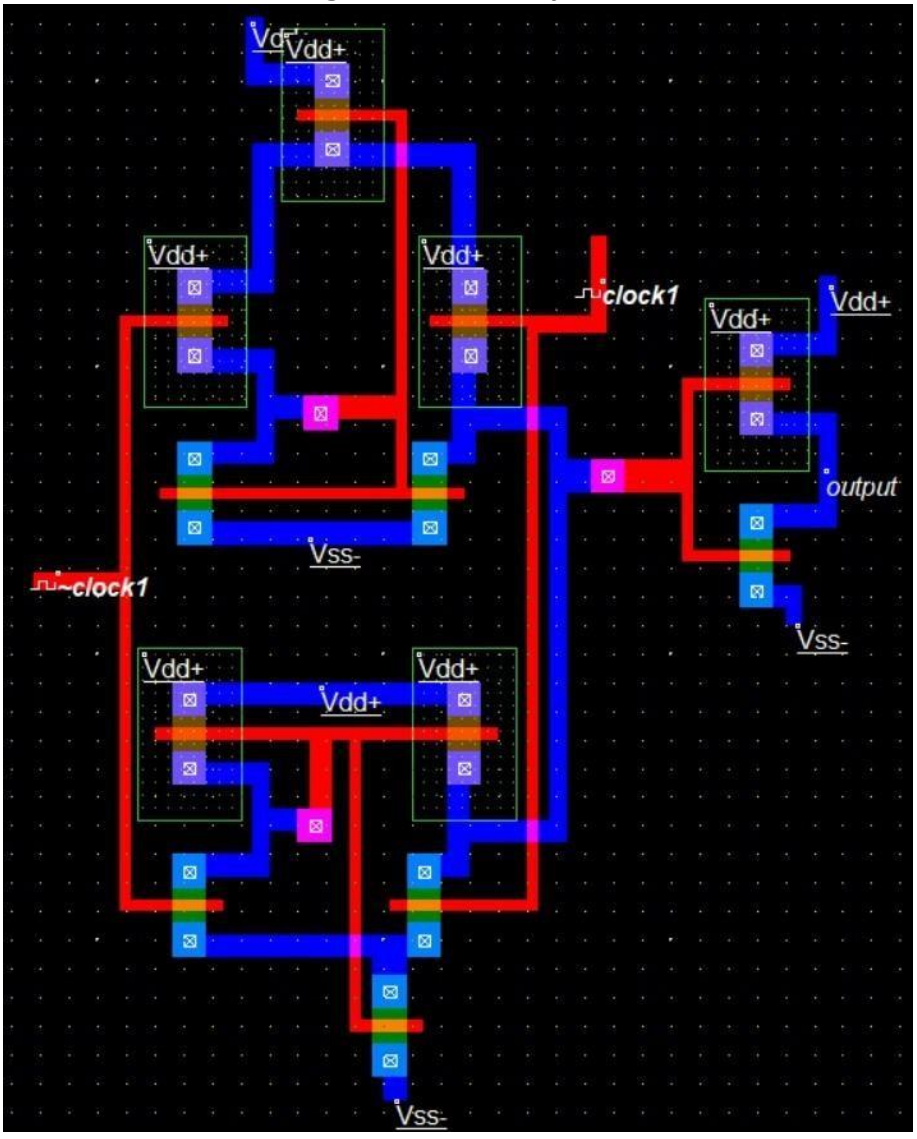


Figure 9: Buffer Output

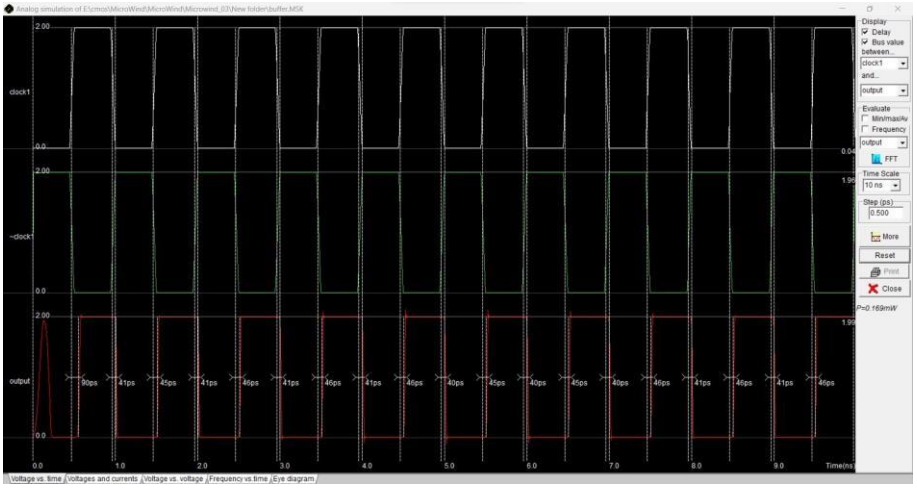


Figure 10: DC Generation Circuit Layout

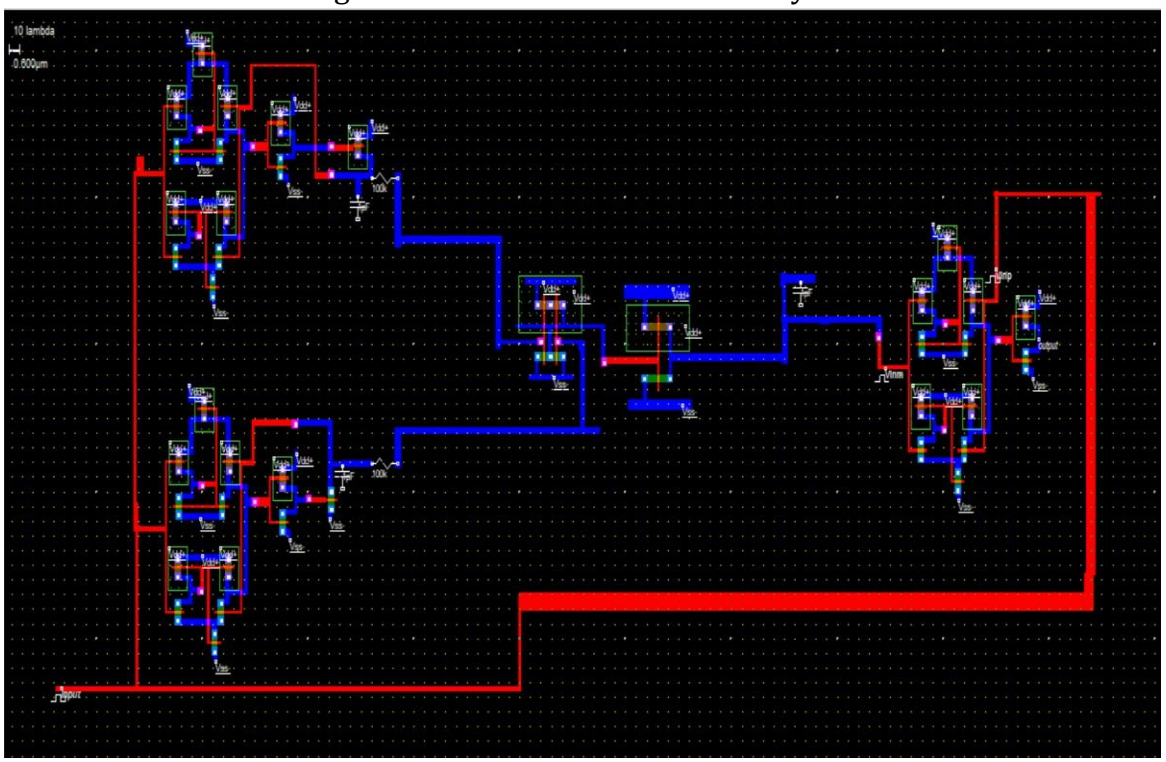
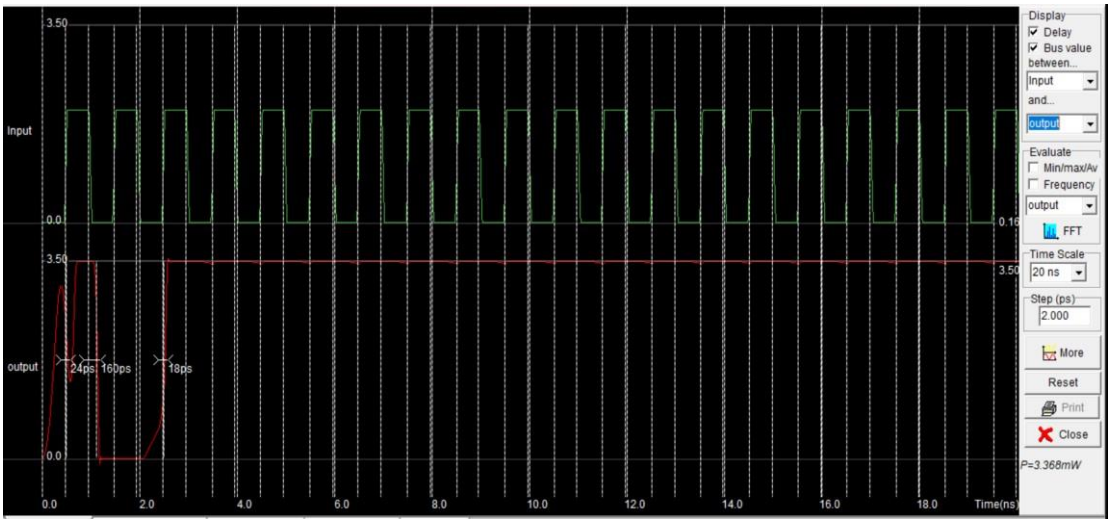


Figure 11: DC Generation Circuit Output



Conclusion:

Successfully implemented a DC generation circuit of power(p=3.368mV) for converting a pulse input to a DC voltage using a Rail to Rail input buffer. Successfully made the netlist for the buffer circuit and the DC generation circuit and also he layouts for the same.