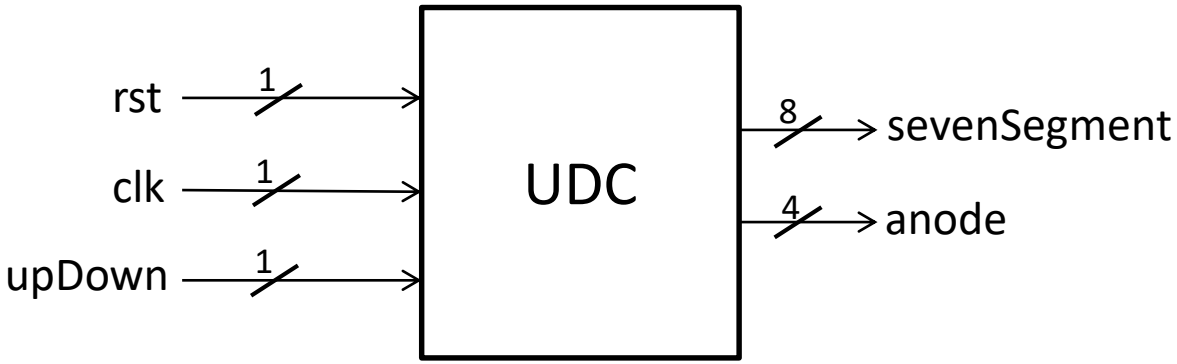
# One Digit Up-Down Counter (UDC)

# Design Description:

- On FPGA board we have 4 seven segments displays. For this design we want to implement up – down counter only using one of the seven segments display.
- It should count from 0 to 9 and 9 to 0 according to one of the input (upDown)

# Design I/O:

| | |
|---|---|
| **rst:** | 1 bit input for reset |
| **clk:** | 1 bit input for clock |
| **upDown:** | 1 bit input coming from a push-button |
| **sevenSegment:** | 8 bit output |
| **anode:** | 4 bit output |



# Design Behavior:

- Output anode should be assigned 4'b0111 to make active only one seven segment display out of 4.
- On seven segment display we should see 0 if rst signal is high, otherwise it should increment or decrement one by one depending on upDown input signal. If upDown is 1, it should increment and if upDown is 0, it should decrement.
- Do not forget to use delay module to slow down incrementing or decrementing. Otherwise numbers on display can not be seen.