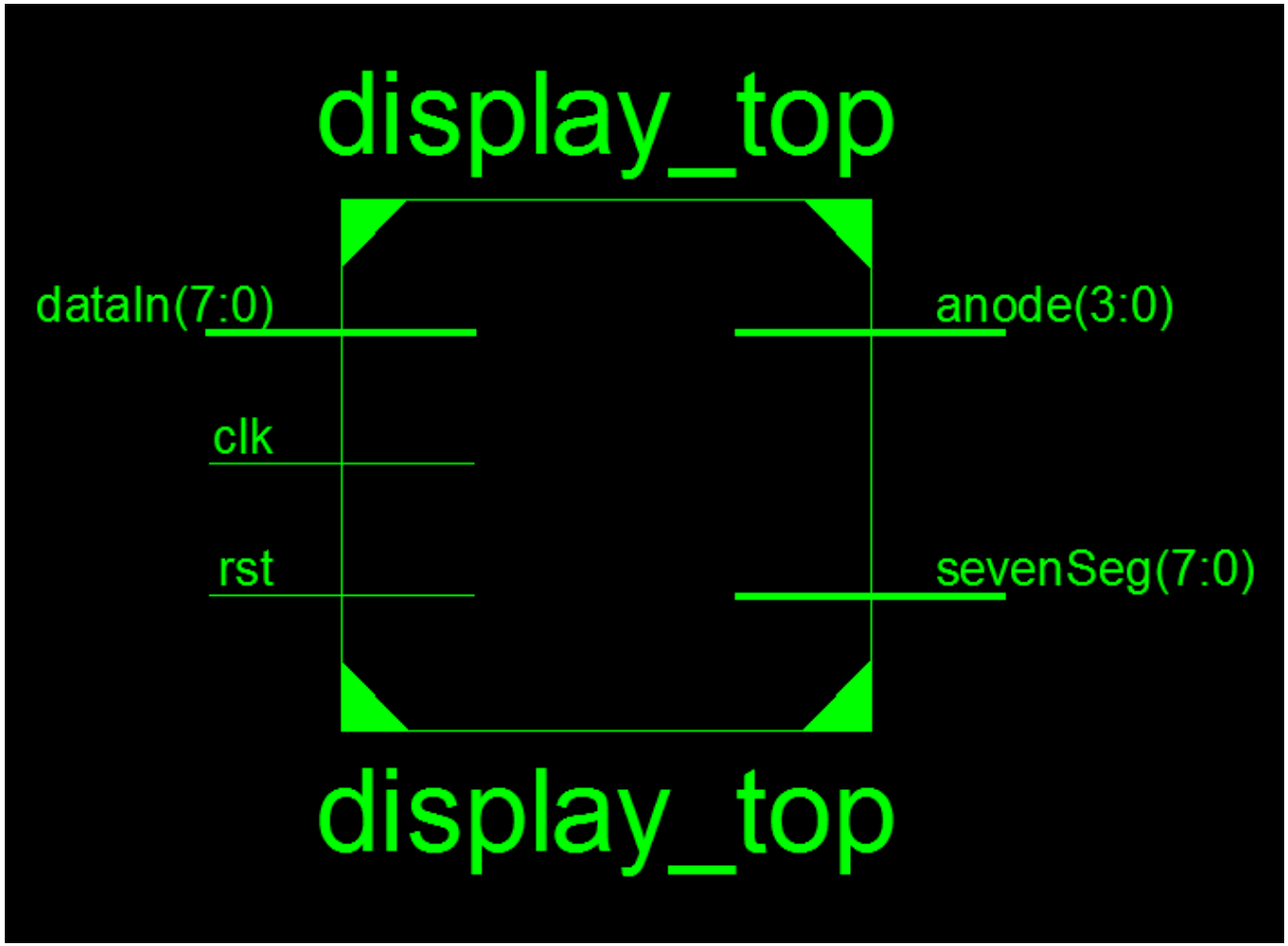
7 Segment Display Driver

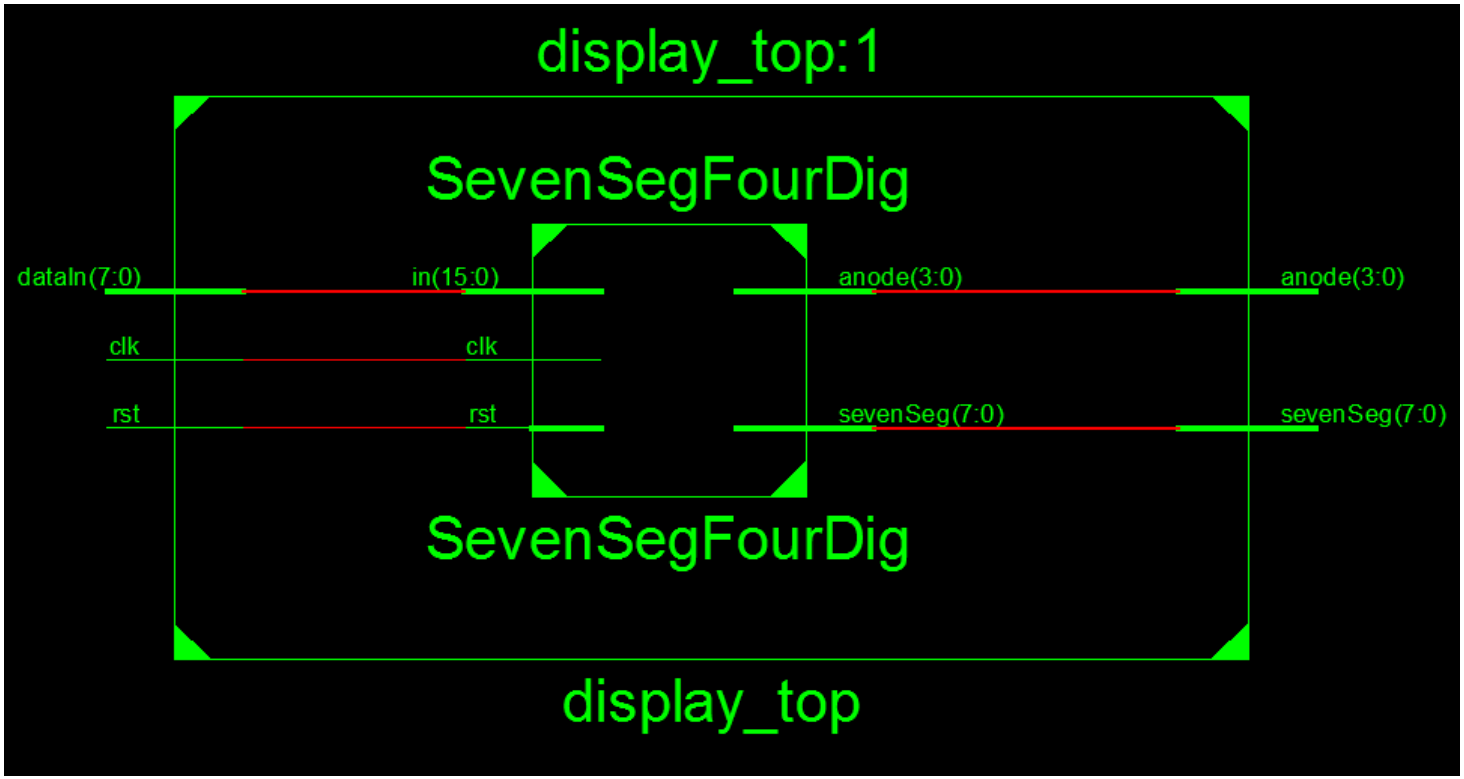
Design Top Level:



Design Top Level:

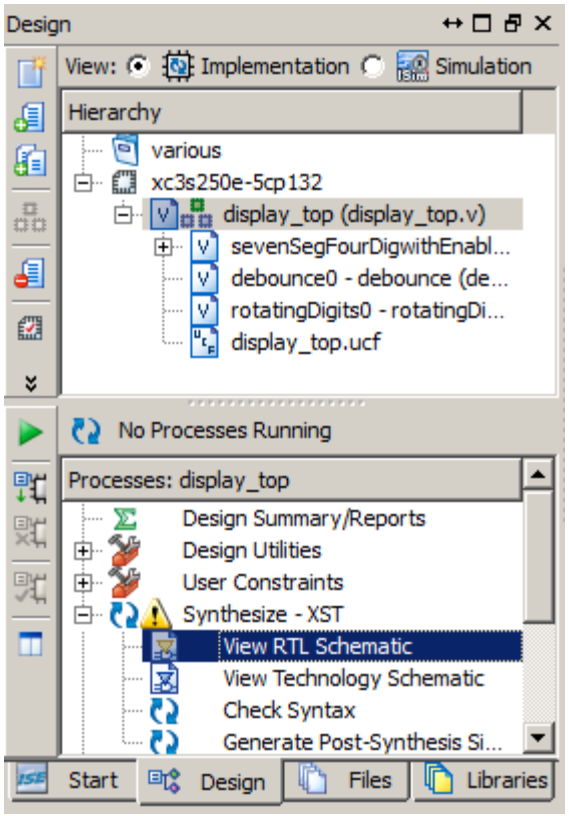
- Inputs
  - dataIn[7:0] will be tied to the switches (SW7-SW0) on the board.
  - clk will be connected to the clock pin.
  - rst will be connected to the button BTN0 on the board.
- Outputs
  - anode[3:0] will be connected to 7 segment anode pins.
  - sevenSeg[7:0] will be connected to each of the seven segment displays.

Submodule Connections:



Be aware that dataIn[7:0] is connected to in[15:0]. You should divide in[15:0] to 4 equal parts and connect the two highest bits to zero, while connecting the lower two bits to dataIn[n:n-1] pins.

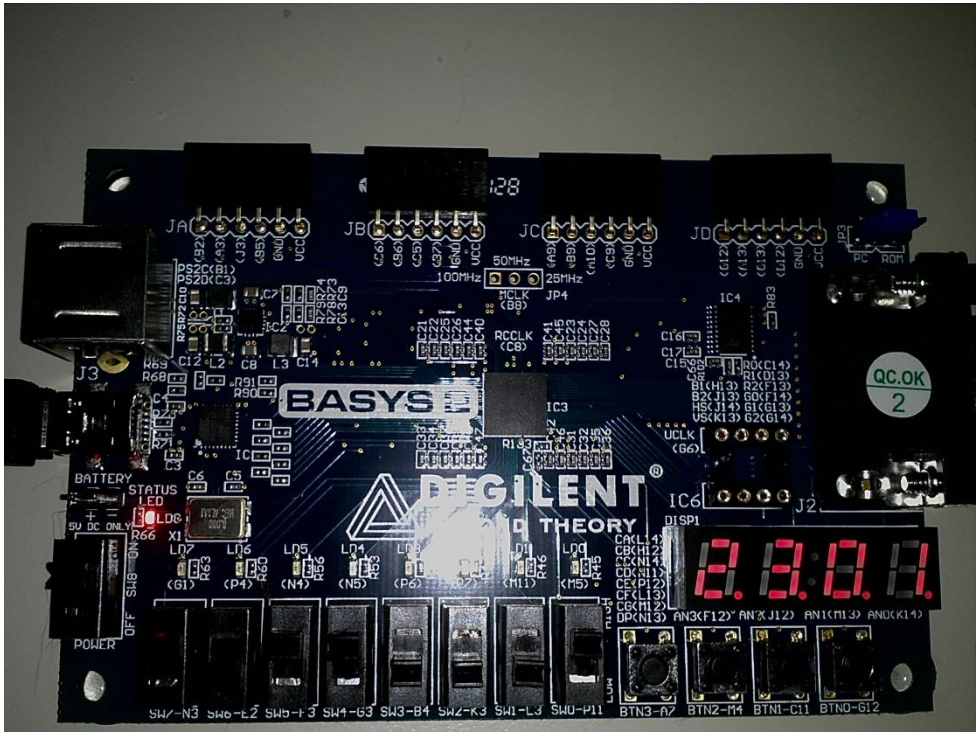
Viewing Schematics:



To see the schematics of your design:

- Select the «Design» tab on the left side of the screen
- Choose «Implementation» on «View» tab on the top.
- Select top level of your design on the «Hierarchy» section.
- In the «Processes» section just below «Hierarchy» section, expand «Synthesize – XST» and run «View RTL Schematic».

Design Behavior:



As it can be seen from the picture above, 4 different 2-bit data (max value = 3) will be entered from switches and the output should be observed on 7-Segment Display instantaneously.