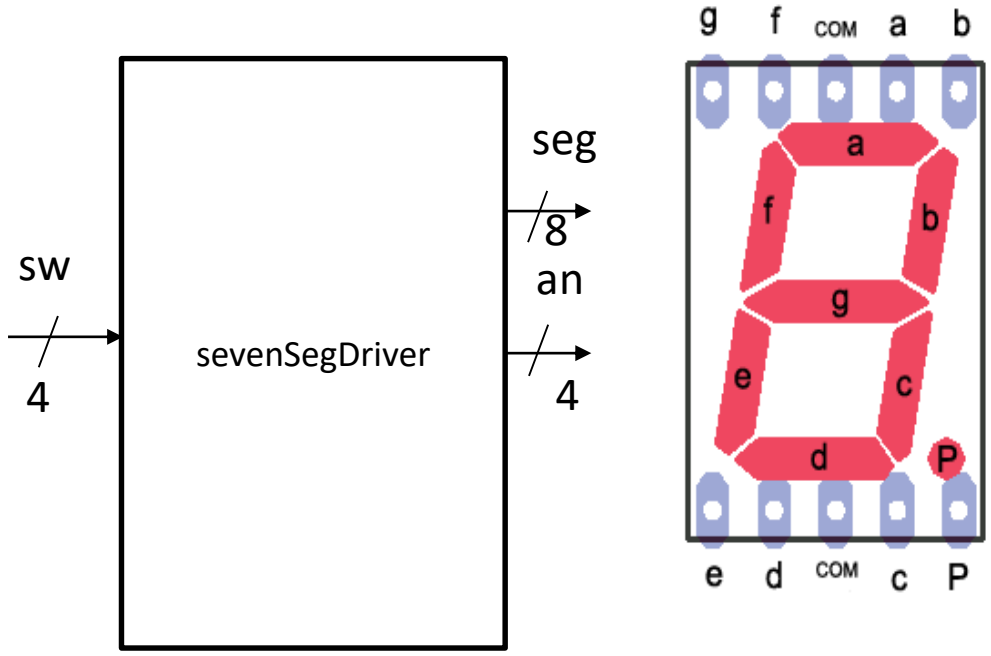
sw
4
sevenSegDriver
seg
8
an
4
g
f
COM
a
b
a
f
b
g
e
c
d
P
e
d
COM
c
P

Module Instantiation

```
module test(mclk, rst, …);
 input mclk;
 input rst;
…

 wire delayOut;
 delay delayModuleInstantiate1(.rst(rst),.mclk( mclk),.out(delayOut));


Endmodule
```

upDown Counter Design