Rotating Dot

Rotating Dot Circuit:

- This Verilog design code produces a circuit that outputs ‘Rotating Dot’ pattern.
- Display frequency of the circuit is adjustable via parameter COUNT.
- The design comes with a self-checking testbench, that takes frequency adjustments into account.
- There is also a .ucf file that can be used to synthesize the circuit on Digilent BASYS2 FPGA boards.

Design I/O:

- The circuit consists of 2 inputs and 1 output bus.
  - clk: clock input provided to the circuit.
  - rst: reset input provided to the circuit.
  - [7:0] dataOut: output bus provided from the circuit, this output bus will be connected to the leds on the FPGA.