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The University of Manchester

A Novel Approach to Modelling of MOS Devices – Development of a Simulation Tool for MOSFET Analysis

Third Year Individual Project – Final Report

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Contents

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Abstract

Metal oxide semiconductor field effect transistors (MOSFETs) have been the building block of high-performance electronics due to their innate speed and power advantages. The trend to shrink down the size of the MOSFETs allows the electronics to be smaller and more powerful and today, few nanometres long MOSFETs can be manufactured. One of the biggest challenges is the cost of initial manufacturing line in sub-micron dimensions.

Thus, the devices can be simulated using models before manufacture. Herein, I review the underlying semiconductor physics…

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1 Introduction

1.1 Background and motivation

The utilization of semiconductor materials has undeniably paved the way for the most significant milestones in the electronics industry. With the invention of first bipolar transistor in 1947, the modern electronics era started. At its core, these tri-terminal devices function as electrical switches, facilitating the execution of mathematical logic operations through the manipulation of voltage and current.

Preceding transistors, their predecessors, such as vacuum tubes also were used for digital computing, however, the use of semiconductor materials has allowed transistors to be much faster, use less power and become progressively smaller, down to nanometric scales today. By 1954, transistors had already replaced forty-eight years old vacuum tubes in many applications [1].

Building upon the success of transistors, further advancements emerged with the invention of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) in 1960. Unlike the bipolar transistors which are controlled by current, MOSFETs are controlled by electric field, thus allowing faster switching speeds. This attribute has propelled MOSFETs to the forefront of contemporary electronic applications. Today, they are predominantly used in all advanced integrated circuits, microprocessors, memory units and more [2].

In 1965, Gordon E. Moore observed that the density of transistors in integrated components was doubling every two years, indicating an exponential decrease in size [3]. This phenomenon owes its validity to the inherent semiconductor nature of these devices. Notably, Moore's Law, encapsulating this doubling trend, persists even 59 years later. As manufacturing complexities and rising fabrication costs pose challenges and signals Moore's Law's end, ongoing innovations, such as leveraging analog behaviours of semiconductor devices, sustains improvements in integrated circuit performance [4]. One constant in this evolving landscape is that technological advancement consistently results in an increase in the complexity of device physics.

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The initial fabrication cost for transistors of this size is notably high. As a result, the study of transistor modelling becomes crucial. In this project, various MOSFET models will be explored, simulations will be implemented for transistors of diverse sizes, and simulation results will be compared with actual measurements to emphasize the need for enhanced models in transistor simulation.

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1.2 Aims and Objectives

The primary objective of this project is building a MOSFET model and developing a tool capable of accurately simulating models for predicting the transfer and output characteristics of a commercial MOSFET. To achieve this overarching aim, the following specific objectives will be pursued:

1. MOSFET Modelling – Theoretical Background
- Propose a MOSFET model by introducing underlying semiconductor device behaviours.
2. Software Development
- Develop a standalone software capable of simulation based on user-provided parameters.
- Enable a plug-and-simulate functionality to incorporate user-defined models seamlessly.
3. Performance Evaluation
- Conduct real-data measurements using an actual MOSFET device.
- Compare the results obtained from the real-data measurements with those generated by the simulation software.

1.3 Project Overview

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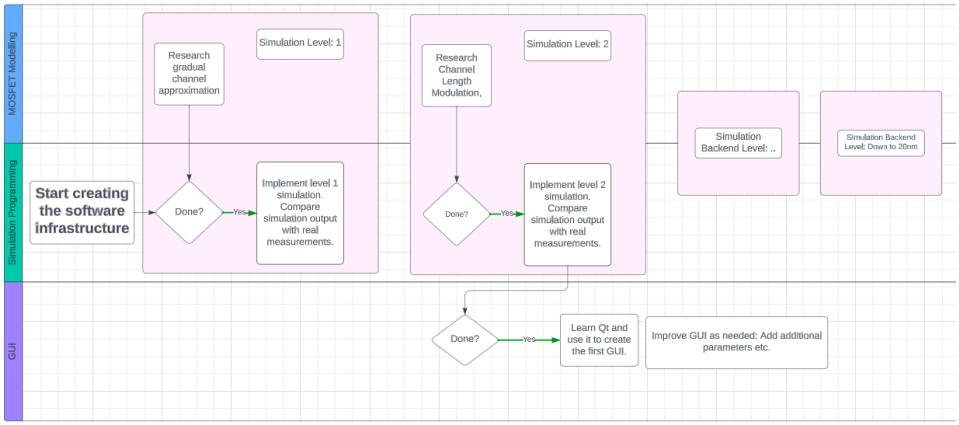

Figure 1 illustrates the project plan, categorized into three key sections: (top) Theoretical Research focusing on publicly available models for MOSFETs up to 20nm, (middle) Main Software Development Plan, and (bottom) GUI Development Plan.

2 Literature review

2.1 Introduction

This chapter employs a bottom-up approach to delve into MOSFET modelling. MOSFETs are semiconductor devices, so modelling them requires a solid grasp of underlying semiconductor physics. This chapter will explain many of the underlying properties of semiconductors except for crystallography. Starting with quantum mechanics and statistical mechanics, semiconductor's carrier concentration in equilibrium will be established. Then, effects of adding impurities to the semiconductor will be quantified. Finally, the movement mechanics of the carriers will be established, leading to characterization of voltage-current relationship. Parameters introduced and quantified in this chapter will be used to analyse devices utilizing semiconductors.

2.2 Quantum Mechanics Principles & Schrödinger Equation

To analyse any semiconductor device, moreover any electricity conducting device, electrons are the most fundamental unit that should be examined. While classical laws of physics yield high accuracy for the analyses of large objects, they become inadequate to describe the subatomic particles. For these particles, quantum mechanical principles are the backbones of their analysis. The quantum mechanics in its core has three principles [5]:

Energy is quantized in discrete packets called quanta and its energy is related to the frequency:

$$E = hf \quad (1)$$

Where E is the energy, h is the Planck's constant and f is the frequency.

Particles exhibit wavelike behaviour. The wavelength of a particle is related to its momentum.

$$\lambda = \frac{h}{p} \quad (2)$$

Where λ is the de Broglie wavelength of a particle and p is the momentum.

The momentum and the position of a particle cannot be described with absolute accuracy; the energy and the time that the particle has that energy cannot be described with absolute accuracy.

$$\Delta p \Delta x \geq \hbar \qquad \Delta E \Delta t \geq \hbar \quad (3)$$

Where Δp, Δx, ΔE, Δt are the uncertainties in momentum, position, energy, and time respectively. $\hbar$ is the reduced Planck's constant.

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$$\hbar = \frac{h}{2\pi} \quad (4)$$

Although these three principles govern quantum mechanics, to apply them and characterize a system's quantum-mechanical state, Schrödinger's time-independent equation should be solved.

$$\frac{d^2\psi}{dx^2} = -\frac{2m}{\hbar^2}(E - V(x))\psi(x) \quad (5)$$

Where ψ is the wavefunction that describes the quantum state of the system, E is the total energy of the particle, $V(x)$ is the potential experienced by the particle and m is the mass of the particle. In this paper, Schrödinger's equation will not be mathematically solved but rather the solutions will be examined to understand how electrons behave.

2.3 Electron Models

2.3.1 Classical Free Electron Model

This model relies on classical laws of physics and electrons are assumed to behave like a classical gas, adhering to the laws of kinetic theory and the electron energies are not quantized; they can take any value without quantum restrictions [6]. The classical free electron theory successfully verified Ohm's law, explained thermal and electrical conductivities. However, its reliance on classical mechanics hindered its ability to explain crucial properties in semiconductors and insulators.

2.3.2 Quantum Mechanical Electron Model – Potential Well

The Schrödinger's equation's solution for the potential well, illustrated in figure 2, has the following form.

$$\psi(x) = A_1 \sin(kx) + A_2 \cos(kx) \quad (6)$$

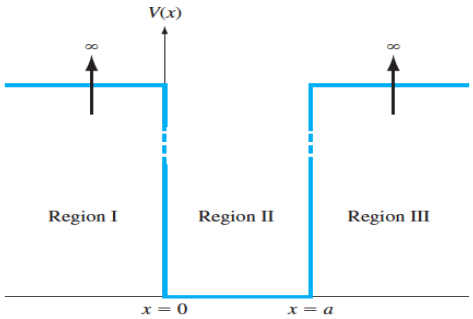

Figure 2 Diagram of the infinite potential well [5]

Where k is the wavenumber and represents the spatial frequency. To describe the energy of the system, k can be written in terms of energy using wave-particle duality.

$$k = \frac{2\pi}{\lambda} = \frac{2\pi}{\frac{\hbar}{p}} = \frac{p}{\hbar} = \sqrt{\frac{2mE}{\hbar^2}} \quad (7)$$

At the boundaries $x = 0$ and $x = a$ of the potential well, the wavefunction is evaluated:

$$\psi(0) = A_1 \sin(0) + A_2 \cos(0) = A_2 = 0 \quad (8)$$

$$\psi(a) = A_1 \sin(ka) + A_2 \cos(ka) = A_1 \sin(ka) = 0 \quad (9)$$

For any non-zero A_1

$$ka = \sqrt{\frac{2mE}{\hbar^2}}\, a = n\pi, \qquad n \in \mathbb{Z} \quad (10)$$

$$E = \frac{n^2\pi^2\hbar^2}{2ma^2} \quad (11)$$

The solution suggests that there are allowed energy levels for the electron to occupy. Allowed energy levels are illustrated in figure 3 for an infinite well with width L.

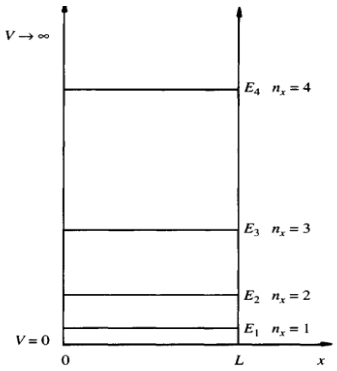

Figure 3 Distribution of allowed quantum levels in the potential well [7]

2.3.3 Band Theory of Solids

Moving from the isolated particle to crystalline solids is necessary to understand how electrons behave. When atoms come together in an arranged way to create a crystal, there exists a potential that is different to the potential well previously assumed. The most basic repeating pattern in a crystal is called the primitive cell. When the primitive cell is replicated in three dimensions the crystal lattice is formed [8]. This periodic structure creates a periodic potential across the volume of the solid. Even without solving the Schrödinger's equation for this potential, the conclusion of

bands and energy gaps could be achieved by applying the quantum mechanical electron model to a crystal lattice. Due to wave particle duality, electrons can be treated as waves, and so the electron waves interacting with the periodic potential creates destructive and constructive interferences.

A linear solid of lattice constant a, as illustrated in figure 4, can be examined to demonstrate the band formation. Bragg condition, which describes the reflections of a wave in a crystal lattice [9], is met at locations $k = \pm\frac{n\pi}{a}$. At these locations the traveling electron wave is reflected continuously, thus becoming a standing wave. At $k = \frac{\pi}{a}$ and $k = -\frac{\pi}{a}$, so called first Brillouin zone of this lattice.

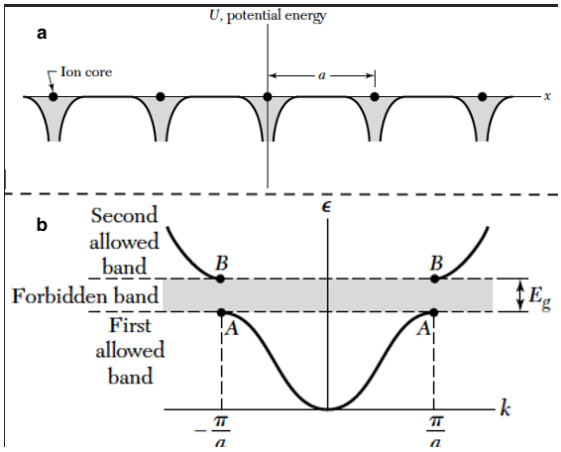

Figure 4 (a) The change in potential energy experienced by a conduction electron due to the ion cores in a linear lattice, (b) the energy bands due to first Brillouin zone edited [10]

For a quantitative description, the Schrödinger's equation is solved for a specific crystal's 3D potential and the solution yields to the specific E-k diagram of that crystal.

2.4 Electrical Conduction in Semiconductor Crystals

Electrical conduction is simply the existence of a net movement of charge carriers. An intrinsic semiconductor at 0 K has all valence electrons bonded to the neighbouring nuclei. As the temperature increases, the bonds break, i.e. the electron gains enough energy to jump to the higher energy level, conduction band, and thus can freely move through the crystal. When the electron jumps to the conduction band, generating a negative charge carrier, it also generates a hole, a positive charge carrier, in the valence band. Thus, in the semiconductor, electrical conduction can be due to the movement of a single negative charge carrier at the conduction

band or due to the collective recombination/generation of the carriers. To simplify the calculations the latter is assumed to be the movement of a single hole. In figure 5, E-k diagrams of GaAs and Si are illustrated and E_g is defined as the energy gap between the lowest level of conduction band and the highest level of the valence band.

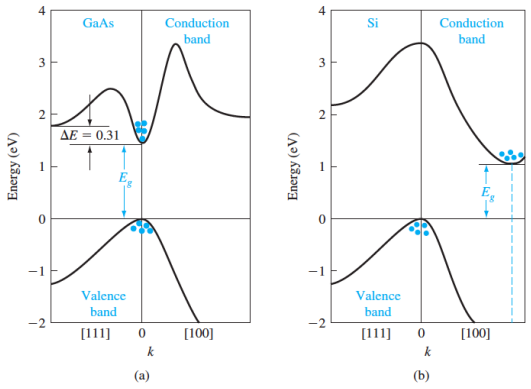

Figure 5 (a) E-k diagram of GaAs, (b) E-k diagram of Si [5]

The energy of a carrier is related to wavenumber, in 3D case wavevector, of that carrier (eq. 7). However, the E-k graphs found by solving to the Schrödinger's equation suggests that the mass of the particle changes as it moves through the lattice. This phenomenon is defined as the effective mass, m^*, and can be approximated using the curvature of the E-k diagram [5].

$$m^* = \frac{\hbar^2}{\frac{d^2E}{dk^2}} \tag{12}$$

2.5 Intrinsic Charge Carrier Concentration

Perhaps the most important parameter for a semiconductor is the charge carrier concentration. To find the charge carrier concentration, density of states, $g(E)$, and probability of state, $f(E)$, functions are simply integrated. Former giving the number of available quantum states and latter giving the probability of a state being occupied using Fermi-Dirac distribution.

Commented [DA6]: Informal

For electron charge carrier concentration in thermal equilibrium n_o:

$$g_n(E) = \left(\frac{2m_e^*}{h^2}\right)^{\frac{3}{2}} 4\pi\sqrt{E - E_c} \qquad \& \qquad f_n(E) = \frac{1}{1+\exp\frac{E-E_f}{k_BT}} \tag{13a, 13b}$$

$$n_0 = \int_{E_c}^{E_{c,max}} g_n(E) f_n(E) dE \approx 2\left(\frac{2\pi m_e^* k_B T}{h^2}\right)^{\frac{3}{2}} \exp\left(-\frac{E-E_f}{k_BT}\right) = N_c * \exp\left(-\frac{E-E_f}{k_BT}\right) \tag{14}$$

For hole charge carrier concentration in thermal equilibrium p_o:

$$g_p(E) = \left(\frac{2m_p^*}{h^2}\right)^{\frac{3}{2}} 4\pi\sqrt{E_V - E} \qquad \& \qquad f_p(E) = 1 - \frac{1}{1+\exp\frac{E-E_f}{k_BT}} \tag{15a, 15b}$$

$$p_0 = \int_{E_v}^{E_{v,min}} g_p(E) f_p(E) dE \approx 2\left(\frac{2\pi m_p^* k_B T}{h^2}\right)^{\frac{3}{2}} \exp\left(-\frac{(E_f - E_v)}{k_B T}\right) = N_v * \exp\left(-\frac{(E_f - E_v)}{k_B T}\right) \tag{16}$$

Where k_B is the Boltzmann's constant, N_c and N_v are effective density of states for conduction and valence bands respectively, E_f is the fermi energy level. Fermi energy level is the energy in which probability of state function is 0.5. For intrinsic semiconductors, intrinsic fermi level, E_{fi}, can be calculated by equalizing (eq 14 & 16):

$$E_{fi} = \frac{1}{2}(E_v + E_C) + \frac{3}{4} k_B T \ln\left(\frac{m_p^*}{m_e^*}\right) \tag{17}$$

The hole and free electron concentration is equal in intrinsic semiconductors, it is defined as the intrinsic carrier concentration, n_i [11]. Intrinsic carrier concentration at thermal equilibrium is constant for a semiconductor:

$$n_i^2 = n_0 * p_0 = N_c e^{-\frac{(E-E_f)}{k_B T}} * N_v e^{-\frac{(E_f - E_v)}{k_B T}} = N_c N_V e^{-\frac{E_g}{k_B T}} \tag{18}$$

2.6 Semiconductor Doping and Change in Fermi Level

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Doping is the addition of impurities to semiconductor crystals to change their properties in a controlled matter. The addition of extra electrons from donor atoms or holes from acceptor atoms change the carrier concentrations of intrinsic semiconductors. Electron doped and hole doped semiconductors are called n-type and p-type respectively. Since the Fermi level is directly related to the probability of an energy state being occupied, the addition of charge carriers changes its position from the intrinsic fermi level [11].

$$\phi_{fp} = E_{fi} - E_f \approx k_B T * \ln\left(\frac{N_d}{n_i}\right) \qquad \& \qquad \phi_{fn} = E_f - E_{fi} \approx k_B T * \ln\left(\frac{N_a}{n_i}\right) \tag{19a, 19b}$$

Where eq. 19a is for n-type, eq. 19b is for p-type, n_0 and p_0 are the concentrations of electrons and holes. Here the importance of Fermi level should be emphasized. It is, as defined, a statistical value, and is extensively used to analyze semiconductor devices since it is a result of all particle behaviors mentioned so far in this paper. Since intrinsic carrier concentration is not related to Fermi level, eq. 18, regardless of doping, it stays the same, thus the product of hole and electron concentrations is a constant.

2.7 Carrier Drift & Diffusion Current

Drift is the movement of carriers due to the electrostatics force acting on them in the presence of an external field and it is the first movement mechanism that will be examined [12]. The current density due to drift J_{drf} is given in terms of carrier concentrations n & p, and charge velocities due to drift v_{dn} & v_{dp}:

$$J_{drf,n} = -env_{drf,n} \quad \& \quad J_{drf,p} = epv_{drf,p} \tag{20a, 20b}$$

The velocities of the carriers can be given in terms of carrier mobilities μ_n & μ_p:

$$v_{drf,n} = -\mu_n \vec{E} \quad \& \quad v_{drf,p} = \mu_p \vec{E} \tag{21a, 21b}$$

The mobility is a proportionality constant and abstracts scattering mechanisms. The charge carrier's interaction with the vibrating atoms of the lattice, phonon scattering, and the charge carrier's interactions with the doped impurities, ionized impurity scattering, are abstracted. They are derived in terms of lattice properties, temperature, and impurity concentrations [8], however, for the purposes of this paper, since the resulting mobilities can be measured are not important.

The other carrier movement mechanism is due to the concentration gradient of the charges, the diffusion current. It is derived using Fick's law of diffusion and given in terms of charge concentration gradients in 3D ∇n & ∇p:

$$J_{dif,n} = eD_n \nabla n \quad \& \quad J_{dif,p} = -eD_p \nabla p \tag{22a, 22b}$$

Where D_n & D_p electron and hole diffusion coefficients respectively and related to the mobilities by the Einstein relation:

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{k_B T}{e} \tag{23}$$

As a result, the total current density, J, is given as:

$$J = en\mu_n \vec{E} + ep\mu_p \vec{E} + eD_n \nabla n - eD_p \nabla p \tag{24}$$

2.8 Recombination & Generation of Electron-Hole Pairs

In nonequilibrium, i.e. when external voltage is applied, heat is changed or light is emitted, carrier concentrations discussed in chapters 2.5 & 2.6 changes due to the generation and recombination of carriers and eq. 18 does not hold true. In equilibrium the rate of generation of electrons & holes and the rate of recombination of electrons & holes, G_n & G_p, R_n & R_p respectively, are equal:

$$G_{n0} = G_{p0} = R_{n0} = R_{p0} \quad (25)$$

In nonequilibrium, however, there are few mechanisms that change these rates causing imbalance in carrier concentrations. First of which will be discovered is direct band-to-band transition. In direct band-to-band recombination an electron in conduction band simply loses energy, by emitting a photon with energy equal to the bandgap energy and combines with a hole in in valence band. This phenomenon happens more frequently in direct bandgap semiconductors and less frequently for in-direct bandgap materials. Direct bandgap materials have their valence band's maximum energy and conduction band's minimum energy occurring at the same momentum, meaning they share the same "k" value in the E-k plot [13]. The recombination rate for band-to-band recombination with low level-injection assumption (i.e. assuming the concentration of excess charges, ∂n & ∂p, being significantly smaller than the majority carrier concentrations in thermal equilibrium) is given for p-type and n-type materials respectively:

Commented [DA8]: III-IV compounds

$$R_n = R_p = \frac{\delta n(t)}{\tau_{n0}} \quad \& \quad R_n = R_p = \frac{\delta n(t)}{\tau_{p0}} \quad (26)$$

Where τ_0 represents excess minority carrier lifetime and is a measurable quantity.

The other mechanism of transition, indirect transition, is the dominant mechanism for direct semiconductors. Indirect transition occurs due to the crystal defects. Since now, the energy gap was considered to have zero probability of state, however, due to the defects there exists allowed energy states in the bandgap called traps. In indirect transition electron does not move directly between conduction and valence bands rather moves to the trap. This transition changes the excess minority carrier lifetime defined in eq. 26, however, since it is a measurable quantity, the eq. 26 encapsulates this transition mechanism and hold true.

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2.9 Continuity Equation

Using all the mechanics discussed so far, an equation can be derived and later be used as the main tool to analyse and model all semiconductor devices [14]. The charge distribution inside the semiconductor as a function of space and time is given in the continuity equation for electrons and holes respectively:

$$\frac{\partial(\delta p)}{\partial t} = D_p \frac{\partial^2(\delta p)}{\partial x^2} - \mu_p \left(E \frac{\partial(\delta p)}{\partial t} + p \frac{\partial E}{\partial x} \right) + G_p - \frac{p}{\tau_{pt}} \quad (27a)$$

$$\frac{\partial(\delta n)}{\partial t} = D_p \frac{\partial^2(\delta n)}{\partial x^2} + \mu_n \left(E \frac{\partial(\delta n)}{\partial t} + n \frac{\partial E}{\partial x} \right) + G_n - \frac{n}{\tau_{nt}} \quad (27b)$$

2.10 Summary

3 Methods

3.1 Introduction

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This chapter is divided into 2 parts: MOSFET model development and simulation software development. In the first part, a basic MOSFET model will be built using the semiconductor physics discussed in chapter 2. MOSFETs are complicated devices utilizing several interfaces, so, to develop a model PN junction and MOS interfaces will be analysed. Analysis of these interfaces will yield key relationships of device and material parameters. With these relationships, famously known MOSFET model for long channel devices will be derived using gradual channel approximation. In the second part, a standalone simulation tool will be introduced, its implementation and features will be explored.

3.2 MOSFET Model Development

3.2.1 PN Junction

3.2.1.1 PN Junction - Conceptual Introduction

When a p-type and an n-type semiconductor are put in contact with each other, PN junction will form. Assuming equilibrium, before contact, both types of semiconductors will be neutral.

During contact, the equilibrium will be disturbed due to minority carriers' diffusion to opposite side. During the diffusion, p-type semiconductor will gain a net negative charge while the n-type semiconductor will gain a net positive charge. Diffusing minority carriers will recombine with the majority carriers on the other side leaving behind the ionized dopant atoms in the junction. A region of no mobile carriers will be created. In this region there will only be these ions creating a charge difference, thus an electric field will be created [15]. The equilibrium will be reestablished when the force of electric field balances out the force of diffusion.

The resultant electric field will act as a potential barrier, V_{bi}, pushing the majority carriers away from the junction and creating a region of no mobile carriers. This depletion region will not allow any charge movement from one side to another, making the PN junction in equilibrium act like an insulator. The junction and the energy diagrams before and after contact are illustrated in figure x.

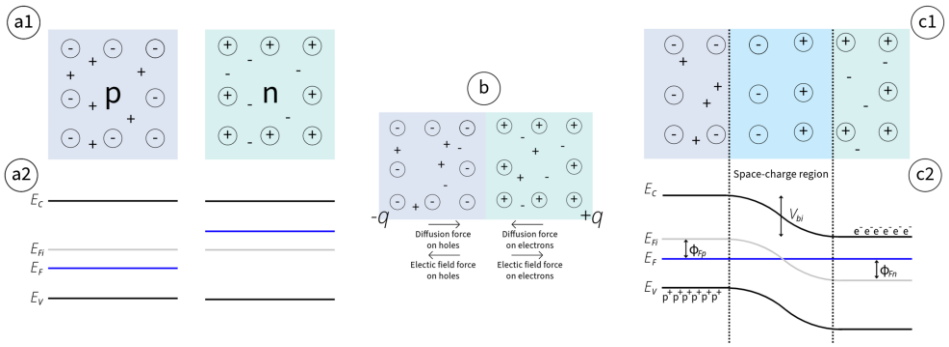

Figure x PN junction before contact (a), transient state (b), and after equilibrium is established (c). Simplified view before contact (a1) and after equilibrium (c1). - and + represents charges; circled charges represent ionized doped charges and non-circled charges represent mobile charges. Band diagram before contact (a2) and after equilibrium (c2); e^- and p^+ represents mobile charge carriers.

Commented [DA11]: Forgot to put e to convert variables into energy

Commented [DA12R11]: E*V_bi e*phi_fp etc

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3.2.1.2 PN Junction – No Bias

Three important PN junction parameters are conceptually explained in the previous section: electric field, built-in potential and space charge region. In this section, they will be mathematically evaluated.

The occurrence of a built-in potential is due to the fermi-level mismatch and since fermi level is a statistical value, in equilibrium it will be constant throughout the whole material. This results in energy bands bending towards the junction. Its value can be derived from (figure x c2) using (19a & 19b):

$$V_{bi} = \frac{\phi_{fp}}{e} + \frac{\phi_{fn}}{e} = \frac{kT}{e} * \ln\left(\frac{N_D}{N_i}\right) + \frac{kT}{e} * \ln\left(\frac{N_D}{N_i}\right) = \frac{kT}{e} * \ln\left(\frac{N_D N_A}{N_i^2}\right) = V_t \ln\left(\frac{N_D N_A}{N_i^2}\right) \quad (28)$$

Where V_t is thermal voltage.

To quantify the electric field, charge densities across the device should be examined. For an easier analysis, so far, the junction is assumed to be linear; for the derivation of electric field, the depletion layer is assumed to be abrupt [16] illustrated in (figure x).

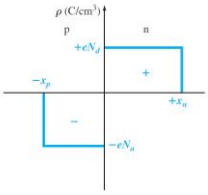

Figure 7.4 | The space charge density in a uniformly doped pn junction assuming the abrupt junction approximation.

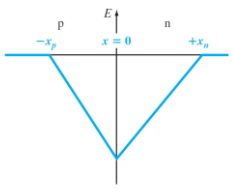

Figure 7.5 | Electric field in the space charge region of a uniformly doped pn junction.

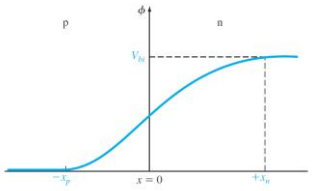

Figure 7.6 | Electric potential through the space charge region of a uniformly doped pn junction.

Figure x

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Using Poisson's equation and Gauss's law gives the electric field in terms of charge density and potential:

$$\nabla^2\phi(x) = -\frac{\rho(x)}{\varepsilon_s} = -\nabla \mathrm{E(x)} \quad (29)$$

Where $\phi(x)$ is the electrical potential at position x, ρ is the net charge density, ε_s is the permittivity of the semiconductor. For one dimensional analysis the electric field in p and n sides respectively:

$$E = \int \frac{\rho(x)}{\varepsilon_s} dx = \int \frac{-eN_A}{\varepsilon_s} dx = \frac{-eN_A}{\varepsilon_s}(x + x_p), \qquad -x_p \le x \le 0 \quad (30a)$$

$$E = \int \frac{\rho(x)}{\varepsilon_s} dx = \int \frac{eN_D}{\varepsilon_s} dx = \frac{-eN_D}{\varepsilon_s}(x_n - x), \qquad 0 \le x \le x_n \quad (30b)$$

The integration constants are in the form that gives results in no electric field outside the depletion layer, i.e. they are zero. The potential for p and n sides respectively:

$$\phi(x) = -\int E(x)dx = \frac{eN_A}{\varepsilon_s}\left(\frac{x^2}{2} + x_p x\right) + C_1, \qquad -x_p \le x \le 0 \quad (31a)$$

$$\phi(x) = -\int E(x)dx = \frac{-eN_D}{\varepsilon_s}\left(x_n x - \frac{x^2}{2}\right) + C_2, \qquad 0 \le x \le x_n \quad (31b)$$

Since the built-in potential is the potential difference between $-x_p$ and x_n, the net potential at $x = -x_p$ is 0, thus, C_1 can be calculated. The net potential at $x = 0$ will then be equal to C_1 and C_2.

$$C_1 = C_2 = \frac{eN_A}{2\varepsilon_s} x_p^2 \quad (32)$$

So, the built-in potential in terms of depletion region width can be written as:

$$V_{bi} = \phi(x_n) = \frac{-e}{2\varepsilon_s}\left(N_D 2x_n^2 + N_A\, x_p^2\right) \quad (33)$$

The electric field is continuous, so at $x = 0$ eq. 30a & 30b can be used to express x_p in terms of x_n:

$$\frac{-eN_A}{\varepsilon_s}(x_p) = \frac{-eN_D}{\varepsilon_s}(x_n), \qquad N_A x_p = N_D x_n, \qquad x_p = \frac{N_D x_n}{N_A} \quad (34)$$

By substituting eq. 34 into eq. 33, depletion regions widths x_p and x_n can be found:

$$x_p = \left[\frac{2\varepsilon_s V_{bi}}{e}\left(\frac{N_D}{N_A}\right)\left(\frac{1}{N_A+N_D}\right)\right]^{1/2} \quad \& \quad x_n = \left[\frac{2\varepsilon_s V_{bi}}{e}\left(\frac{N_A}{N_D}\right)\left(\frac{1}{N_A+N_D}\right)\right]^{1/2} \quad (35a, 35b)$$

Finally, the total depletion width:

$$W = x_p + x_n = \left[\frac{2\varepsilon_s V_{bi}}{e}\left(\frac{N_A+N_D}{N_A N_D}\right)\right]^{1/2} \quad (36)$$

It is important to note this analysis is done for the doping profile given at in (figure x), however, for any doping profile, the same analysis can be done by changing the net charge density function, $\rho(x)$.

3.2.2 MOS Capacitor

3.2.2.1 MOS Capacitor – Conceptual Introduction

Metal-oxide-semiconductor structure is a specific type of metal-insulator-semiconductor structure and is at the core of MOSFET devices. In MOSFETs, the output current is regulated through the voltage applied to this structure. The structure is like a parallel plate capacitor as illustrated in figure x.

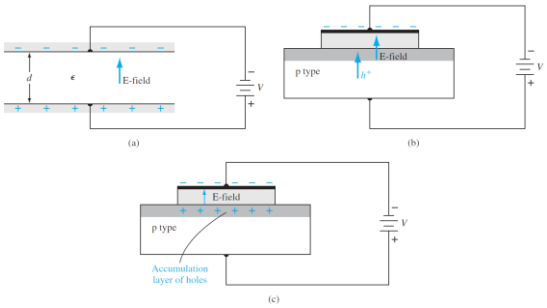

Figure 10.2 | (a) A parallel-plate capacitor showing the electric field and conductor charges. (b) A corresponding MOS capacitor with a negative gate bias showing the electric field and charge flow. (c) The MOS capacitor with an accumulation layer of holes.

Figure x

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The figure illustrates a p-type semiconductor; however, an n-type semiconductor could also be used. To simplify, the semiconductor will be assumed to always be p-type in this section unless explicitly stated and the jargon will be used accordingly. When an external voltage is applied to the metal, depending on the polarity of the voltage, the holes, majority charge carriers, will either be attracted to or pushed away from the oxide interface. These events are called accumulation of holes and depletion respectively. During the depletion, a region of no carriers will be created in the interface like the case of PN junction. This region will be called space charge region or depletion region. When further voltage is applied, holes will be further pushed and electrons will have a high concentration, effectively creating an n-type channel in the oxide-semiconductor

interface, and this is called the inversion of electrons. MOS capacitor will operate in these three regions.

3.2.2.2 MOS Capacitor – Threshold Inversion Point

In this section, an in-depth analysis of MOS structures will be undertaken starting with an isolated semiconductor. The threshold voltage, a crucial MOSFET parameter, will be derived from device and interface parameters.

To quantitatively analyse the depletion region, the energy-band diagram of a p-type semiconductor is illustrated in figure x where bending of bands is present for any reason.

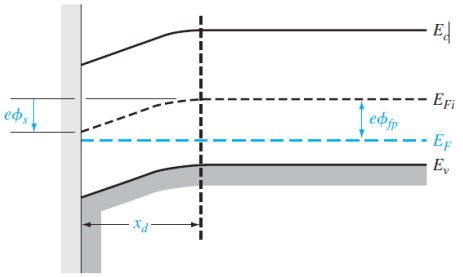

Figure 10.8 | The energy-band diagram in the p-type semiconductor, indicating surface potential.

Figure x

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Surface potential, ϕ_s, is defined to quantify the bending of the bands. The thickness of the depletion region, x_d, could be derived using the depletion width formula derived for PN junctions (eq. 36). The formula simplifies due to $N_a \gg N_d$ in depletion region:

$$x_{d,p} = \left[\frac{2\varepsilon_s\phi_s}{e}\left(\frac{N_a+N_d}{N_aN_d}\right)\right]^{1/2} = \sqrt{\frac{2\varepsilon_s\phi_s}{eN_a}},\ x_{d,n} = \sqrt{\frac{2\varepsilon_s\phi_s}{eN_d}} \qquad \text{(36a, 36b)}$$

If the surface potential is increased further, the bends will bend further, and the depletion region thickness will increase. The threshold inversion point will be reached when the concentration of majority carriers in the bulk semiconductor is equal to the concentration of minority carriers on the surface. The voltage in which this point is reached is defined as the threshold voltage, V_t, and it occurs when $\phi_s = 2\phi_{fp}$ [17]. After the threshold inversion point is reached, further increase in surface potential will only slightly change the space charge region's thickness [18], thus, its maximum is defined:

$$x_{d_{max},p} = \sqrt{\frac{4\varepsilon_s\phi_{fp}}{eN_A}}, \quad x_{d_{max},n} = \sqrt{\frac{4\varepsilon_s\phi_{fp}}{eN_D}} \qquad \text{(37a, 37b)}$$

So far, the metal and oxide are not considered. Now, a complete MOS structure will be analysed, thus the specific material choices for the MOS structure will be important. For this analysis, silicon dioxide (SiO_2) is assumed to be the oxide layer, p-type silicon (P-Si) is assumed to be the semiconductor substrate. With different material choices the interface could be made so in equilibrium it can in inversion. For this case the energy band diagram is illustrated in figure x.

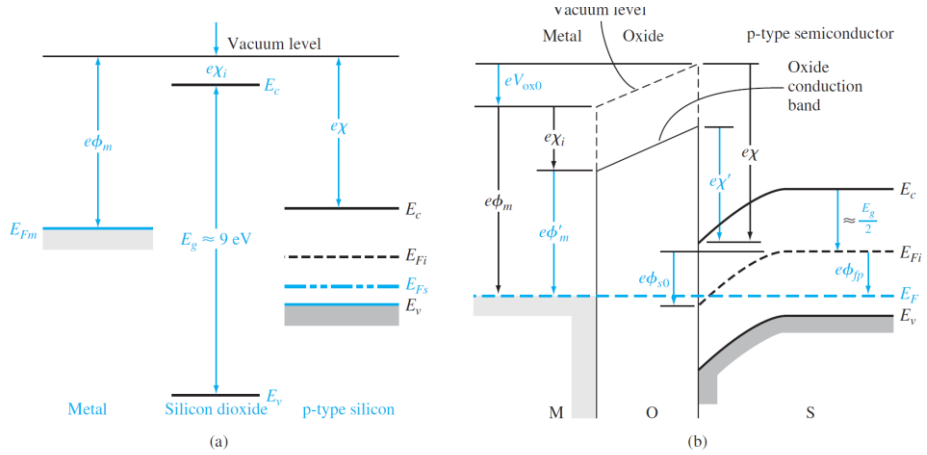

Figure 10.13 | (a) Energy levels in a MOS system prior to contact and (b) energy-band diagram through the MOS structure in thermal equilibrium after contact.

Figure x

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Commented [DA19R18]: B is too complicated make it easier to understand no need to define weird parameters such as x' phi'

The work function, $e\phi$, is defined as the energy needed to remove an electron from the fermi level to the vacuum level. For metals this value is dependent on temperature, however it is fairly constant for a long range of temperatures [19] and can be treated as a material constant, while for semiconductors, the fermi level should be calculated using (eq. 19a 19b).

The electron affinity, $e\chi$, is defined as the energy needed to remove an electron from the bottom of the conduction band to the vacuum level, thus it is a material constant for both metals, insulators and semiconductors [20].

When the materials are in contact and thermal equilibrium is reached, the resulting energy-band diagram is illustrated in (figure x.b). There exist charge traps in the oxide-semiconductor interface, similar to those mentioned in section 2.8, due to oxidation process during device fabrication. These charge traps result in a potential difference across the oxide layer, $V_{ox,0}$. As a result, the bending of the bands depends on this potential as well as the fermi level differences of metal and

semiconductor. The fermi level difference before contact can be quantified by defining metal-semiconductor work function difference, ϕ_{ms}, that will be constant for a given gate-semiconductor material choice:

$$\phi_{ms} = \frac{E_{f,s}}{e} - \frac{E_{f,m}}{e} = \phi_m - \left(\frac{E_g}{2e} + \phi_{fp} + \chi_s\right) \quad (38)$$

After contact, the fermi level on the semiconductor-oxide interface and metal-oxide interface should be equal in equilibrium:

$$E_{f,s} = E_{f,m} = e\chi_s - e\phi_{s,0} + \frac{E_g}{2} + e\phi_{fp} = e\phi_m + eV_{ox,0} \quad (39)$$

Eq. 39 can be simplified and rearranged using eq. 38:

$$\phi_{ms} + \phi_{s,0} + V_{ox,0} = 0 \quad (40)$$

So far, the analysis assumed no potential bias. If there exists an external potential, the gate voltage, V_g, surface potential and the potential across the oxide will change, thus eq. 40 will no longer be equal to zero:

$$V_g = \phi_{ms} + \phi_s + V_{ox} \quad (41)$$

Since the oxide is a dielectric, voltage across it can be derived using Gauss's law [17] and depletion region thickness formula derived in (eq. 36a, 36b). The voltage across the oxide during inversion:

$$V_{ox} = \frac{Q_m}{C_{ox}} = \frac{Q_{s,dep} - Q_{ox}}{C_{ox}} = \frac{eN_a x_{d,p}}{\frac{\varepsilon_{ox}}{t_{ox}}} - \frac{Q_{ox}}{\frac{\varepsilon_{ox}}{t_{ox}}} = \frac{t_{ox}}{\varepsilon_{ox}}\left[\sqrt{eN_a 2\varepsilon_s \phi_s} - Q_{ox}\right] \quad (42)$$

Where Q, is the charge density (Q_m is in metal side of metal-semiconductor interface, $Q_{s,dep}$ is in semiconductor side of oxide-semiconductor interface, Q_{ox} is the trapped charge in the semiconductor side of the oxide semiconductor interface), C_{ox}, is the oxide capacitance per unit area and t_{ox} is the thickness of the oxide. It is important to note that charge in the channel created due to inversion is ignored in this derivation.

Finally, a formula for threshold voltage can be derived assuming the condition $\phi_s = 2\phi_{fp}$:

$$V_{th,p} = \phi_{ms} + 2\phi_{fp} + V_{ox} = \phi_m - \left(\frac{E_g}{2e} + \phi_{fp} + \chi_s\right) + 2\phi_{fp} + \frac{t_{ox}}{\varepsilon_{ox}}\left[\sqrt{\left|eN_a 4\varepsilon_s \phi_{fp}\right|} - Q_{ox}\right] \quad (43)$$

$$V_{th,n} = \phi_{ms} + 2\phi_{fn} + V_{ox} = \phi_m - \left(\frac{E_g}{2e} + \phi_{fn} + \chi_s\right) + 2\phi_{fn} + \frac{t_{ox}}{\varepsilon_{ox}}\left[\sqrt{\left|eN_d 4\varepsilon_s \phi_{fn}\right|} - Q_{ox}\right] \quad (44)$$

The required voltage to create an inversion, i.e. to make the minority carrier concentration in the oxide-semiconductor interface equal to the majority carrier concentration in the bulk semiconductor, can now be calculated from manufacturing parameters.

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3.2.3 MOSFET I-V Characteristics – Long Channel Model

In this section, a basic and well known MOSFET model, long channel model, will be derived [18] [21] [22]. The model will not consider many quantum-mechanical effects which will ultimately result in low accuracy prediction of device behaviour. However, the model is beneficial to understand the MOSFET device.

To create a MOSFET, in addition to the previously analysed MOS capacitor, two heavily doped semiconductors are added to the substrate. These semiconductors are connected to electrodes which are called source and drain and the metal of the MOS capacitor is called the gate. These are the three terminals of a MOSFET. The device is called NMOS if the source and drain are n-type and PMOS if they are p-type. The source and drain are always the same type while the substrate is the opposite type. The device is illustrated in figure x.

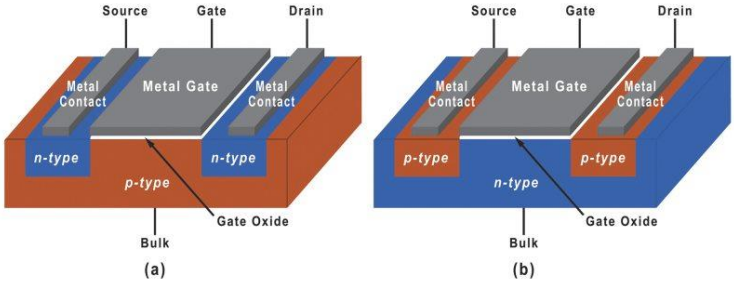

Figure x

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Under zero potential, the structure has two PN junctions that would not allow current flow from source to drain. A potential applied to the gate (defined as V_g in the previous section and is applied from gate to bulk, here will be labelled as V_{gs} for convention and will assume the bulk is connected to the source) will control the conductivity of these PN junctions. In the accumulation region, the conductivity will be decreased, ideally will be zero; in depletion region the conductivity will still be ideally zero; in inversion region the conductivity will be nonzero, and a conductive channel will be formed. In the most ideal MOSFET model, the switch model, this behaviour is modelled such that once the threshold inversion point is reached, a channel with infinite conductivity will be present. Unlike this, in the long channel model, conductivity of the channel is defined using the previously

discussed topics and the effect of the potential across source and drain, V_{ds}, on the channel conductivity is considered. The model assumes following [18]:

1. Only drift current occurs in the channel.
2. There is no leakage current due to MOS capacitor.
3. The potential in x-direction gradually decreases from source to drain and the potential in y-direction quickly decreases from gate to the bulk semiconductor. This assumption is called the gradual channel approximation.
4. All trapped charges in the oxide are at the semiconductor interface.
5. Carrier mobility is constant throughout the channel.
6. Generation, recombination and hole current are negligible.

Assuming an NMOS device, illustrated in figure x, the derivation is as follows:

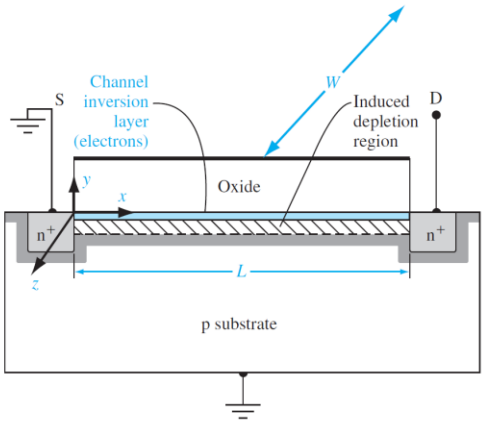

Figure 10.43 | Geometry of a MOSFET for I_D versus V_{DS} derivation.

Figure x

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Due to assumption 1, the current density is equal to the drift current density that is derived in (eq. 20, 21):

$$J_{total} = J_{drf,n} = en(y)\mu_n E_x \qquad (45)$$

Since the electron concentration is not constant it is given in as a function of position y. The total current in x-direction is:

$$I_x = \int_y \int_z en(y)\mu_n E_x \, dydz = \mu_n E_x \int_y \int_z en(y) \, dydz = \mu_n E_x \int_z -Q_{ch} dz = -\mu_n E_x W_{ch} Q_{ch} \qquad (46)$$

Where Q_{ch} is the charge per unit area in the channel and W_{ch} is the width of the channel. To find the charge in the channel, Gauss's law is applied to the surface illustrated in figure x.a.

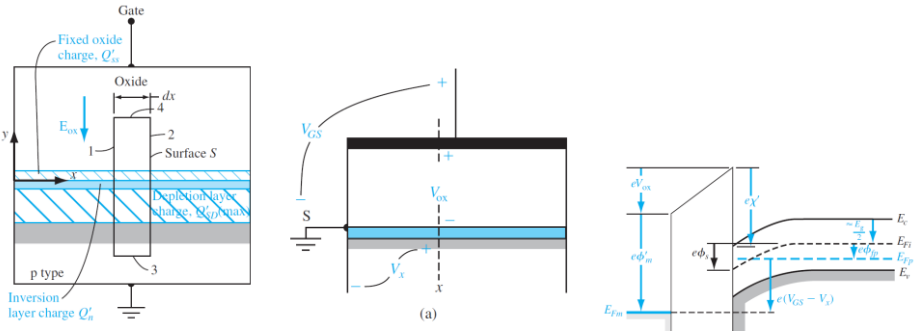

Figure x

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$$\varepsilon \oint_S \boldsymbol{E} = Q_{enc} \quad (47)$$

The electric field vectors to surfaces 1 and 2 cancel each other and no electric field is present at bulk semiconductor, so the integral is only solved for surface 4:

$$\varepsilon_{ox} E_{ox} W dx = \left[Q_{enc} = Q_{ox} + Q_{s,ch} + Q_{s,dep}\right] W dx \quad (48)$$

Electric field across the oxide at x-position x can be written in terms of the oxide potential eq. 43:

$$E_{ox} = \frac{V_{ox}}{t_{ox}} = \frac{(V_{gs} - V_x) - (\phi_{ms} + 2\phi_{fp})}{t_{ox}} \quad (49)$$

The total charge in the channel can be derived using eq. 48, 49 and written in terms of threshold voltage using eq. 42, 43:

$$Q_{s,ch} = \frac{\varepsilon_{ox}}{t_{ox}}\left[(V_{gs} - V_x) - (\phi_{ms} + 2\phi_{fp})\right] - (Q_{s,dep} - Q_{ox}) = C_{ox}(V_{gs} - V_x - V_{th}) \quad (50)$$

The channel charge concentration can be substituted back to eq. 46:

$$I_x = -\mu_n E_x W_{ch} C_{ox} (V_{gs} - V_x - V_{th}) \quad (51)$$

Finally, the electric field can be written in terms of potential and the equation can be integrated through the channel length:

$$\int_0^L I_x \, dx = \int_0^L -\mu_n W_{ch} C_{ox} \frac{dV_x}{dx} (V_{gs} - V_x - V_{th}) \, dx = -\mu_n W_{ch} C_{ox} \int_{V_x(0)}^{V_x(L)} (V_{gs} - V_x - V_{th}) \, dV_x =$$
$$-I_{ds} L = -\mu_n W_{ch} C_{ox} \left[(V_{gs} - V_t) * V_x - \frac{V_x^2}{2}\right] \quad (52)$$

The equation can be rearranged:

$$I_{ds} = \frac{\mu_n W_{ch} C_{ox}}{2L}\left[2(V_{gs} - V_t)V_{ds} - V_{ds}^2\right] \quad (53)$$

This equation is valid only for $V_{gs} > V_t$ and $V_{gs} - V_t > V_{ds}$. The equation shows for a given gate-to-source voltage, increase in drain-to-source voltage will quadratically increase and quadratically decrease. When maximum current occurs at $V_{ds} = V_{gs} - V_t$, the saturation voltage, $V_{ds,sat}$, is defined.

This model assumes after saturation voltage, current stays constant and before threshold voltage there is no current. So, the complete long channel model for NMOS becomes:

$$I_{ds} = 0, \qquad V_{gs} < V_t \quad (54)$$

$$I_{ds} = \frac{\mu_n W_{ch} C_{ox}}{2L}\left[2(V_{gs} - V_t)V_{ds} - V_{ds}^2\right], \qquad V_{gs} > V_t \;\&\; V_{ds} < V_{ds,sat} \quad (55)$$

$$I_{ds} = \frac{\mu_n W_{ch} C_{ox}}{2L}\left[V_{gs} - V_t\right]^2, \qquad V_{gs} > V_t \;\&\; V_{ds} > V_{ds,sat} \quad (56)$$

For PMOS:

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$$I_{ds} = 0, \qquad |V_{gs}| < |V_t| \quad (57)$$

$$I_{ds} = -\frac{\mu_p W_{ch} C_{ox}}{2L}\left[2(V_{gs} - V_t)V_{ds} - V_{ds}^2\right], \qquad |V_{gs}| < |V_t| \;\&\; |V_{ds}| > |V_{ds,sat}| \quad (58)$$

$$I_{ds} = -\frac{\mu_p W_{ch} C_{ox}}{2L}\left[V_{gs} - V_t\right]^2, \qquad |V_{gs}| > |V_t| \;\&\; |V_{ds}| > |V_{ds,sat}| \quad (59)$$

3.2.4 Model for MOSFET Simulation

Since the aim of this project is simulating the device before manufacturing intermediate parameters such as threshold voltage cannot be the input of the simulation. For an n-type device, the parameters used in the simulation are visualized in the flowchart in figure x and the implementation of the flowchart in code is in appendix x.

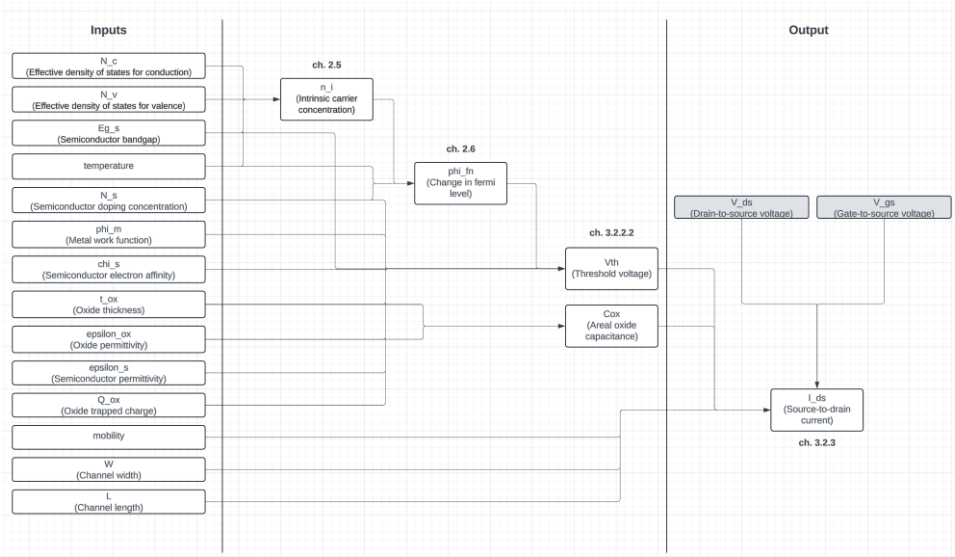

Figure x

3.2.5 Review of Current MOSFET Models

The long channel model is a very simple model. Although its accuracy is poor and gets even poorer as the channel size gets shorter, it is still used quite extensively. Mainly for educational purposes and as a hand-calculation. It is also important to note that this model does not consider any frequency effects and thus purely a DC model.

Currently the MOSFET sizes are down to few nanometres, so the quantum effects become crucial to consider. As more effects are considered, the models get more complicated and computationally expensive. The models are categorized into four categories [23]:

- Table lookup models: Either experimental or analytical model simulation data is stored for various conditions and used for further simulation. No underlying physical insights in the models.
- Empirical models: Real data measurements are modelled by curve-fitting. No underlying physical insights in the models.

- Analytical models: Models developed purely from device physics through rigorous mathematical calculations. They are the most computationally expensive models. Further categorized in two categories
- Semi-empirical analytical models: Combines of analytical and empirical elements. The model is analytically developed, and the accuracy is further improved by curve fitting with empirical values. Extensively used in current industry.

The choice of a model depends on the aim. Since the aim of this project is to simulate a MOSFET before manufacture, no data measurement is possible for the combined MOS structure. Therefore, analytical or semi-empirical analytical models should be developed. In this paper, a simple yet complete development process of an analytical model is undertaken to develop the long channel model. Device outputs can be simulated by choosing the geometry of the device and the material properties of the metal, oxide and semiconductors.

The most advanced simulators such as Silvaco TCAD or Synopsys Sentaurus are purely physical models that numerically solves the fundamental equations derived in section two such as continuity equation, transport equation, Poisson's equation alongside other quantum mechanical equations for the specific 2D or 3D device structure for the most accurate results.

3.3 Simulation Software Development

3.3.1 Purpose of the Software

A standalone simulation program is built as part of this project. The purpose of software is to simulate output and transfer characteristics of a MOSFET with defined models. Although the main purpose is specific for MOSFET devices, other transistor models can be simulated with some limitations.

The software alone is targeted for engineers who wants to simulate their transistor models with ease. However, as part of this project, the developed MOSFET model (3.2.4) can be used by manufacturers before the device is built.

3.3.2 Software Implementation

Main principles of software implementation throughout this project include efficiency, modularity and ease of use.

The simulation can generate thousands of curves, with each curve containing hundreds of x-y data points. While the exact speed at which these tasks are executed will depend on the system's

specifications and load, the software is implemented to execute them quickly and with minimal load due to the choice of C++ language and low level memory control features of such low-level languages.

The ease-of-use principle is attributed to the simple graphical user interface created for the software. For the frontend development, Qt framework has been utilized. Although comprehensive testing has not been conducted, the software will not allow inputs that may result in crashing or produce physically illogical devices. Figure x shows some images from the user interface, showcasing some of its features. For the visualization of data, a public library “pbPlots” is used. Some modifications to the library has been done in order to make graphs more unique and suitable for the application.

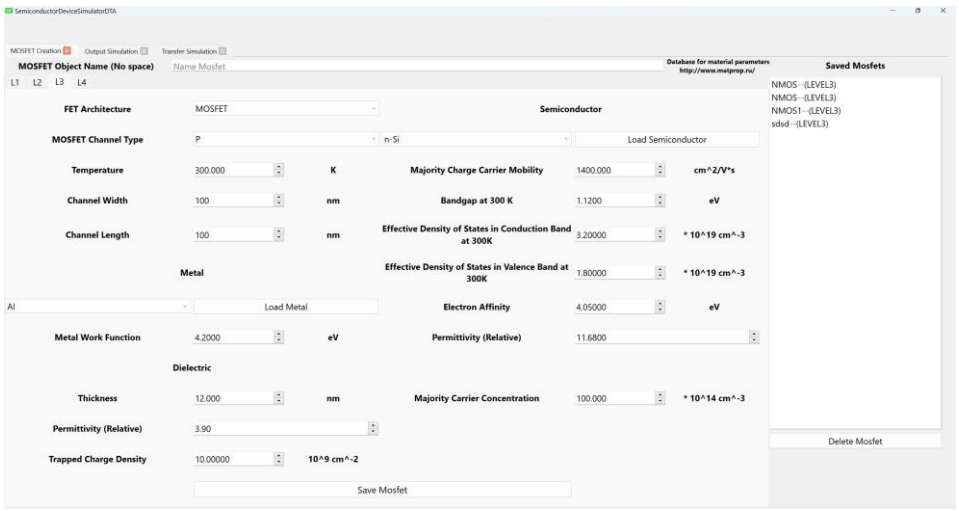

Figure x Starting screen where MOSFETs can be created with user inputs. L3 is the model defined in chapter 3.2.4

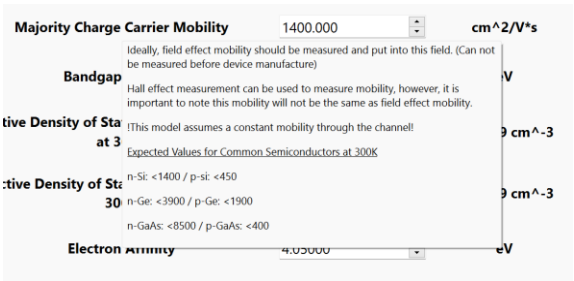

Figure x Tooltip explaining parameter majority charge carrier mobility.

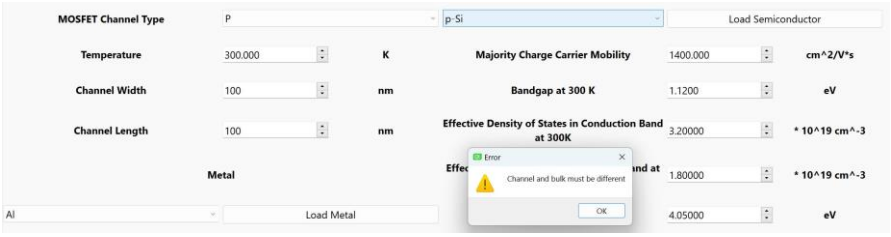

Figure x Error popup that does not allow channel type and bulk type to be the same to not create physically illogical device.

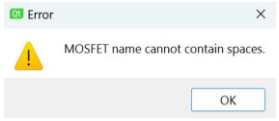

Figure x Error popup that does not allow space in MOSFET name to avoid a program malfunction.

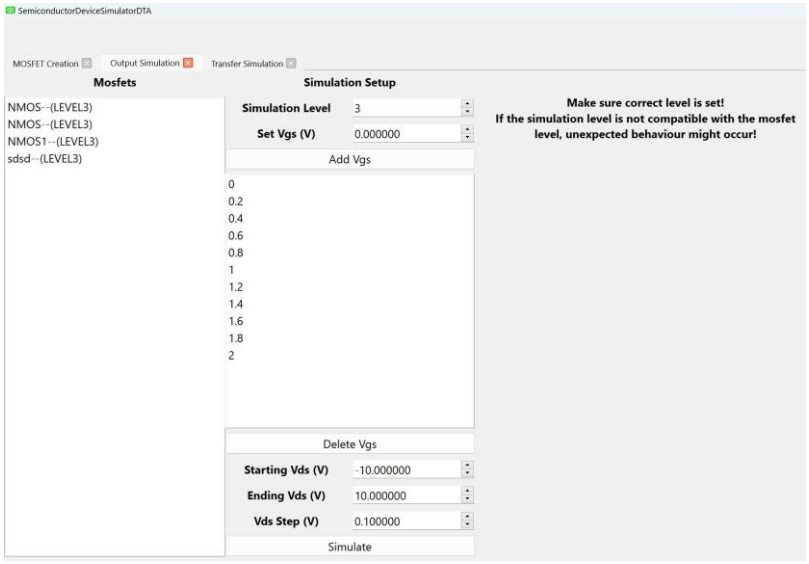

Figure x Output simulation page where the user can choose one of the devices created, simulation level, gate-to-source voltage values and drain-to-source voltage sweep parameters.

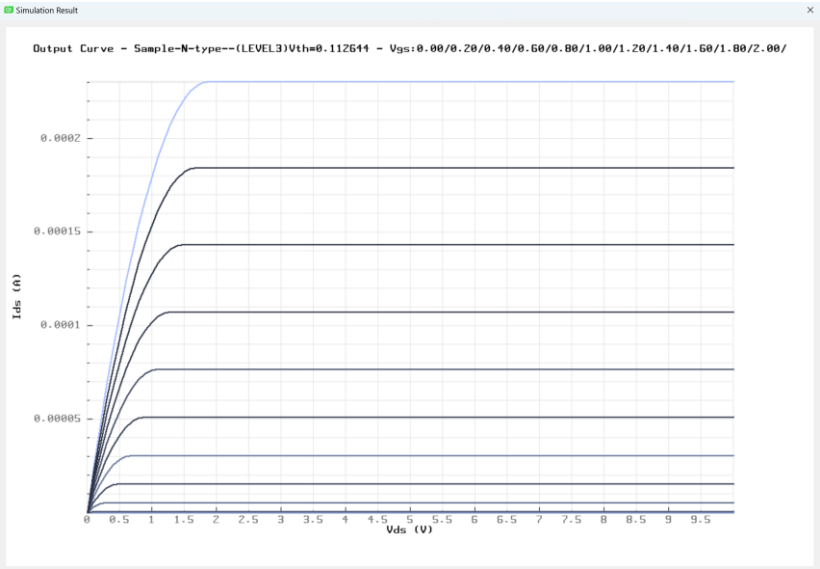

Figure x A sample output curve generated.

The software is also highly modular, with all source files clearly labelled for their purpose. Any single file of the software can be utilized for other purposes with minor adjustments. More importantly, any transistor model can be integrated into the software by following the guidance provided. Figure x shows the current file management for the software.

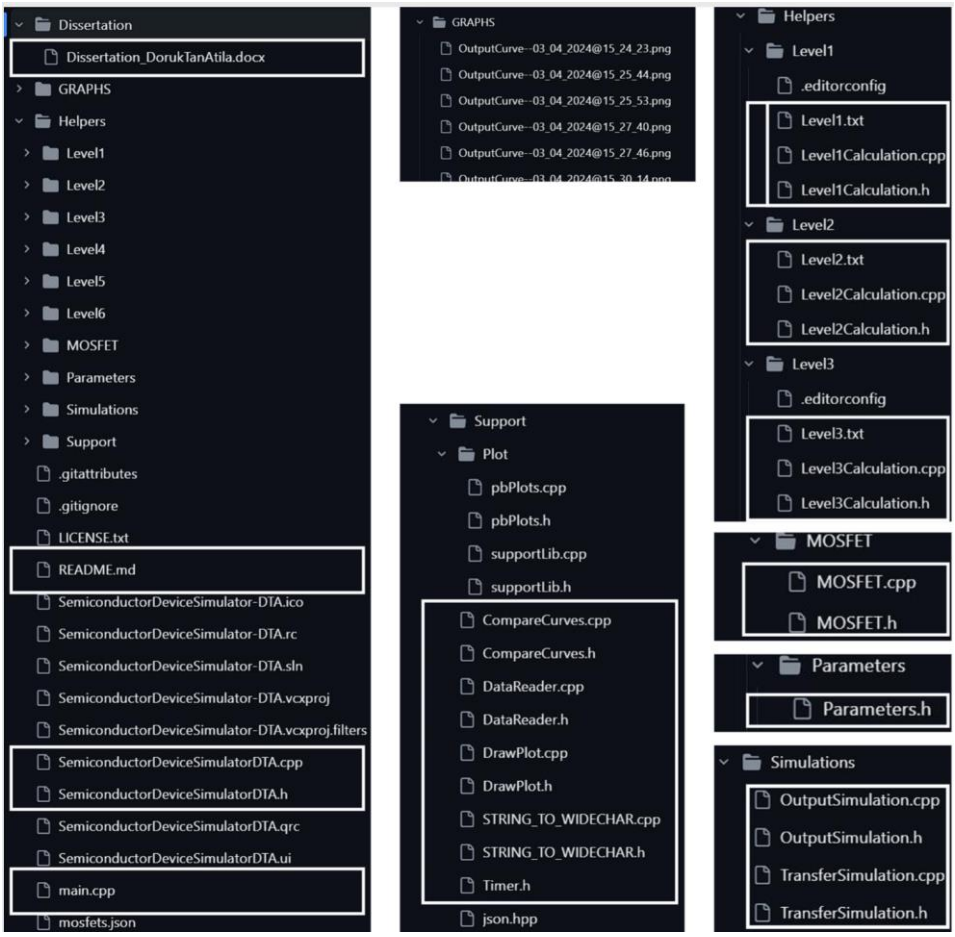

Figure x Source files for the software shown with the folder management. The files in white rectangles are written solely by the author.

The flow of the program can be explained by an example: The user starts by running the program. The "main.cpp" file executes and initializes the Qt files to create the user interface. The user then selects a model and enters the required inputs to create a device based on that chosen model. They name the device and save it.

In the backend, this action creates a MOSFET object defined in the "MOSFET.h" file. The user then navigates to the Output (or Transfer) Simulation page, selects the device name to be simulated, fills in the sweep parameters, and clicks "simulate."

In the backend, this action calls the "OutputSimulation.h" (or "TransferSimulation.h") files to create a simulation object. This object stores all data for that simulation, such as sweep

parameters, input voltages, and output currents (which are initially zero). The object then calls "Level3Calculation.cpp" to calculate the output currents (if the simulation level is chosen as 3).

At this point, the simulation is complete, but visualization has not yet been done. Thus, the simulation object calls "DrawPlot.cpp" to plot the data points. This generates an image, such as Figure x, and the user interface displays this image as a popup.

3.3.3 Key Features & Capabilities - Limitations & Improvements

- Plot as many curves as the system RAM allows.
- If the models are back compatible, a higher-level device can be simulated with lower-level simulation level. Otherwise, this will result in an unexpected behaviour.
- The program currently allows saving devices when the program is shut down so that the same device can be simulated without the need for re-creation. However, while the saving part works, reading the file and recovering the device does not work. The current problems with file I/O are present in the program documentation.
- Output current is calculated for two given input voltages: drain-to-source voltage and gate-to-source voltage. All other parameters except these two are constant and can be in any complexity. Any mathematical model that uses this structure can be simulated with this software regardless of the device type.
- Parallelism can be utilized in models. While parallelism is not used in current model due to its relatively low complexity, models added in future can utilize parallelism without making any changes to the rest of the software.
- Other simulation structures can be added instead of the proposed 2 input voltage model with minimal effort. This creates possibility to extend the software to do other analysis such as AC analysis.

4 Results and discussion

Commented [DA25]: Commerciality of mosfet parameters

4.1 Presentation of Measurement Results

To test the accuracy of the developed model a commercial MOSFET's transfer and output characteristics are measured. The device measured is Toshiba's MOSFET with manufacture number SSM3K15AFS, LF. The measurements are graphed in figures x-x.

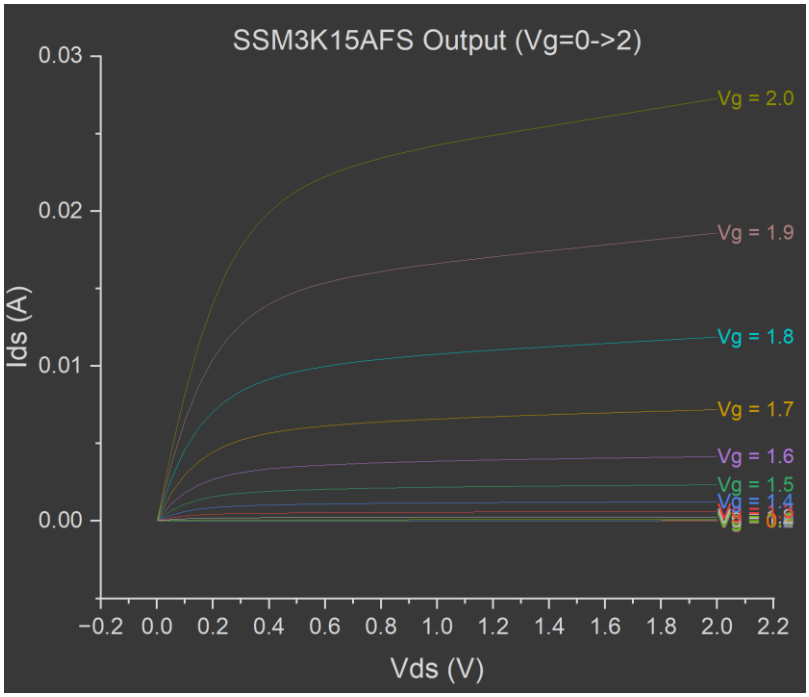

Figure x Output curves of SSM3K15AFS with gate voltages 0 V to 2 V and steps of 0.1 V.

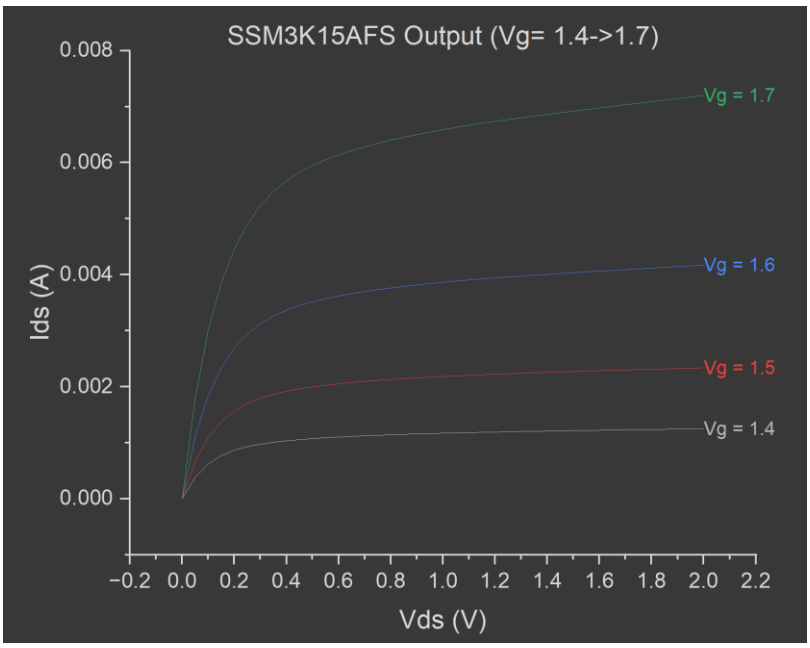

Figure x Output curves of SSM3K15AFS with gate voltages 1.4 V to 1.7 V and steps of 0.1 V.

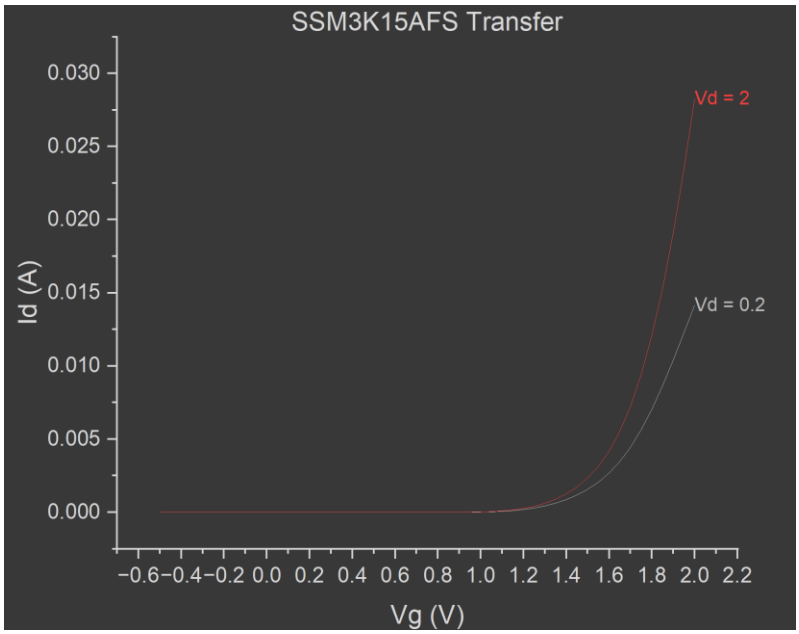

Figure x Transfer curves of SSM3K15AFS for drain-to-source voltages 0.2 V and 2 V.

4.2 Presentation of Simulation Results

Ideally, to test the accuracy of the proposed model, manufacturing parameters should be put into the simulation and the results of the simulation should be compared with the measurement results. However, most of the manufacturing parameters of the devices are not publicly available due to competition in the market. For this purpose, simulation inputs will be reasonably guessed and general trend of the curves will be examined.

According to the manufacturer's datasheet, the threshold voltage is given as 0.8 volts. To confirm this value, constant current method can be used on the transfer curve given at figure x. At 0.8 volts gate-to-source voltage and 2 volts drain-to-source voltage, output current is measured as 9.42E-7 amps. This result confirms that the channel is starting to form at 0.8 volts, however, the saturation points in the output curves suggest a threshold voltage around 1.2 volts. The region between 0.8 and 1.2 volts is the subthreshold region. Since the model defined does not consider subthreshold region, 1.2 volts will be used as the threshold voltage.

According to the manufacturer's datasheet, the technology used is silicon and the device is N-channel.

Given this information, following parameter values can be used as simulation inputs:

Since the channel is N type, the bulk must be P type.

Commented [DA26]: kaynak

- Semiconductor Minority Charge Carrier Mobility: 1400 $\frac{\mathrm{cm}^2}{\mathrm{V}*\mathrm{s}}$
- Semiconductor Bandgap at 300 K: 1.12 eV
- Semiconductor Effective Density of States in Conduction Band at 300 K: 3.2 $* 10^{19}\ \mathrm{cm}^{-3}$
- Semiconductor Effective Density of States in Valence Band at 300 K: 1.8 $* 10^{19}\ \mathrm{cm}^{-3}$
- Semiconductor Electron Affinity: 4.05 eV
- Semiconductor Relative Permittivity: 11.68

Commonly with silicon, silicon dioxide is used as dielectric, and aluminium is used as gate metal.

- Metal Work Function 4.2 eV
- Dielectric Relative Permittivity: 3.90
- Dielectric Thickness: 6 nm
- Dielectric Trapped Charge Density: $10 * 10^{9}\ \mathrm{cm}^{-3}$

Since threshold voltage is 0.8 V, majority charge carrier concentration can be reverse engineered for the parameters stated.

- Majority Charge Carrier Concentration: $6 * 10^{18}\ \mathrm{cm}^{-3}$

Measurements are taken in room temperature.

- Temperature: 300 K

Channel width and channel length solely scales the output current with their ratio thus the following are used:

- Channel Length: 7500 nm
- Channel Width: 100 nm

For the simulation, these inputs will be used, since they confirm with the data sheet values and are possible values for current technologies. The resulting output and transfer curves are shown in figure x and x.

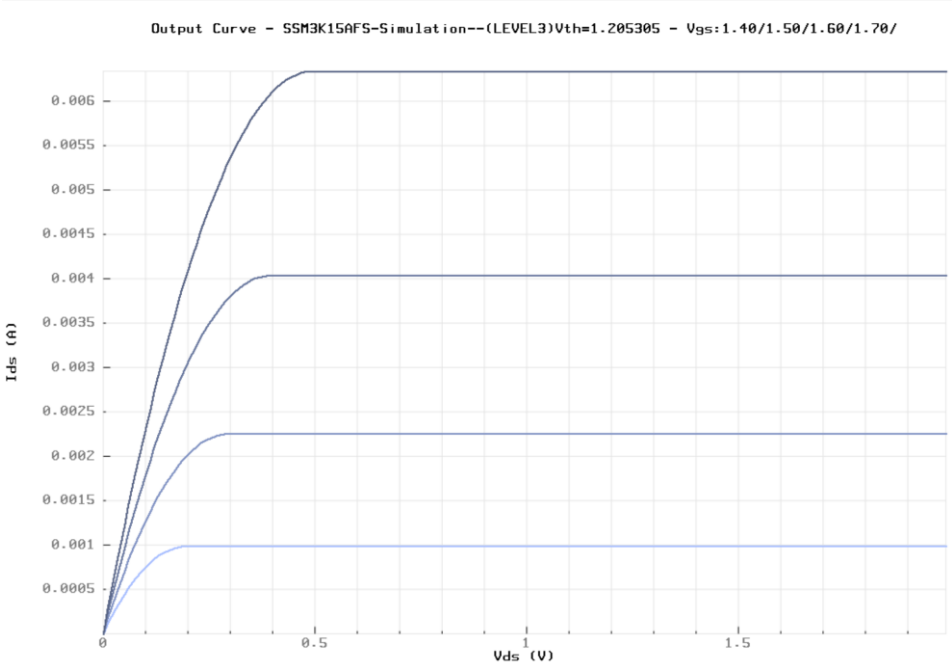

Figure x Output curves of simulation with gate voltages of 1.4 V to 1.7 V and steps of 0.1 V.

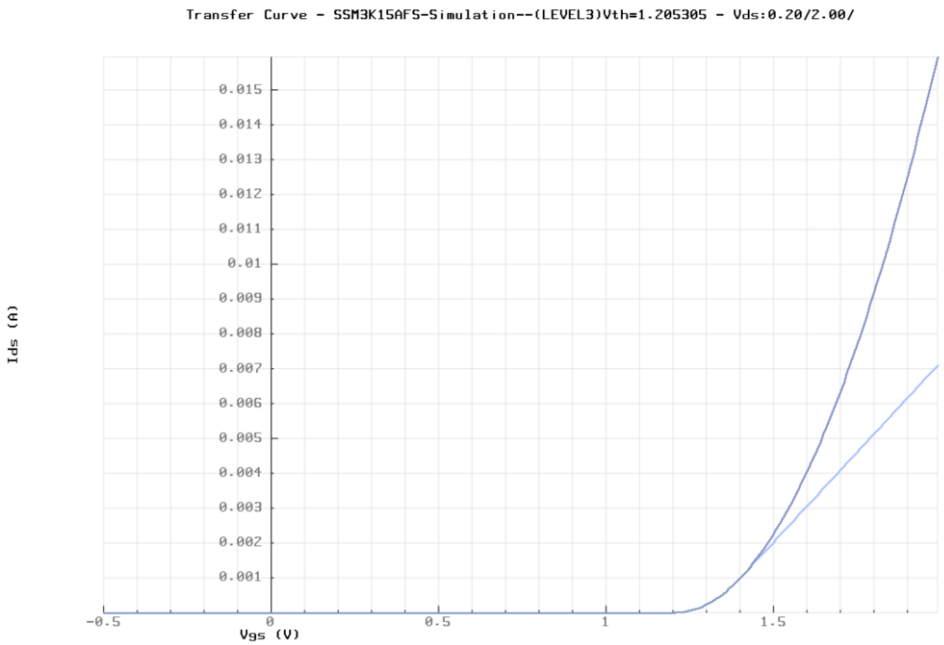

Figure x Transfer curves of simulation for drain-to-source voltages of 0.2 V and 2 V.

4.3 Discussion

4.4 Summary

5 Conclusions and future work

5.1 Conclusions

5.2 Future work

- Light simulation -> optoelectronics
- Modular program so it can be expanded
- Plastic transistor modelling
- Using AI to create empirical models – Since cost of manufacturing is low it is viable to create empirical models.

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Appendices

A Project outline

Project outline as submitted at the start of the project is a required appendix. Put here.

B Risk assessment

Risk assessment is a required appendix. Put here.

C Tables of Symbols – etc.

Notes: Subscript $_0$ represents the variable at equilibrium condition. Subscripts $_{,n}$ & $_{,p}$ are used to represent the variable for n and p type semiconductors respectively.

Table I - Table of Symbols - Chapter 2

Symbol	Meaning	Symbol	Meaning
$\mathbf{E}$	Energy	h	Planck's constant
$\mathbf{f}$	Frequency	λ	Wavelength
$\mathbf{p}$	Momentum	$\Delta\mathrm{p}$	Uncertainty in momentum
$\Delta\mathbf{x}$	Uncertainty in position	$\Delta\mathrm{E}$	Uncertainty in energy
$\Delta\mathbf{t}$	Uncertainty in time	$\hbar$	Reduced Planck's constant
$\boldsymbol{\psi}$	Wavefunction	m	Mass
$\boldsymbol{V}$	Electrical potential	k	Wavevector or wavenumber
$\boldsymbol{E_g}$	Bandgap energy	m^*	Effective mass
$\boldsymbol{n}$	Electron carrier concentration	p	Hole carrier concentration
$\boldsymbol{g(E)}$	Density of states function	$f(E)$	Probability of state function
$\boldsymbol{E_f}$	Fermi level energy	E_c	Conduction band energy
$\boldsymbol{E_v}$	Valence band energy	k_B	Boltzmann's constant
$\boldsymbol{T}$	Temperature	N_c	Effective density states at conduction band

$\boldsymbol{N_v}$	Effective density states at valence band	n_i	Intrinsic carrier concentration
$\boldsymbol{e}$	Elementary charge	E_{fi}	Intrinsic Fermi energy level
$\boldsymbol{\phi_{fp}}$	Fermi potential for p-type semiconductor	ϕ_{fn}	Fermi potential for n-type semiconductor
$\boldsymbol{N_a}$	Acceptor atom concentrations	N_d	Donor atom concentration
$\boldsymbol{J_{drf}}$	Drift current density	v_{drf}	Drift velocity
$\boldsymbol{\mu_n}$	Electron mobility	μ_p	Hole mobility
$\boldsymbol{\vec{E}}$	Electric field	J_{dif}	Diffusion current density
$\boldsymbol{D_n}$	Electron diffusion coefficient	D_p	Hole diffusion coefficient
$\mathbf{G_n}$	Electron generation rate	G_p	Hole generation rate
$\boldsymbol{R_n}$	Electron recombination rate	R_p	Hole recombination rate
$\boldsymbol{\tau_0}$	Excess minority carrier lifetime		

Table 2 - Table of Symbols - Chapter 3

Includes Table 1. Some symbols can be used for different variables and some variables can have different symbols.

Symbol	Meaning	Symbol	Meaning
$\boldsymbol{k}$	Boltzmann's constant		