A Novel Approach to Modelling of MOS Devices – Development of a Simulation Tool for MOSFET Analysis

Third Year Individual Project – Final Report

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Abstract

Metal oxide semiconductor field effect transistors (MOSFETs) have been the building block of high-performance electronics due to their innate speed and power advantages. The trend to shrink down the size of the MOSFETs allows the electronics to be smaller and more powerful and today, few nanometres long MOSFETs can be manufactured. One of the biggest challenges is the cost of initial manufacturing line in sub-micron dimensions.

Thus, the devices can be simulated using models before manufacture. Herein, I review the underlying semiconductor physics…

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Declaration of originality

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# Introduction

## Background and Motivation

The utilization of semiconductor materials has undeniably paved the way for the most significant milestones in the electronics industry. With the invention of first bipolar transistor in 1947, the modern electronics era started. At its core, these tri-terminal devices function as electrical switches, facilitating the execution of mathematical logic operations through the manipulation of voltage and current.

Preceding transistors, their predecessors, such as vacuum tubes also were used for digital computing, however, the use of semiconductor materials has allowed transistors to be much faster, use less power and become progressively smaller, down to nanometric scales today. By 1954, transistors had already replaced forty-eight years old vacuum tubes in many applications [1].

Building upon the success of transistors, further advancements emerged with the invention of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) in 1960. Unlike the bipolar transistors which are controlled by current, MOSFETs are controlled by electric field, thus allowing faster switching speeds. This attribute has propelled MOSFETs to the forefront of contemporary electronic applications. Today, they are predominantly used in all advanced integrated circuits, microprocessors, memory units and more [2].

In 1965, Gordon E. Moore observed that the density of transistors in integrated components was doubling every two years, indicating an exponential decrease in size [3]. This phenomenon owes its validity to the inherent semiconductor nature of these devices. Notably, Moore's Law, encapsulating this doubling trend, persists even 59 years later. As manufacturing complexities and rising fabrication costs pose challenges and signals Moore’s Law’s end, ongoing innovations, such as leveraging analog behaviours of semiconductor devices, sustains improvements in integrated circuit performance [4]. One constant in this evolving landscape is that technological advancement consistently results in an increase in the complexity of device physics.

The initial fabrication cost for transistors of this size is notably high. As a result, the study of transistor modelling becomes crucial. In this project, various MOSFET models will be explored, simulations will be implemented for transistors of diverse sizes, and simulation results will be compared with actual measurements to emphasize the need for enhanced models in transistor simulation.

## Aims and Objectives

The primary objective of this project is building a MOSFET model and developing a tool capable of accurately simulating models for predicting the transfer and output characteristics of a commercial MOSFET. To achieve this overarching aim, the following specific objectives will be pursued:

1. MOSFET Modelling – Theoretical Background

* Propose a MOSFET model by introducing underlying semiconductor device behaviours.

1. Software Development

* Develop a standalone software capable of simulation based on user-provided parameters.
* Enable a plug-and-simulate functionality to incorporate user-defined models seamlessly.

1. Performance Evaluation

* Conduct real-data measurements using an actual MOSFET device.
* Compare the results obtained from the real-data measurements with those generated by the simulation software using proposed MOSFET model.

## Report Structure

This report is organized as follows:

Section 2 provides a comprehensive quantitative analysis of semiconductor mechanisms, leveraging fundamental solid-state physics definitions, parameter definitions, and their interrelations. Additionally, it identifies special semiconductor structures and reviews industry standards relevant to MOSFET simulation software.

Section 3 introduces a MOSFET model derived from the theoretical groundwork outlined in Section 2. It also outlines the development process of a standalone software, which serves as the primary simulation tool for this project.

Section 4 presents and deliberates on the outcomes derived from the MOSFET model simulation and real device measurements.

Finally, Section 5 offers concluding remarks, highlighting key achievements, and delineates potential avenues for future research and development.

# Literature review

## Introduction

This chapter employs a bottom-up approach to delve into MOSFET modelling. MOSFETs are semiconductor devices, so modelling them requires a solid grasp of underlying semiconductor physics. Section 2.2 will delve into fundemental properties of semiconductors, excluding crystallography, starting from quantum mechanics and statistical mechanics to establish carrier concentration equilibrium in semiconductors. Subsequently, the section will quantify the effects of adding impurities to semiconductors and establish the movement mechanics of carriers, leading to the characterization of the electrical behaviour of semiconductors.

In Section 2.3, the electrical properties of semiconductors will be leveraged to describe structures utilizing semiconductors. Following that, Section 2.4 will focus on modelling MOSFET devices, the primary concern of this project. Lastly, Section 2.5 will review the device modelling and simulation software used in the industry.

## Technical Background – Semiconductor Physics

### Quantum Mechanics Principles & Schrödinger Equation

To analyse any semiconductor device, furthermore, any electricity conducting device, electrons are the most fundamental unit that should be examined. While classical laws of physics yield high accuracy for the analyses of large objects, they become inadequate to describe the subatomic particles. For these particles, quantum mechanical principles are the backbones of their analysis. The quantum mechanics in its core has three principles [5]:

Energy is quantized in discrete packets called quanta and its energy is related to the frequency by

where is the energy, is the Planck’s constant and is the frequency.

Particles exhibit wave-like behaviour. The wavelength of a particle is related to its momentum by

where is the de Broglie wavelength of a particle and is the momentum.

The momentum and the position of a particle cannot be described with absolute accuracy; the energy and the time that the particle has that energy cannot be described with absolute accuracy. This relationship is given by

where p, x, E, t are the uncertainties in momentum, position, energy and time respectively. is the reduced Planck’s constant defined as

Although these three principles govern quantum mechanics, to apply them and characterize a system’s quantum-mechanical state, Schrödinger’s time-independent equation given below should be solved.

where is the wavefunction that describes the quantum state of the system, is the total energy of the particle, is the potential experienced by the particle and is the mass of the particle. In this paper, Schrödinger’s equation will not be mathematically solved but rather the solutions will be examined to understand how electrons behave.

### Electron Models

##### Classical Free Electron Model

This model relies on classical laws of physics and electrons are assumed to behave like a classical gas, adhering to the laws of kinetic theory and the electron energies are not quantized; they can take any value without quantum restrictions [6]. The classical free electron theory successfully verifies Ohm’s law, explains thermal and electrical conductivities. However, its reliance on classical mechanics hinders its ability to explain crucial properties in semiconductors and insulators.

##### Quantum Mechanical Electron Model – Potential Well

The Schrödinger’s equation’s solution for the potential well, illustrated in Figure 1, is in the form

A diagram of a region

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Figure 1: Diagram of the infinite potential well [5]

where is the wavenumber and represents the spatial frequency. To describe the energy of the system, can be written in terms of energy using wave-particle duality:

At the boundaries and of the potential well, the wavefunction is evaluated:

Using Equation (8),energy can be evaluated for any non-zero :

The solution suggests that there are allowed energy levels for the electron to occupy. Allowed energy levels are illustrated in Figure 2 for an infinite well with width illustrated in Figure 1.

A diagram of a rectangular object with numbers and equations

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Figure 2: Distribution of allowed quantum levels in the potential well [7]

##### Band Theory of Solids

Understanding the behaviour of electrons in crystalline solids requires a departure from the analysis of isolated particles. When atoms arrange themselves in a crystal lattice, a distinct potential field emerges, differing from the idealized potential well depicted in Figure 1. The fundamental building block of this lattice is known as the primitive cell, which, when replicated in three dimensions, forms the crystal lattice [8]. This periodic structure creates a periodic potential across the volume of the solid. Even without solving the Schrödinger’s equation for this potential, the conclusion of bands and energy gaps could be achieved by applying the quantum mechanical electron model to a crystal lattice. Due to wave particle duality, electrons can be treated as waves, and so the electron waves interacting with the periodic potential creates destructive and constructive interferences.

A linear solid of lattice constant , as illustrated in Figure 3, can be examined to demonstrate the band formation. Bragg condition, which describes the reflections of a wave in a crystal lattice [9], is met at locations . At these locations the traveling electron wave is reflected continuously, thus becoming a standing wave. Between and , first Brillouin zone of the lattice is defined.

A diagram of a waveform

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Figure 3: (a) The change in potential energy experienced by a conduction electron due to the ion cores in a linear lattice, (b) the energy bands due to first Brillouin zone [10] (edited).

For a quantitative description of such crystal, the Schrödinger’s equation is solved for that crystal’s 3D potential and the solution yields to the E-k relationship for that crystal.

### Electrical Conduction in Semiconductor Crystals

Electrical conduction is the existence of a net movement of charge carriers within a material. An intrinsic semiconductor at 0 K has all valence electrons bound to neighbouring nuclei. However, with increasing temperature, thermal energy enables these bonds to break, allowing electrons to transition to higher energy levels, specifically the conduction band. These electrons then can freely move through the crystal lattice. Simultaneously, when the electron jumps to the conduction band, generating a negative charge carrier, it also generates a hole- a positive charge carrier- in the valence band. Therefore, in semiconductors, electrical conduction can occur either through the movement of negative charge carriers in the conduction band or through the collective recombination or generation of carriers. For simplicity in calculations, the latter scenario is often treated as the movement of a single hole. In Figure 4, E-k diagrams of GaAs and Si are illustrated and is defined as the energy gap between the lowest level of conduction band and the highest level of the valence band.

**A graph of energy and energy

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Figure 4: (a) E-k diagram of GaAs, (b) E-k diagram of Si [5]

The energy of a carrier is related to wavenumber- in 3D analysis, wavevector- of that carrier as given in Equation (8). However, the E-k graphs found by solving to the Schrödinger’s equation reveals that the mass of the particle changes as it moves through the lattice. Due to this phenomenon, effective mass, , is defined. The magnitude of effective mass can be approximated using the curvature of the E-k diagram [5]:

### Intrinsic Charge Carrier Concentration

The charge carrier concentration is a crucial parameter in semiconductor characterization. To find the charge carrier concentration, density of states and probability of state functions are integrated, former giving the number of available quantum states and latter giving the probability of a state being occupied. For electrons, density of states function is given in Equation (14), probability of state function is given in Equation (15). For holes, density of states function is given in Equation (17), probability of state function is given in Equation (18).

The electron charge carrier concentration in thermal equilibrium, , can thus be calculated:

Similarly, the hole charge carrier concentration in thermal equilibrium, , can be calculated:

Where is the Boltzmann’s constant, and are defined parameters for effective density of states for conduction and valence bands respectively, is the fermi energy level. Fermi energy level is the energy in which probability of state function is 0.5. For intrinsic semiconductors, intrinsic fermi level, , can be calculated by equalizing Equations (16) and (19):

The hole and electron carrier concentrations are equal in intrinsic semiconductors, and it is defined as the intrinsic carrier concentration, [11]. For a semiconductor crystal, the product of hole and electron carrier concentrations at a given temperature is given by

The implications of this product will be discussed in section 2.2.5.

### Semiconductor Doping and Change in Fermi Level

Doping is the addition of impurities to semiconductor crystals to change their properties in a controlled matter. The addition of extra electrons from donor atoms or holes from acceptor atoms change the carrier concentrations of intrinsic semiconductors. Electron doped and hole doped semiconductors are called n-type and p-type respectively. Since the Fermi level is directly related to the probability of an energy state being occupied, the addition of charge carriers changes its position from the intrinsic fermi level [11]. For high doping concentrations, change in fermi level can be approximated in terms of carrier concentrations in thermal equilibrium:

where Equation (22) is for p-type and Equation (23)is for n-type semiconductor. Here the importance of Fermi level should be emphasized. It is, as defined, a statistical value, and is extensively used to analyze semiconductor devices since it is a result of all particle behaviors mentioned so far in this paper.

The intrinsic carrier concentration defined in Equation (20)suggests that its magnitude depends on crystal constants and temperature but not the fermi level. This means that doping, while it changes the electron and hole concentrations, their product stays the same.

### Carrier Drift & Diffusion Current

Drift is the movement of carriers due to the electrostatics force acting on them in the presence of an external field and it is the first movement mechanism that will be examined [12]. The current density due to drift is given in terms of carrier concentrations and , and charge velocities due to drift and :

The velocities of the carriers can be given in terms of carrier mobilities and :

The carrier mobilities is a proportionality constant and abstracts complex scattering mechanisms. The charge carrier’s interaction with the vibrating atoms of the lattice, phonon scattering, and the charge carrier’s interactions with the doped impurities, ionized impurity scattering, are abstracted. They are derived in terms of lattice properties, temperature, and impurity concentrations [8].

The other carrier movement mechanism is due to the concentration gradient of the charges, the diffusion current. It is derived using Fick’s law of diffusion and given in terms of charge concentration gradients in 3D and :

Where and electron and hole diffusion coefficients respectively and related to the mobilities by the Einstein relation:

As a result, the total current density, , is given as:

### Recombination & Generation of Electron-Hole Pairs

In nonequilibrium, i.e. when external voltage is applied, heat is changed or light is emitted, carrier concentrations discussed in 2.2.4 changes due to the generation and recombination of carriers and Equation (21)does not hold true. In equilibrium, the rate of generation of electrons, holes; the rate of recombination of electrons and holes, , *,*  and respectively, are equal:

In nonequilibrium, however, there are few mechanisms that change these rates causing imbalance in carrier concentrations. First of which will be discovered is direct band-to-band transition. In direct band-to-band recombination an electron in conduction band simply loses energy, by emitting a photon with energy equal to the bandgap energy and combines with a hole in in valence band. This phenomenon happens more frequently in direct bandgap semiconductors and less frequently for in-direct bandgap materials. Direct bandgap materials have their valence band's maximum energy and conduction band's minimum energy occurring at the same momentum, meaning they share the same "k" value in the E-k plot [13]. The recombination rate for band-to-band recombination with low level-injection assumption (i.e. assuming the concentration of excess charges, & , being significantly smaller than the majority carrier concentrations in thermal equilibrium) is given for p-type and n-type materials respectively:

where represents excess minority carrier lifetime and is a measurable quantity.

The other mechanism of transition, indirect transition, is the dominant mechanism for indirect semiconductors. Indirect transition occurs due to the crystal defects. Since now, the energy gap was considered to have zero probability of state, however, due to the defects there exists allowed energy states in the bandgap called traps. In indirect transition electron does not move directly between conduction and valence bands rather moves to the trap. This transition changes the excess minority carrier lifetime defined in Equations (33) and (34), however, since it is a measurable quantity, the equations encapsulate this transition mechanism and hold true.

### Continuity Equation

Using the mechanics of drift current, diffusion current, recombination and regeneration discussed, an equation can be derived and be used as the main tool to analyse and model all semiconductor devices [14]. The continuity equation is a fundamental consequence of physics describing the charge concentration per unit time at a volume. The charge concentration depends on the carrier flux due to the current mechanisms explained in section 2.2.6 and generation and recombination of carriers explained in section 2.2.7. The continuity equation for 1 dimensional analysis for holes and electrons are respectively:

where andare the hole and electron flux respectively.

## Technical Background – Junction Analysis

MOSFETs are complicated devices utilizing several interfaces, so, to develop a model, PN junction and MOS interfaces will be analysed. Analysis of these interfaces will yield key relationships of junction parameters such as depletion region width and threshold voltage. With these relationships, famously known MOSFET model for long channel devices will be derived using gradual channel approximation.

### PN Junction

##### PN Junction - Conceptual Introduction

When a p-type and an n-type semiconductor are put in contact with each other, PN junction will form. Assuming equilibrium, before contact, both types of semiconductors will be neutral.

During contact, the equilibrium will be disturbed due to minority carriers’ diffusion to opposite side. During the diffusion, p-type semiconductor will gain a net negative charge while the n-type semiconductor will gain a net positive charge. Diffusing minority carriers will recombine with the majority carriers on the other side leaving behind the ionized dopant atoms in the junction. A region of no mobile carriers will be created. In this region there will only be these ions creating a charge difference, thus an electric field will be created [15]. The equilibrium will be reestablished when the force of electric field balances out the force of diffusion.

The resultant electric field will act as a potential barrier, , pushing the majority carriers away from the junction and creating a region of no mobile carriers. This depletion region will not allow any charge movement from one side to another, making the PN junction in equilibrium act like an insulator. The junction and the energy diagrams before and after contact are illustrated in Figure 5.

A screenshot of a computer

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Figure 5: PN junction before contact (a), transient state (b), and after equilibrium is established (c). Simplified view before contact (a1) and after equilibrium (c1). - and + represents charges; circled charges represent ionized doped charges and non-circled charges represent mobile charges. Band diagram before contact (a2) and after equilibrium (c2); and represents mobile charge carriers.

##### PN Junction – No Bias

Three important PN junction parameters are conceptually explained in the previous section: electric field, built-in potential and space charge region. In this section, they will be mathematically evaluated.

The occurrence of a built-in potential is due to the fermi-level mismatch and since fermi level is a statistical value, in equilibrium it will be constant throughout the whole material. This results in energy bands bending towards the junction. Its value can be derived from Figure 5 (c2) using Equations (22) and (23):

It is important to note that and , however, the hole concentration is taken at the p side and the electron concentration is taken at the n side. Therefore, to avoid confusion different symbols are used.

To quantify the electric field, charge densities across the device should be examined. For an easier analysis, so far, the junction is assumed to be linear; for the derivation of electric field, the depletion layer is assumed to be abrupt [16] illustrated in Figure 6 (a).

A diagram of a triangle with a circle and a circle with a circle

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Figure 6: (a) Charge density function for abrupt pn junction, (b) electric field and (c) electric potential through the depletion layer created by the pn junction [17] (edited).

Using Poisson’s equation and Gauss’s law gives the electric field in terms of charge density and potential:

where is the electrical potential at position x, is the net charge density, is the permittivity of the semiconductor. For one dimensional analysis the electric field in p and n sides respectively:

The integration constants are in the form that gives results in no electric field outside the depletion layer, i.e. they are zero. The potential for p and n sides respectively:

Since the built-in potential is the potential difference between and , the net potential at is 0, thus, can be calculated. The net potential at will then be equal to and :

So, the built-in potential in terms of depletion region width can be written as:

The electric field is continuous, so at Equations (39) and (40)can be used to express in terms of :

By substituting Equation (47) to Equation (44), depletion regions widths and can be evaluated as

Finally, the total depletion width can be evaluated as

It is important to note this analysis is done for the doping profile given in Figure 6 (a), however, for any doping profile, the same analysis can be done by changing the net charge density function, .

### MOS Capacitor

##### MOS Capacitor – Conceptual Introduction

Metal-oxide-semiconductor structure is a specific type of metal-insulator-semiconductor structure and is at the core of MOSFET devices. In MOSFETs, the output current is regulated through the voltage applied to this structure. The structure is like a parallel plate capacitor as illustrated in Figure 7.

A diagram of a diagram

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Figure 7: (a) Parallel plate capacitor with stored electric field, (b) corresponding MOS structure and (c) MOS structure with accumulated hole layer [18].

The figure illustrates a p-type semiconductor; however, an n-type semiconductor could also be used. To simplify, the semiconductor will be assumed to always be p-type in this section unless explicitly stated and the jargon will be used accordingly. When an external voltage is applied to the metal, depending on the polarity of the voltage, majority charge carriers, holes in this case, will either be attracted to or pushed away from the oxide interface. These events are called accumulation and depletion respectively. During depletion, a region of no carriers will be created in the interface like the case of PN junction. This region will be called space charge region or depletion region. When further voltage is applied, holes will be further pushed and electrons will have a high concentration, effectively creating an n-type channel in the oxide-semiconductor interface, and this is called the inversion of minority carriers, electrons in this case. MOS capacitor will operate in these three regions.

##### MOS Capacitor – Threshold Inversion Point

In this section, an in-depth analysis of MOS structures will be undertaken starting with an isolated semiconductor. The threshold voltage, a crucial MOSFET parameter, will be derived from device and interface parameters.

To quantitatively analyse the depletion region, the energy-band diagram of a p-type semiconductor is illustrated in Figure 8 where bending of bands is present for any reason.

A diagram of a power line

Description automatically generated

Figure 8: Bent energy-band diagram of a p-type semiconductor [18].

Surface potential, , is defined to quantify the bending of the bands. The thickness of the depletion region, , could be derived using the depletion width formula derived for PN junctions in Equation (50). The formula simplifies since in depletion region:

If the surface potential is increased further, the bends will bend further, and the depletion region thickness will increase. The threshold inversion point will be reached when the concentration of majority carriers in the bulk semiconductor is equal to the concentration of minority carriers on the surface. The voltage in which this point is reached is defined as the threshold voltage, , and it occurs when [19]. After the threshold inversion point is reached, further increase in surface potential will only slightly change the space charge region’s thickness [18], thus, its maximum can be evaluated at :

So far, the metal and oxide are not considered. Now, a complete MOS structure will be analysed, thus the specific material choices for the MOS structure will be important. For this analysis, materials used have the band diagrams illustrated in Figure 8. With different material choices the interface could be engineered so the device operates as required.

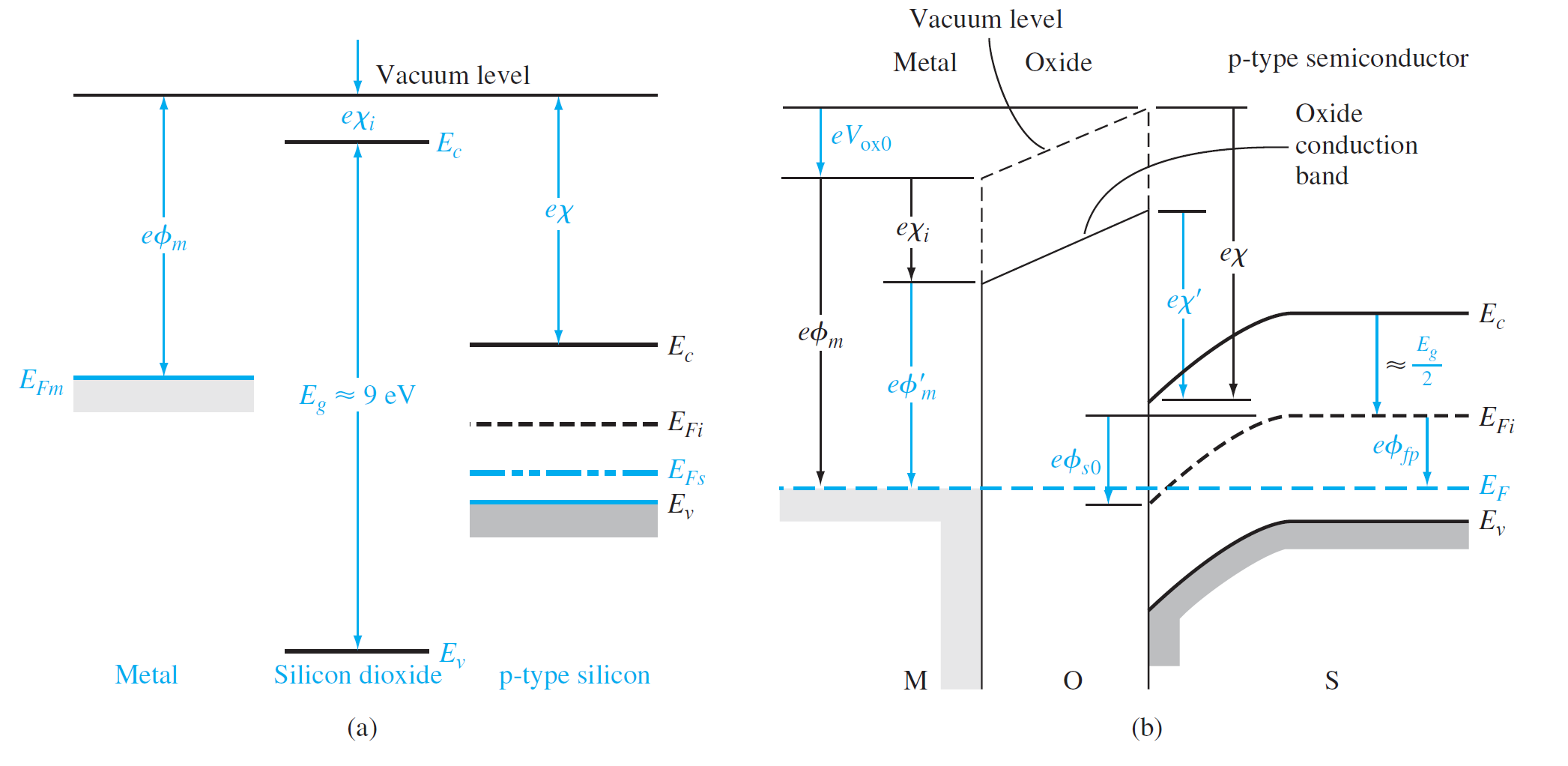


Figure 9: Energy bands of a MOS structure (a) before and (b) after contact [18].

The work function, , is defined as the energy needed to remove an electron from the fermi level to the vacuum level. For metals this value is dependent on temperature, however it is fairly constant for a long range of temperatures [20] and can be treated as a material constant, while for semiconductors, the fermi level should be calculated using Equations (22) and (23).

The electron affinity, , is defined as the energy needed to remove an electron from the bottom of the conduction band to the vacuum level, thus it is a material constant for both metals, insulators and semiconductors [21].

When the materials are in contact and thermal equilibrium is reached, the resulting energy-band diagram is illustrated in Figure 9 (b). There exist charge traps in the oxide-semiconductor interface, similar to those mentioned in section 2.2.7, due to oxidation process during device fabrication. These charge traps result in a potential difference across the oxide layer,. As a result, the bending of the bands depends on this potential as well as the fermi level differences of metal and semiconductor. The fermi level difference before contact can be quantified by defining metal-semiconductor work function difference, , that will be constant for a given gate-semiconductor material choice:

After contact, the fermi level on the semiconductor-oxide interface and metal-oxide interface should be equal in equilibrium:

Equation can be simplified and rearranged using Equation (55):

So far, the analysis assumed no potential bias. If there exists an external potential, which is applied by the gate voltage, , surface potential and the potential across the oxide will change, thus Equation (57) will no longer be equal to zero:

Since the oxide is a dielectric, voltage across it can be derived using Gauss’s law [19] and depletion region thickness formula derived in Equations (51) and (52). The voltage across the oxide during inversion can be evaluated:

Where , is the charge density ( is in metal side of metal-semiconductor interface, is in semiconductor side of oxide-semiconductor interface, is the trapped charge in the semiconductor side of the oxide semiconductor interface), , is the oxide capacitance per unit area and is the thickness of the oxide. It is important to note that charge in the channel created due to inversion is ignored in this derivation.

Finally, a formula for threshold voltage can be derived assuming the condition :

## MOSFET I-V Characteristics – Long Channel Model

In this section, a basic and well known MOSFET model, long channel model, will be derived [18] [22] [23]. The model will not consider many quantum-mechanical effects which will ultimately result in low accuracy prediction of device behaviour. However, the model is beneficial to understand the MOSFET device.

To create a MOSFET, in addition to the previously analysed MOS capacitor, two heavily doped semiconductors are added to the substrate. These semiconductors are connected to electrodes which are called source and drain and the metal of the MOS capacitor is called the gate. These are the three terminals of a MOSFET. The device is called NMOS if the source and drain are n-type and PMOS if they are p-type. The source and drain are always the same type while the substrate is the opposite type. An NMOS device’s cross section is illustrated in Figure 10.

Diagram of a diagram of a body

Description automatically generated

Figure 10: Cross section of an NMOS device [18].

Under zero potential, the structure has two PN junctions that would not allow current flow from source to drain. A potential applied to the gate (defined as in the previous section and is applied from gate to bulk, here will be labelled as for convention and will assume the bulk is connected to the source) will control the conductivity of these PN junctions. In the accumulation region, the conductivity will be decreased, ideally will be zero; in depletion region the conductivity will still be ideally zero; in inversion region the conductivity will be nonzero, and a conductive channel will be formed. In the most ideal MOSFET model, the switch model, this behaviour is modelled such that once the threshold inversion point is reached, a channel with infinite conductivity will be present. Unlike this, in the long channel model, conductivity of the channel is defined using the previously discussed semiconductor dynamics and the effect of the potential across source and drain,, on the channel conductivity is considered. The model assumes following [18]:

1. Only drift current occurs in the channel. i.e. there is no diffusion.
2. There is no leakage current due to MOS capacitor.
3. The potential in x-direction gradually decreases from source to drain and the potential in y-direction quickly decreases from gate to the bulk semiconductor. This assumption is called the gradual channel approximation.
4. All trapped charges in the oxide are at the semiconductor interface.
5. Carrier mobility is constant throughout the channel and does not saturate.
6. Generation, recombination and hole current are negligible.

Assuming an NMOS device, illustrated in Figure 11, the derivation is as follows:

Diagram of a diagram of a rectangular structure

Description automatically generated

Figure 11: Cross section of an NMOS device where inversion layer is present, labelled [18].

Due to assumption 1, the total current density given in Equation (31) has only one term:

Since the electron concentration is not constant, it is given in as a function of position y. The total current in x-direction can be evaluated as

Where is the charge per unit area in the channel and is the width of the channel. To find the charge in the channel, Gauss’s law given below is applied to the surface illustrated in Figure 12:

A diagram of a structure

Description automatically generated

Figure 12: Surface to apply Gauss law [18].

The electric field vectors to surfaces 1 and 2 cancel each other and no electric field is present at bulk semiconductor, so the integral is only solved for surface 4:

Electric field across the oxide at x-position can be written in terms of the oxide potential using Equation (58):

The total charge in the channel can be derived using Equations (65) and (66) and rearranged in terms of threshold voltage defined in Equations (60) and (61) :

The channel charge concentration can be substituted back to Equation (63):

Finally, the electric field can be written in terms of potential and the equation can be integrated through the channel length:

The equation can be rearranged:

This equation is valid only for and . The equation shows for a given gate-to-source voltage, increase in drain-to-source voltage will quadratically increase and quadratically decrease. When maximum current occurs at , the saturation voltage, , is defined.

This model assumes after saturation voltage, current stays constant and before threshold voltage there is no current. So, the complete long channel model for NMOS becomes:

For PMOS:

## Review of MOSFET Models and Simulation Programs

The long channel model is a very simple model. Although its accuracy is poor and gets even poorer as the channel size gets shorter, it is still used quite extensively. Mainly for educational purposes and as a hand-calculation. It is also important to note that this model does not consider any frequency effects and thus purely a DC model.

Currently the MOSFET sizes are down to few nanometres, so the quantum effects become crucial to consider. As more effects are considered, the models get more complicated and computationally expensive. The models are categorized into four categories [24]:

* Table lookup models: Either experimental or analytical model simulation data is stored for various conditions and used for further simulation. No underlying physical insights in the models.
* Empirical models: Real data measurements are modelled by curve-fitting. No underlying physical insights in the models.
* Analytical models: Models developed purely from device physics through rigorous mathematical calculations. They are the most computationally expensive models. Further categorized in two categories
* Semi-empirical analytical models: Combines of analytical and empirical elements. The model is analytically developed, and the accuracy is further improved by curve fitting with empirical values. Extensively used in current industry.

The choice of a model depends on the aim. Since the aim of this project is to simulate a MOSFET before manufacture, no data measurement is possible for the combined MOS structure. Therefore, analytical or semi-empirical analytical models can be developed. So far in this paper, a simple yet complete development process of an analytical model is undertaken to develop the long channel model. Device outputs can be simulated by choosing the geometry of the device and the material properties of the metal, oxide and semiconductors. In the following sections, a model that utilizes the long channel model with pre-fabrication parameters will be proposed and simulated.

The most advanced simulators in industry such as Silvaco TCAD or Synopsys Sentaurus are purely physical models that numerically solves the fundamental equations derived in section two such as continuity equation for the specific 2D or 3D device structure for the most accurate results. While most used simulators such as SPICE employs semi-empirical models. The addition of empirical parameters on the derived long channel model is extensively done in literature and industry. Those parameters approximate secondary effects which the long channel does not consider and thus improves accuracy.

# Methods

## Introduction

This chapter is divided into 2 parts: Proposing a MOSFET model and simulation software development. In the first part, a MOSFET model will be proposed that is implementing the long channel model derived in section 2.4 with manufacturing parameters. In the second part, a standalone simulation tool will be introduced, its implementation, features and limitations will be explored.

## Proposed MOSFET Model

Given the objective of simulating the device prior to the fabrication of the MOS interface, adjustments to the long channel model are necessary, particularly concerning the calculation of the threshold voltage. In this model, the threshold voltage is computed using Equations (60) and (61)**,** where most parameters remain constant for the chosen metal, dielectric, and semiconductor materials, except for the Fermi level shift. The Fermi level shift can be determined through Equations (22) and (23)**,** where the majority carrier concentration serves as an input for the simulation. Notably, the majority carrier concentration can be measured before the fabrication of the MOS interface, and the intrinsic carrier concentration can be calculated using Equation (21), where all parameters remain constant for a given semiconductor material and temperature. The relationship between these parameters and their role in calculating the output characteristics for an n-type MOSFET is depicted in the flowchart presented in Figure 13 below.

A diagram of a voltage

Description automatically generated

Figure 13: Flowchart representing the relations between the parameters. Different line colours and thicknesses are used to increase visibility. Naming convention is the naming convention used in software and explanation of the abbreviations are stated if found necessary.

Given that material selection predominantly dictates input parameters, the model offers the flexibility to refine its specifications further. For instance, opting for p-type silicon as the bulk semiconductor necessitates adhering to pertinent parameters such as effective density of states, bandgap, and electron affinity, tailored to p-type silicon characteristics. This aspect is integrated into the simulation, ensuring alignment with the chosen semiconductor material.

## Simulation Software Development

### Purpose of the Software

The purpose of the software developed as part of this project is to provide a standalone simulation program capable of simulating the output and transfer characteristics of a MOSFET using defined models. While the primary focus is on MOSFET devices, the software also allows for the simulation of other transistor models, albeit with certain limitations.

Primarily aimed at researchers and engineers seeking to simulate their device models conveniently, the software serves as a versatile tool. Additionally, the proposed MOSFET model developed within this project can be utilized by manufacturers in the pre-fabrication stage of device production. The proposed MOSFET model is named L3 or level3 through the software development.

### Software Implementation

The software implementation for this project adheres to several key principles to ensure its effectiveness and usability. These principles include:

1. Efficiency: The software is designed to be efficient in terms of computational resources, memory usage, and processing speed. This ensures that simulations can be performed in a timely manner without excessive resource consumption.
2. Modularity: The software is structured in a modular fashion, with distinct components or modules responsible for specific functionalities. This modular design allows for easier maintenance, scalability, and flexibility, as individual modules can be modified or replaced without affecting the entire system.
3. Ease of Use: User interface design and overall usability are prioritized to ensure that the software is intuitive and easy to use. This includes clear navigation and well-defined input parameters. The goal is to make the software accessible to researchers and engineers without extensive programming experience.

By adhering to these principles, the software implementation aims to provide a reliable, flexible, and user-friendly tool for simulating MOSFET devices and other transistor models.

##### Efficiency of the Software

The efficiency of the software is a critical aspect, particularly when generating numerous curves, each comprising hundreds of x-y data points during simulation. The software is designed to execute these tasks swiftly and with minimal resource usage. This efficiency is achieved through the utilization of C++ language, known for its performance and low-level memory control features inherent in such low-level languages. As a result, the software can handle intensive computational tasks efficiently, ensuring timely generation of simulation results even with large datasets.

##### Ease of Use of the Software

To ensure ease of use, the software features a simple graphical user interface developed using the Qt framework. While comprehensive testing has not yet been performed, the interface is designed to prevent inputs that could potentially cause crashes or lead to the creation of physically illogical devices. Sample images from the user interface, highlighting various features, are provided in Figure 21 through Figure 26 in appendix E. Additionally, for data visualization, the software leverages the "pbPlots" public library, with some modifications made to ensure graphs are tailored to the application's requirements and unique in appearance.

##### Modularity of the Software

The software exhibits a high degree of modularity, with each source file clearly designated for its specific purpose. This modular design allows for flexibility, as any individual file can be repurposed for other applications with minimal adjustments. Furthermore, the software accommodates the integration of user defined transistor models, as outlined in appendices D.

Figure 14 illustrates the organization of source files within the software, showcasing its modular structure.

A screenshot of a computer program

Description automatically generated

Figure 14: Source files for the software shown with the folder management. The files in white rectangles are written solely by the author.

The program's execution can be elucidated through an example: Upon launching the program, the "main.cpp" file initializes the Qt framework to generate the user interface. Subsequently, the user selects a transistor model and provides the necessary inputs to instantiate a device based on the chosen model, assigning it a name and saving it.

Internally, this action creates a MOSFET object defined in the "MOSFET.h" file. The user then proceeds to the Output or Transfer Simulation page, selects the device for simulation, specifies the sweep parameters, and initiates the simulation process.

In the background, this action triggers the "OutputSimulation.h" or "TransferSimulation.h" files to generate a simulation object, which stores all relevant data for the simulation, including sweep parameters, input voltages, and output currents, which are initially set to 0. If the simulation level is set to 3, the object invokes "Level3Calculation.h" to compute the output currents.

Upon completion of the simulation, the simulation object invokes "DrawPlot.cpp" to plot the data points, generating an image such as Figure 26. The user interface then presents this image as a popup for visualization.

### Key Features, Capabilities and Limitations of the Software

* Software performance: The software maximizes system performance by fully utilizing available resources. For example, when generating curves, there is no arbitrary limit on the number of curves users can generate; instead, the limitation is imposed by the system's RAM capacity.
* Simulation Flexibility: If the transistor models are backward compatible, users can simulate higher-level device models with lower-level simulation levels. However, attempting this with incompatible models may lead to unexpected behaviour.
* Device Saving: The software enables users to save device configurations to an external file, allowing for easy retrieval and simulation of the same device without the need for re-creation.
* Output Current Calculation: The software computes output currents based on two specified input voltages: drain-to-source voltage and gate-to-source voltage. All other parameters, except for these two, are defined by the model owner and are established during device creation. This structure enables the simulation of any device model that adheres to these input specifications, irrespective of the device type.
* Flexible Simulation Structures: The software architecture allows for the addition of alternative simulation structures beyond the current two-input voltage model with minimal effort. This flexibility opens up possibilities for extending the software's capabilities to include other types of analyses, such as AC analysis.
* Parallelism Support: Although not utilized in the current model due to its low complexity, the software supports parallelism. This means that future models could leverage parallel processing without requiring major changes to the software itself. Guidance for implementing parallelism is provided in Appendix C.
* Data Visualization: Presently, the software utilizes the "pbPlots" public library for data visualization, and thus limited by it. Despite efforts to customize the visualization, the images generated by the software are deemed unsatisfactory.

# Results and discussion

## Presentation of Measurement Results

To test the accuracy of the developed model a commercial MOSFET’s transfer and output characteristics are measured. The device measured is Toshiba’s MOSFET with manufacture number SSM3K15AFS, LF. The measurement device had current measurement accuracy up to 15th order. The measurements are graphed in Figure 15 and Figure 16 below.

A graph of a line graph

Description automatically generated with medium confidence

Figure 15: Output curves of SSM3K15AFS measurements with various gate voltage values.

A graph of a function

Description automatically generated with medium confidence

Figure 16: Transfer curves of SSM3K15AFS with drain-to-source voltages 0.2 V and 2 V. Left axis logarithmic, right axis linear.

## Analysis of Measurement Results

Analysis of transfer and output curves yields to extraction of crucial parameters. These parameters are then can be used to build table lookup and empirical models explained in section 2.5. While the number of the empirical parameters increase with the complexity of the model, for the model proposed in this project threshold voltage is the only crucial parameter. In this section various methods will be employed to extract an accurate threshold voltage which will be used to simulate the proposed model.

According to the manufacturer’s datasheet, the threshold voltage is specified as 0.8 V.

The linear transfer curve in Figure 16 suggests that the threshold voltage is approximately 1.2 V. However, this method is considered the least reliable due to the inherent limitations of the linear scale.

The constant current method can be applied to the measurement results. At a gate-to-source voltage of 0.8 V and a drain-to-source voltage of 2 V, the output current is measured as 9.42E-7 A. This finding indicates that the channel begins to form at 0.8 V, thereby corroborating the manufacturer’s datasheet. However, it's worth noting that the current threshold for this method is arbitrarily chosen, leading to lower precision in the results.

Utilizing the definition of saturation voltage as defined inequation the output curves in Figure 15 can be analysed. The onset of saturation points indicates that the threshold voltage is approximately 1.1 V. Although this method provides an accurate means of extracting the threshold voltage, the precision is limited to ±0.2 V due to the challenge of selecting the appropriate saturation point.

The logarithmic transfer curve shown in Figure 16 can be analysed for the most accurate and precise assessment. Before the threshold, channel formation leads to a linear increase in drain current. Once the threshold is reached, the MOSFETs operate at saturation, and thus the linear increase ceases. This method suggests that the threshold voltage is approximately 1 V.

Apart from the threshold voltage, a few differences can be observed in the measurement results that the proposed model does not account for. These will be discussed in in section 4.4.

## Presentation of Simulation Results

The proposed model's accuracy ideally requires incorporation of manufacturing parameters into the simulation and subsequent comparison of simulation outcomes with measured results. However, the unavailability of most device manufacturing parameters due to market competition necessitates a reasonable estimation of simulation inputs. These estimations are based on the extracted threshold voltage, manufacturer's datasheet information, and industry standards. Given the limited availability of detailed manufacturing data, the comparison between measurement and simulation will focus on identifying general trends rather than precise alignment.

The simulation will use a threshold voltage of 1 V, extracted from the measurement results.

According to the manufacturer’s datasheet, the technology is silicon, and the device is N-channel. Given this information, semiconductor material values for silicon, where the bulk is p-type, can be used. It is commonly assumed that aluminium is used as the gate material and silicon dioxide as the dielectric. This analysis yields the following parameters:

* P-type bulk silicon minority charge carrier mobility: 1400
* Silicon bandgap at 300 K: 1.12
* Silicon effective density of states in conduction band at 300 K: 3.2
* Silicon effective density of states in valence band at 300 K: 1.8
* Silicon electron affinity: 4.05
* Silicon relative permittivity: 11.68
* Aluminium work function 4.2
* Silicon dioxide relative permittivity: 3.90

Measurements are taken in room temperature:

* Temperature: 300

To achieve a threshold voltage of 1 V within values acceptable by common practice, the following parameters are chosen:

* Silicon dioxide thickness: 2.5
* Silicon dioxide trapped charge density: 10
* P-type bulk silicon majority charge carrier concentration: 5

The channel width and channel length solely scale the output current with their ratio. Thus, the following values are used:

* Channel Length: 3000
* Channel Width: 100

For the simulation, these inputs will be utilized as they align with the data sheet values and are feasible for current technologies. The resulting output and transfer curves are depicted in Figure 17, Figure 18 and Figure 19.

A graph with lines on a grid

Description automatically generated

Figure 17: Output curves of SSM3K15AFS simulation for gate-to-source voltages 0 V, 1.5 V, 1.6 V, 1.7 V, 1.8 V, 1.9 V and 2.0 V. Plots generated by the software developed as part of this project.

A graph with a line drawn on it

Description automatically generated

Figure 18: Transfer curves of SSM3K15AFS simulation for drain-to-source voltages of 0.2 V and 2 V. Plots are automatically generated by the software developed as part of this project.

A graph with a curve

Description automatically generated

Figure 19: Transfer curves of SSM3K15AFS simulation for drain-to-source voltages of 0.2 V and 2 V where log of drain current is taken. Log of 0 is defined as -15 to avoid error. Plots are automatically generated by the software developed as part of this project.

## Discussion of Results

While notable disparities exist between the measurement and simulation results, they mostly exhibit a similar trend. In the following discussion, the results of all three types of graphs will be examined, and the unaccounted factors contributing to these disparities will be discussed.

The most significant discrepancy can be observed in the transfer curve with a logarithmic voltage axis. While the proposed model follows a similar trend after the threshold voltage, it predicts zero current before the threshold voltage. This discrepancy arises from the proposed model's omission of secondary effects such as the existence of subthreshold current due to leakage mechanisms. While such simplifications may be acceptable for certain applications, they become crucial in the context of very low channel size MOSFETs, where accurate modelling is essential to avoid undesired device behaviour.

Transfer curves with linear voltage axis exhibit a similar trend, albeit with discrepancies in magnitudes between the measurement and simulation results. However, when compared to the output curves, both measurements and simulation results consistently correspond to their respective transfer and output curves.

Output curves exhibit a mostly similar trend. However, the independence of saturation current from drain-to-source voltage in the proposed model does not align with the measurement results. Instead, the saturation current increases linearly with drain-to-source voltage. This discrepancy can be attributed to the secondary effect known as channel length modulation, which becomes more pronounced as the channel lengths decrease. Channel length modulation accounts for the influence of drain-to-source voltage on the inversion channel, thereby affecting the output current. In many models, this effect is addressed by introducing an empirical parameter.

Several secondary effects contribute to the discrepancies between the proposed model and the measurement results. These include surface scattering, velocity saturation, and parasitic resistances. In the long channel model derivation, charge carriers were assumed to move only in the x-direction, influenced by the electric field created by the source-to-drain voltage. However, as channel dimensions decrease, the vertical electric field generated by the gate-to-source voltage causes charge carriers to scatter at the oxide surface, reducing their mobility.

Additionally, the model does not account for velocity saturation, assuming mobility remains proportional to the electric field for all values. However, it's observed that under high electric field conditions, charge carrier mobility decreases. This oversight significantly impacts the output currents of the model, particularly in the saturation region.

Furthermore, parasitic resistances due to contacts are neglected in the model. These resistances, being in series, scale the output currents. While these effects are not explicitly considered in the model, the simulation parameters are arbitrarily chosen to replicate the measurement results, inadvertently capturing some of these effects as byproducts.

The significant disparities observed between the measurement and simulation results suggest that the MOSFET manufactured by Toshiba, with part number SSM3K15AFS, LF, likely features shortened dimensions indicative of modern fabrication technology.

# Conclusions and Future Work

## Conclusions

This project embarked on a comprehensive exploration of MOSFET modelling and simulation, aiming to bridge the gap between theoretical understanding and practical application. Through meticulous examination of semiconductor mechanisms and the development of a bespoke simulation software, significant insights into device behaviour were attained and a working simulation software has been publicized.

The in-depth theoretical background provided in semiconductor physics facilitated the characterization of MOSFETs. This characterization was adapted to align with the project's objective of constructing a MOSFET model capable of characterizing device behavior before costly device fabrication.

Another objective of this project was to develop a simulation tool capable of simulating such models. This objective has been surpassed by creating software that serves as a framework for simulating any model, with the capacity to allow users to easily incorporate their own models.

The final objective of this project was to evaluate the performance of the proposed MOSFET model and the simulation software. This objective was achieved by comparing simulation results with measurement results obtained from a commercial MOSFET.

## Future work

While future improvements to the simulation software would involve enhancing user-friendliness by refining the frontend design and addressing the discussed limitations, the outcomes of this project hold significant potential for various applications:

* Modelling and simulation of optoelectronics devices’ power characteristics,
* Modelling and simulation of organic transistors, which is a trending research topic mainly due to low fabrication cost,
* Modelling and simulation of more complex device architectures, which is a trending research topic due to their possible applications in areas such as artificial synapses [25], flexible electronics and bioelectronics.

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# Appendices

A Project outline

Background

Undoubtedly, one of the most significant developments in history is the invention of transistors. The word 'electronics' gained commercial significance after the discovery of these three-terminal devices in 1943. In the most basic sense, a transistor is an electrical switch controlled by an electric input, enabling the implementation of all mathematical logic operations.

What sets transistors apart from other types of switches, such as vacuum tubes, is the utilization of semiconductors. This advancement has allowed transistors to become progressively smaller, down to nanometric scales today. Consequently, they have emerged as the superior choice compared to other types of switches, offering significant improvements in terms of both speed and power consumption. While transistors have analogue applications, this project primarily focuses on their digital characteristics.

As transistor sizes continued to shrink, alternative transistor structures were discovered. The Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) serves as the central transistor architecture for this project. MOSFETs find widespread use in high-performance applications, including CPUs, GPUs, and fast memory units (RAM). This is primarily attributed to their high switching speeds, the ability to control output with input voltage (i.e., no current passing through the gate), and ease of reproducible manufacture.

Motivation

Today, we are approaching the culmination of Moore's Law, which predicted that transistor size would halve every 2 years. This slowdown is primarily a consequence of quantum effects coming into play and semiconductor physics no longer behaving as expected. However, through strategic adjustments to MOSFET structures, careful material selections, and ultra-controlled manufacturing processes, advancements continue to be made.

As previously mentioned, MOSFETs offer the advantage of easily reproducible manufacture. However, establishing the initial manufacturing line incurs costs amounting to billions of dollars. To avoid the wastage of such vast resources, highly intricate MOSFET simulations are employed. These simulations empower engineers to anticipate the device's output behavior before committing billions of dollars to the endeavour.

Aim

The primary aim of this project is to create an accurate simulation of a commercial MOSFET device manufactured with a ~100-micrometer process using various materials. The simulation will predict the device's transfer and output characteristics after parameterization.

Objectives

To achieve this aim, the following objectives will be pursued:

1. Implement Simple MOSFET Models: Develop and employ simple MOSFET models, particularly the gradual channel approximation model combined with the channel length modulation property, to achieve accurate simulations.
2. Accuracy Testing: Evaluate the accuracy of the simulation by comparing its results with those of a commercial MOSFET device manufactured with ~100-micrometer technology.
3. Exploration of Complex Models: If the simple models do not achieve the desired accuracy for ~100-micrometer MOSFETs, or if time allows, explore and implement more advanced transistor models to enhance accuracy.
4. Analogue Properties of the MOSFET: If time allows, model the analogue characteristics of the MOSFET.

GANNT Chart

A screenshot of a project

Description automatically generated

B Risk assessment

General Risk Assessment Form

| Date: (1)  10.10.2023 | Assessed by: (2) | Checked / Validated\* by: L.A. Majewski | Location: (4)  University of Manchester | Assessment ref no (5) | Review date: (6) |
| --- | --- | --- | --- | --- | --- |
| Task / premises: (7)  Working at home on the dissertation projects for Postgraduate Taught students. | | | | | |

*Result: T = trivial, A = adequately controlled, N = not adequately controlled, action required, U = unknown risk*

| Activity (8) | Hazard (9) | Who might be harmed and how (10) | Existing measures to control risk (11) | Risk rating (12) | Result (13) |
| --- | --- | --- | --- | --- | --- |
| Working at home | Coronavirus | Student home working  Infected self-isolation | 1. For the latest information on coronavirus please visit the UoM Coronavirus Website.   2.All staff keep in touch and inform EEE of your expected return to work date (working from home) | Low | A |
| Working at home | Lone working | Student home working  Isolated | 1. Please refer to the University Lone Working policy and guidance for  more information  2. Please refer to the new University Working at Home guidance  3. Please refer to the new University Wellbeing Support website  4. Staff to remain in regular direct contact with line manager and colleagues via phone, Skype, Zoom, Slack or email | Low | A |
| Working at home | Stress/  Wellbeing | Student home working  Psychosocial effects;  Work/Life imbalance;  Anxiety | 1. Please refer to Stress Prevention and Management toolkit for policies and guidance  2. Please refer to new University guidance for Managing teams working from home  3. Please refer to Seven rules of home working published by AMBS  4. Regular contact meetings with manager and peers, Skype, Zoom, Phone  5. Define working hours, set a start & close daily routine, get dressed and prioritize your tasks  6. Manager / Employee consultation, wellbeing focused | Low | A |
| Working at home | Poor posture, repetitive movements, long periods looking at DSE (display screen equipment) | Student home working  Back strain (due to poor posture);  Repetitive Strain  Injury (RSI) to upper limbs;  Eye strain. | 1. Please refer to the DSE policy, guidance and poster for more  information on how to set up your workstation properly  2. Complete DSE self-assessment for guidance on how to set up workstation properly  3. Set up workstation to a comfortable position with good lighting and natural light where possible  4. Take regular breaks away from the screen, at least some activity at your workstation every 20mins and a 5-minute break from workstation every hour.  5. Regularly stretch your arms, back, neck, wrists and hands to avoid repetitive strain injuries. Refer to workstation exercises here  6. Set up a desktop working space where possible and try to avoid working on a laptop without a docking station | Low | A |
| Working at home | Electrical appliance faulted | Student home working  Electric shock,  burns and fire | 1. All office equipment used in accordance with the manufacturer’s instructions  2. Visual checks before use to make sure equipment, cables and free from defects  3. Avoid daisy chaining and do not overload extension leads  4. University IT equipment brought home should already be PAT tested  5. The domestic electrical supply and equipment owned by the employee is the responsibility of the employee to maintain  6. Liquid spills cleaned up immediately  7. Defective plugs, cables and equipment should be taken out of use | Low | A |
| Working at home | Incidents | Student home working  Injuries from home working or other activities | 1. Floors and walkways kept clear of items, e.g. boxes, packaging,  equipment etc.  2. Furniture is arranged such that movement of people and equipment  are not restricted  3. Make sure all areas have good level of lighting  4. Reasonable standards of housekeeping maintained  5. Trailing cables positioned neatly away from walkways  6. Cabinet drawers and doors kept closed when not in use  7.Report the event to personal line manager and the School Safety Advisor to complete an incident form | Low | A |

Probe Station Risk Assessment Form

**LOCATION: 4A.018 LABORATORY (PROBE**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WORK ACTIVITY/**  **WORKPLACE**  **(WHAT PART OF THE ACTIVITY POSES RISK OF INJURY OR ILLNESS)** | **HAZARD (S)**  **(SOMETHING THAT COULD CAUSE HARM, ILLNESS OR INJURY)** | **LIKELY CONSEQUENCES**  **(WHAT WOULD BE THE RESULT OF THE HAZARD)** | **WHO OR WHAT IS AT RISK**  **(INCLUDE NUMBERS AND GROUPS)** | **EXISTING CONTROL MEASURES**  **IN USE**  **(WHAT PROTECTS PEOPLE FROM THESE HAZARDS)** | **WITH EXISTING CONTROLS** | | | | |
| **SEVERITY** | LIKELIHOOD | **RISK RATING** | **RISK ACCEPTABLE** |
| **ELECTRICAL**  **CLEAN ROOM EQUIPMENT**  **CHARACTERIZATION OF SAMPLES USING EQUIPMENT HOUSING HIGH VOLTAGE (E.G. SOURCE-MEASURE UNITS, SEMICONDUCTOR PARAMETER ANALYZERS, ETC.)** | **HIGH VOLTAGE**  **(V < 100V)**  **FIRE** | **ELECTRIC SHOCK**  **BURNS TO SKIN**  **BURNS, DEATH**  **SMOKE INHALATION** | **USER**  **USER**  **ALL IN BUILDING**  **FIRE SERVICES** | **USE OF EQUIPMENT**  **LIMITED TO TRAINED PERSONS**  **SPECIFIC RISK ASSESSMENTS**  **EQUIPMENT IS SUBJECT**  **TO A RECORDED MAINTENANCE PROGRAMME**  **WARNING NOTICE DISPLAYED**  **VOLTAGE LIMITING INTERLOCK**  **USE OF EQUIPMENT**  **LIMITED TO TRAINED PERSONS**  **SPECIFIC RISK ASSESSMENTS**  **WARNING NOTICE DISPLAYED**  **FIRE EXTINGUISHERS** | **4**  **3** | **1**  **1** | **4**  **3** | **Y**  **Y** |
| **LONE/OUT OF HOURS WORKING**  **WORKING IN**  **ISOLATION DURING**  **EVENINGS, WEEKENDS AND HOLDIAYS** | **ALL HAZARDS ASSOCIATED WITH USER ACTIVITIES IN THE CLEAN ROOM** | **ILL HEALTH**  **DELAY IN SUMMONING HELP IN THE EVENT OF EMERGENCY** | **USER** | **NO ONE IS TO WORK ALONE**  **IN THE CLEAN ROOM OUTSIDE**  **THE WORKING HOURS WITHOUT ACADEMIC PERMISSON**  **THE DEPARTAMENTAL POLICY FOR LONE/OUT OF HOURS WORKING IS FOLLOWED**  **ELECTRONIC LOCK SYSTEM GIVING AND LOGGING ACCESS TO THE CLEAN ROOM** | **1** | **1** | **1** | **Y** |
| **DISPLAY SCREEN EQUIPMENT (DSE)**  **MISCELLANEOUS ACTIVITIES E.G. USING COMPUTER, MICROSCOPE, WRITING, ETC.** | **LACK OF AWARENESS**  **E.G. IF USING HEADPHONES** | **NOT HEARING**  **FIRE ALARM** | **PERSON**  **ENGAGED**  **IN ACTIVITY** | **WARNING NOTICE DISPLAYED**  **INDIVIDUAL**  **EQUIPMENT RISK ASSESSMENTS** | **1** | **1** | **1** | **Y** |

**C Initial project plan**

A diagram of a process

Description automatically generated

Figure 20: Illustration of the project plan, categorized into three key sections: (top) theoretical research plan, (middle) Software Development Plan and (bottom) graphical user interface development plan.

**D Software Repository**

MOSFET Simulation Software

Introduction

This is a simulator software repository for semiconductor devices and is implemented in C++. The simulator is designed to be easy to use and to be easily extendable. It is intended for use in teaching environments but can also be utilized for research purposes.

Referencing

This work is described in the dissertation written by Doruk Tan Atila, titled "A Novel Approach to Modelling of MOS Devices – Development of a Simulation Tool for MOSFET Analysis". The dissertation is available in the repository.

How to Add a New Model

To add a new model, follow the steps below:

1. If your model requires a MOSFET object that is not already available (i.e., it requires different inputs), you need to implement it first:
   * Go to MOSFET.h and MOSFET.cpp and create a MOSFET constructor such as:
   * // LVL2 Constructor
   * MOSFET(std::string name, char type, double vt, double mobility, double cox, double w, double l, double lambda);
   * Under the Models folder, create a new folder with the name of the model. Create necessary .h and .cpp files.
   * Include "../MOSFET/MOSFET.h" at the beginning of the model.
   * Define the model's functions, such as:
   * void XXX\_sweep\_output(MOSFET &mosfet, std::unordered\_map<double, std::vector<double>>& Vgs\_Ids\_vector, std::vector<double> Vds\_vector);
   * void XXX\_sweep\_transfer(MOSFET &mosfet, std::unordered\_map<double, std::vector<double>>& Vgs\_Ids\_vector, std::vector<double> Vds\_vector);

(Replace XXX with your model name)

* + Implement any other intermediate functions as needed.

1. Go to OutputSimulation.h and TransferSimulation.h and include the newly created model source file.
2. Go to OutputSimulation.cpp and TransferSimulation.cpp and alter the switch case statements to include your model:
3. switch (COMPLEXITY) {
4. case 1:
5. level1\_sweep\_output(mosfet\_, Params\_Vgs\_Ids\_, Params\_Vds\_);
6. break;
7. case 2:
8. level2\_sweep\_output(mosfet\_, Params\_Vgs\_Ids\_, Params\_Vds\_);
9. break;
10. case 3:
11. level3\_sweep\_output(mosfet\_, Params\_Vgs\_Ids\_, Params\_Vds\_);
12. break;
13. default:
14. throw std::invalid\_argument("Invalid Complexity Level");
15. }

(Replace XXX with your model’s name and do the same for transfer)

Your model is now added to the source code and can be simulated.

**- Doruk Tan Atila**

E Sample Software Images

A screenshot of a computer

Description automatically generated

Figure 21: Starting screen where MOSFETs can be created with user inputs. L3 is the proposed model.

A screenshot of a computer

Description automatically generated

Figure 22: Tooltip explaining parameter majority charge carrier mobility.

A screenshot of a computer

Description automatically generated

Figure 23: Error popup that does not allow channel type and bulk type to be the same to not create physically illogical device.

A screenshot of a computer

Description automatically generated

Figure 24: Error popup that does not allow space in MOSFET name to avoid a program malfunction.

A screenshot of a computer

Description automatically generated

Figure 25: Transfer simulation page where the user can choose one of the devices created, simulation level, gate-to-source voltage values and drain-to-source voltage sweep parameters.

A graph with lines and numbers

Description automatically generated

Figure 26: A sample output curve generated using the software