Lab #2

Due: *Monday, April 21st, 11:59 PM (Design Review)*
Due: *Thursday, April 24th, 5:00 PM (Lab Report)*

Your second project at Triton Industries, Inc. is to re-layout the comparator in your high-speed SAR ADC considering matching. The schematic is shown in **Figure 1** and provided in the starter files ($PUBLIC/labs/Lab_2). You are allowed to resize the devices, specifically to finger the device. All dummy devices must be back annotated onto the schematic. Your layout must pass DRC, LVS, and have an offset of less than ±0.5 LSB (3.9 mV) with an RCX filter cap limit of 50 aF and a propagation delay of less than 2 ns (for a 0.1 LSB input) across process corners and mismatch. The SAR inputs should be on the left side of the block, and the digital inputs/outputs on the right side. All pins must be labeled and on metal 4. You are strongly encouraged, although not required, to label all internal nets.

You must work on this in teams of two. Each team must submit one project report as specified below. You are encouraged to discuss the design problem with other teams, but your implementation *must be unique*. Under **NO** circumstances should you exchange computer files with other teams; this would violate the student honor code and be submitted to the academic integrity office.

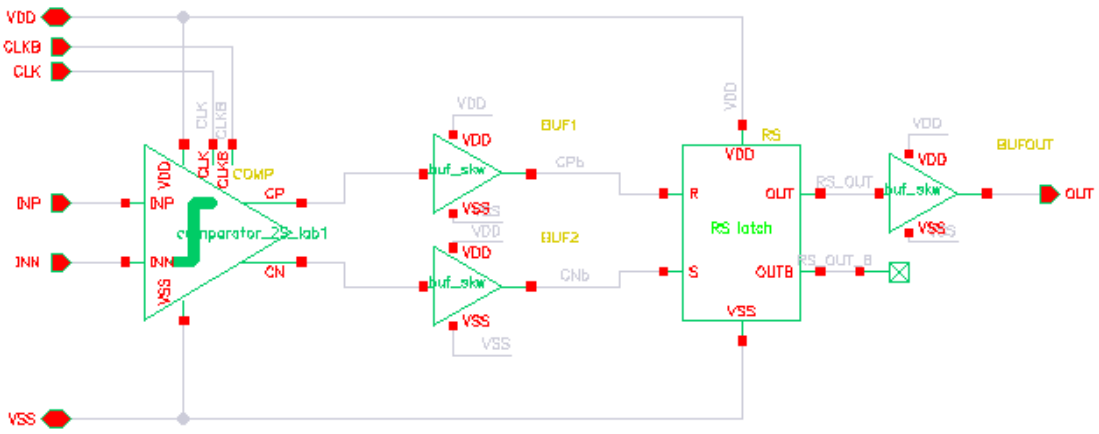

Figure 1 – Schematic of the comparator

Keep in mind that this project involves a great deal of plain old labor; it takes a significant amount of time to learn the tools, floorplan, wire up the design, run the necessary design checks, and clearly document your work. Don't delay getting started!

Project Report: Your team is required to prepare a single report. Reports must be submitted online through Canvas. *We will not grant any extensions.* Reports are in the form of PowerPoint slides and must follow the following structure:
Slide 0: Cover page. Indicate the names of the team members, including PID and email.
Slide 1: Schematic annotated with dummy devices. (White background only)
Slide 2: Picture(s) of your comparator layout. Annotate the devices/blocks and the dimensions of the block (using rulers). Make sure to have at least one top-level block.
Slides 3-4: DRC and LVS results.
Slide 5: Capacitance table showing cap-to-ground and coupling caps for all nodes. Compare against Lab 1.
Slide 6: Simulation results showing the input-referred offset of the extracted comparator using Monte Carlo. Compare this to your Lab 1 results. Also, show process corner simulations. Summarize your results in a table.
Slide 7: Simulation results showing the propagation delay of extracted comparator across corners. Compare this to your lab 1 results (where we didn't even consider this).

Slide 8-11: Summarize your strategy, floorplan (metal routing), and approach. Explain the techniques you used to achieve the performance, using figures as necessary. Convey any issues you encountered with the lab. Comment on places where you would improve the layout if you had more time.

Grading Rubric: 40% design, 10% DRC clean, 10% LVS clean, 10% simulations/comparison, 10% summary, and 20% design review. Points will be deducted for non-professional presentations at my discretion.

Frequently Asked Questions

The R-C-CC extracted simulation is very different from the C-CC simulation in terms of offset! What is wrong?
If you look in the output window, you'll (likely) see several errors about "trapezoidal ringing." This is telling you that the simulator is having trouble converging. Change the simulation options to "Conservative" and then under transient, click on Options and select "gear2only." This should fix the problems.

When should I use nch_mac or pch_mac devices?
During Monte Carlo mismatch simulation. These contain the statistical parameters of the model. Without them, you won't see any device-to-device variation!

Should I use *_mac devices for Monte Carlo process simulation?
No, you should keep the devices basic for process simulation. Note that it is important to differentiate between PROCESS and MISMATCH in Monte Carlo. If this doesn't make sense, re-read the lecture slides!

When running MC analysis on the delay testbench, many of my runs have errors due to what I believe is the larger offset. Is that correct/expected?
Yes. You can try increasing V_{IH} and decreasing V_{IL} simultaneously to see the number of errors decrease.

There is an error about missing "par1fn_mc" parameters in my Monte Carlo simulations. Why?
You are missing a library. Add stat_mis, stat_noise, tt, and tt_lvt.

What is the difference between DRC and DFM?
DRC ensures compliance with the design rules and helps prevent manufacturing defects and fabrication errors. DFM takes this further by implementing design practices and techniques that improve manufacturability. DRC is essential for fabricating your chip, whereas DFM techniques are followed on top of DRC to improve performance and other factors.

How do I change basic to MAC devices in layout for post-extraction simulations?
Add the LVSDMY layer over the devices before extracting. Alternatively, you can modify the netlist to add _mac to the devices, but I strongly recommend the former approach where the tool takes care of this!

How do I exchange files with my lab partner?
We have a shared folder called FileXchng. Copy the library using: cp -r filename destination_dir. Then navigate to FileXchng and run: chmod -R 777 filename (Note: the -R is case sensitive). Now, your teammate can copy the file to their home directory. Afterward, remove the file from FileXchng: rm -r filename Finally, in Cadence Library Manager, go to Edit → Library Path and create a new path for the copied library.

That seems hard… and laborious. Isn't there a better way?
Yes… but we need to get ITS involved! This takes time. For Lab 2, we will use the above method. For subsequent labs, we will have them create "groups" that you and your teammates are members of. The shared files will go in these shared folders.

Where do I submit my design review files? Can I present from my own computer?

A DropBox link will be provided. All presentations will be from my computer to maximize our time. Name your file group # _LastName1_LastName2. PDF and PPTX accepted.