Lab #4

Design Review: *Monday, Jun 2nd, 11:59 PM*
Report Due: *Tuesday, June 10th, 11:59 PM*
Preliminary GDS: *Monday, June 2nd, 5:00 PM*
Final GDS: *Monday, June 9th, 5:00 PM*

Your final project at Triton Industries, Inc. involves adding decoupling capacitors, designing a pad frame with appropriate ESD protection, and integrating your SAR ADC. The chip will have multiple SAR ADCs (yours and a few other teams). Your layout must pass density, DRC (full chip), LVS, and ERC. It is up to you to think about where to floorplan your blocks and create the layout. You need to back-annotate your schematic with any decoupling capacitors you add. You must mux the digital outputs (B0-B9 and EOC) and share the pads with the other teams. You may need to add buffers to route your digital signals to/from the pads. The input signals do not need to be muxed, nor do VSS/VDD and CLK. Lastly, you need to stream out your design to generate a GDS and stream it back in to verify that it was generated correctly. Finally, you need to add the TSMC seal ring to the outside of your chip. The final chip dimensions must match (exactly) the dimensions provided to your mega-team (including the seal ring).

You must work on this in mega-teams based on the distributed table. Each team (not mega-team) must submit one project report as specified below. You are encouraged to discuss the design problem with other teams, but your implementation *must be unique*. Under **NO** circumstances should you exchange computer files with other teams; this would violate the student honor code and be submitted to the academic integrity office.

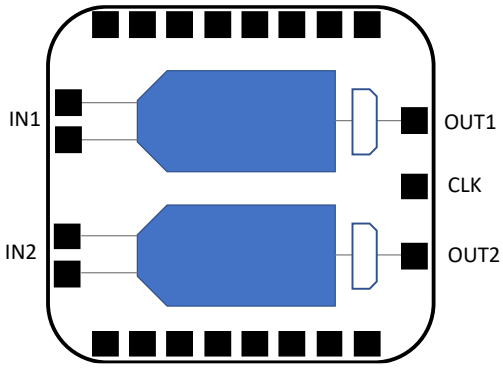


Figure 1 – Multi-channel SAR ADC

Project Report: Your team is required to prepare a single report. Reports must be submitted online through Canvas. *We will not grant any extensions.* Reports are in the form of PowerPoint slides and must follow the following structure:
Slide 0: Cover page. Clearly indicate the names of team members, including PID and email. Include your mega-team number.
Slide 1: Top-level schematic with back-annotated decoupling capacitors. Annotate with the total amount of decap added to each supply.
Slide 2: Schematic of the pad ring. Annotate the pin direction and I/O type.
Slide 3: Tabular format documenting the pad frame.
Slide 4-7: Pictures(s) of your top-level layout. Annotate the pin locations and the block's dimensions (using rulers).
Slide 8-9: DRC and LVS result summary.
Slide 10: Density of each metal layer in a table + photographs.
Slides 11-14 (or more): Top-level (whole chip + ESD) simulations with the pin model (in the starter code) demonstrating that your design functions correctly and meets specifications. At a minimum, show ramped startup transient, at least one full SAR conversion cycle, and the SNR/SNDR performance. This is your LAST chance to convince me that your design works and

should be taped out!! This is ***incredibly*** important! Note that you may be unable to simulate with the dummy fill due to computational constraints.

Slide 15-18: Summarize your strategy, floor plan, and approach. Explain the techniques you employed to achieve the performance, using figures as necessary. Convey any issues you encountered with the lab. Comment on places where you would improve the layout if you had more time.

Grading Rubric: 30% design strategy and floor planning, 10% DRC clean, 10% LVS clean, 20% simulations, 10% summary, and 20% design review. Points will be deducted for non-professional presentations at my discretion.

Frequently Asked Questions

How should I get started on Lab 4?

My recommended flow:

- Meet with your team and do a high-level placement of your various blocks and do the pin assignment. I usually recommend doing this in Excel rather than Cadence directly. You'll need to determine the number of pads you have based on the allotted area.
- Divvy up the ancillary tasks (*i.e.*, mux, pad frame, sealring, fill, etc.)
- Fill your blocks with decap and density in the allotted area. Use blocking over sensitive parts of your design.
- Place all the blocks together and make sure there are no DRC errors
- Top-level connections to the pads
- Fix antenna errors
- Top-level density fill
- Verification simulations!!!

Is there a checklist for things I should check before submitting the GDS?

Yes! Here is a quick checklist. It is not all-inclusive but captures many issues that have come up previously. I would encourage every group to have a few members independently check this off since it affects EVERYONE on the chip!

- ☐ The lower left of the chip AND the boundary is at (0,0).
- ☐ The boundary does not exceed the allocated X/Y dimensions. (Yes, by even 0.05µm!)
- ☐ Verify that you've inserted buffers for routing distances greater than 500 um and sized them appropriately. (Check your logic → DAC switches!!! This delay can cause problems if it is too long. Also, check your pad → digital logic and digital logic → pad connections.)
- ☐ There are no critical DRC errors (see below) on a full chip DRC. Make sure you have CHIP LEVEL checks enabled!
- ☐ LVS is clean. (Make sure you do NOT have soft connect enabled!)
- ☐ Antenna is clean.
- ☐ Verify you did not use AP metal for internal routing.
- ☐ Verify that your design has the seal ring.
- ☐ Verify that you've included the dummy fill.
- ☐ Create a waiver request for the final GDS for every error.

What DRC deck should I be using for the final tapeout?

Ensure you use the "Calibre_fullchip.drc" deck to check your whole chip. This DRC deck has additional switches enabled to look at the seal ring and ESD structures. This is the DRC output that needs to be submitted with your full GDS.

Can we go a little over the die area provided in the spreadsheet?

NO!!!! The dimensions of your chip (including the padframe, sealring, etc.) need to be EXACTLY what I sent you – not less, not more.

There are DRC errors in the foundry-provided cells! Should I fix them?

No! There are some known issues in the standard cells. These are waivable and should NOT be fixed. The foundry knows what they are doing in violating these errors. Sometimes there is a floating NWELL error in the AVSS pad that can also be safely ignored.

The following are known DR issues in the TSMC-provided cells:

- ESD.21g (in PVDDANA)
- ESD.22g (in all Oscillators, all 1/0 cells)
- ESD.23g (in PVDD2ANA)
- PM.W.1 (in the sealring)

The following are known DFM issues in the TSMC-provided cells:

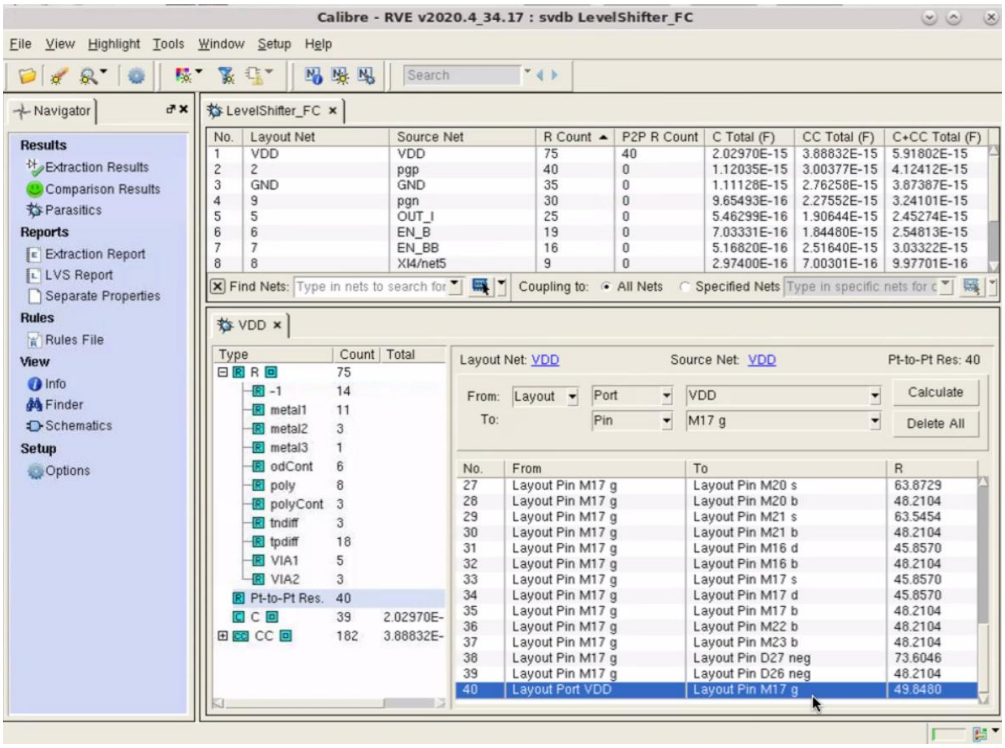
- RR:AR:SP:POEN1 (in all I/O cells)
- RR:AR:SP:POEN2 (in PCLAMPIANA, PCLAMP2ANA, PVDDIANA, PVDDIDGZ, PVDD2ANA, PVDD2DGZ, PVDD2POC, all Oscillators, and I/O cells)
- RR:AR:SP:POEN3 (in PVDDIANA, PVDDIDGZ, PVDD2DGZ, PVDD2POC, all Oscillators, all I/O cells)
- RR:AR:SP:POS14 (in PVDDIANA, PVDD1DGZ, all I/O cells)
- RR:GL:SP:NWR1 (in PFILLEROS, PFILLER1)
- RR:RE:S:MIS7 (in chip level)

What about other errors? Can I get a waiver?

ESD.22g can be waived. Density-related errors can sometimes be waived. These are NOT guaranteed; you must be ready to fix them if they deny the waiver request. This can happen during/after finals; be ready for this!

How can I see the resistance of a trace in layout?

There is a tool in Calibre that you can use to do this in the RVE window. Specifically, you want to look at the pt-to-pt Res in the RCX tool. See the example below showing 40 Ω.



Great… Why would I want to do this?!

This is very useful for debugging IR drop issues and finding where your routing adds significant resistance. Looking at the list below, you will see ALL the routes contributing to that final number.

I am getting a LUP.6 DRC error. How do I fix this?

You will get this error if you have a floating NWELL or PSUB guard ring and try running DRC without connecting it to the respective potential. This should be clean once you do the routing and have the necessary body connections. So, if you are getting this error after device placement, it is fine to ignore it. If this is a fully connected layout, you need to fix it!

I am getting antenna errors. How can I fix them?

You have two options: add antenna diodes or use metal bridges or jumpers. The latter is the preferred method as it will incur a much smaller performance penalty, especially in analog circuits.

Can you perform a dummy fill with the seal ring in place?

Yes (but you probably shouldn't). If you want to do this, draw a dummy exclude (all layers) and POBLK over the seal ring. Then, run the dummy fill script. Finally, you need to remove the POBLK layer; otherwise, DRC will fail.