Lab #1

Due: *Thursday, April 10th, 5:00 PM*

Your first project at Triton Industries, Inc. is to lay out the comparator in your SAR ADC. The schematic is shown in **Figure 1** and provided in the starter files ($PUBLIC/labs/Lab_1). Due to time-to-market constraints, your manager insists you *do not* change the schematic. Your focus is to lay out the circuit and ensure it passes all design rule checks (DRC) and matches the schematic (LVS). The inputs should be on the left side of the block, and the output should be on the right side. All pins must be labeled and on metal 4. You are strongly encouraged, although not required, to label all internal nets.

You must work on this alone (all subsequent labs will be in pairs). You must submit a project report as specified below. You are encouraged to discuss the design problem with other teams, but your implementation *must be unique*. Under **NO** circumstances should you exchange computer files with others; this would violate the student honor code and be submitted to the academic integrity office.

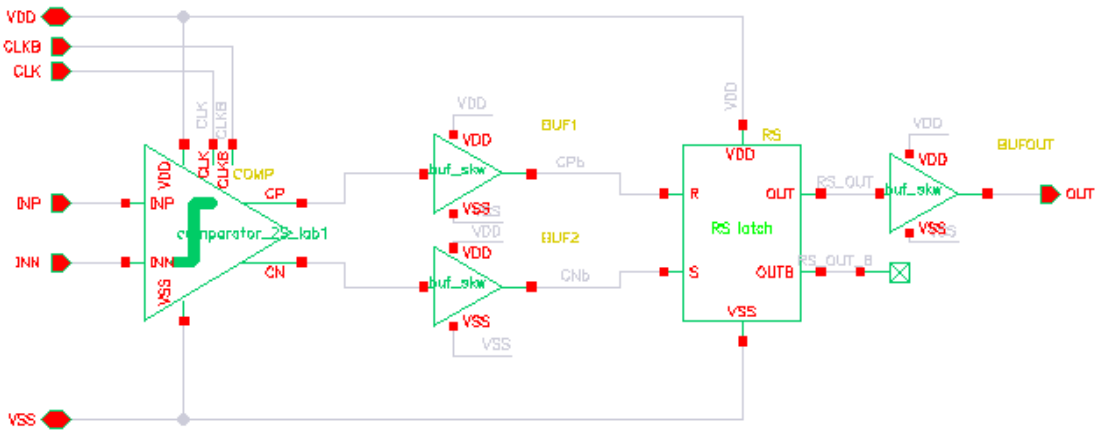


Figure 1 – Schematic of the comparator

Keep in mind that this project involves a great deal of plain old labor; it takes a significant amount of time to learn the tools, floorplan, wire up the design, run the necessary design checks, and clearly document your work. Don't delay getting started!

Project Report: Reports must be submitted online through Canvas. *We will not grant any extensions.* Reports are in the form of PowerPoint slides and must follow the following structure:
Slide 0: Cover page. Clearly indicate your name, PID, and email.
Slide 1: Picture(s) of your layout. Annotate the devices/blocks and the dimensions of the block (using rulers). Make sure to have at least one top-level block.
Slide 2: DRC result summary.
Slide 3: LVS result summary.
Slide 4-6: Summarize your strategy, floorplan (metal routing), and approach. Convey any issues you encountered with the lab. Comment on places where you would improve the layout if you had more time.
Slide 7-X: Proposal to do a project "extension." All extensions must use the SAR ADC as a core but can augment it in various ways described in class or as you propose. Include your proposed team, plan, timeline, and key references.

Grading Rubric: 50% design, 20% DRC clean, 20% LVS clean, 10% summary. Points will be deducted for non-professional presentations at my discretion.

Frequently Asked Questions

Is my password the same as my single-sign-on (SSO)?
NO! This is a different account and password.

What is the link to reset the password?
Here is the link: Reset Password

How do I check if I have permission to access the PDK?
Type '*groups'* in a terminal. You will see ieng6_ibm_pdk1 if you have been added. There is also a list of authorized users in $PUBLIC/TSMC-PDK-accounts. Why is it "ibm_pdk" rather than "tsmc_pdk"? I have no idea… I ask myself this often!

I cannot see the TSMC PDK in the Cadence library, but I was added to the group.
You should run the following commands before launching Virtuoso to create initial libraries:
cd
mk_setup_files

I don't know Unix/Linux… How can I learn more?
Most electronic design automation (EDA) tools are Unix-based. It is important to have at least a cursory ability to navigate around. There are a lot of great tutorials on the internet with much more comprehensive lists, but really, a few commands will go a long way!
ls – list directory contents
cd – change directory
pwd – print current (working) directory
mkdir – make a directory
cp – copy file/directory
mv – move file/directory
rm – remove file/directory
cat – display the content of a file
grep – search for a pattern in a file
top – utilization of the computer
virtuoso – Cadence virtuoso
If you want to learn more about the parameters of any of the above, use the command man <cmd>.

What important files should exist in my home directory before launching Virtuoso?
Cadence uses a few files in your home directory for configuration. Specifically, .cdsenv (environment setup), .cdsinit (initialization), and cds.lib (library paths). The mk_setup_files script just copies these into your folder! Note that any file that starts with a period is hidden in Linux by default. To view these files, you can type ls -a. If you started Cadence BEFORE running the mk_setup_files command, Cadence will create these files for you, but they won't be set up properly! Delete them and run the mk_setup_files command.

I can't find the Lab 1 library.
The libraries should auto-populate in your library (if you've run the mk_setup_files script above). If you still cannot see any assignment libraries, you can go to Virtuoso → Tools → Library Manager → Edit → Library Path. Add the following details:
Library: Lab_1 Path: $PUBLIC/labs/Lab_1

Where can I find the PDK documentation?
The files are located at: $PUBLIC/Documentation

Can I download the PDK documents to my laptop/computer/phone/… for easy access?
No, remember you have signed an NDA, and these documents are part of the PDK. They need to stay on the server.

What should the grid be?
The grid needs to be 0.005! You should *always* check that this is correct. If you do a layout with a different setting here, it may not be fabricatable, and you will get "off-grid" errors when you run DRC. You can set this up as the default in your .cdsenv file by adding the following:

```
layout  xSnapSpacing    float      0.005
layout  ySnapSpacing    float      0.005
```

Is there any preferred metal orientation that we should follow?
Usually, odd metal layers have a vertical orientation, and even metal layers have a horizontal orientation. This is not a hard rule but a general practice that makes layout design easier at higher hierarchies. It is also important to be consistent with metal orientations when combining blocks with other groups in later labs. For Metal 1, it is hard to abide by this and is usually routed wherever without much thought. For higher metals, it is stricter.

The layout window is getting stuck. How do I fix it?
Try minimizing and maximizing the window. This usually does the trick!

How do I add a PR boundary?
To add a PR boundary, follow these steps: Create → P&R objects → P&R boundary

I am running out of disk space! How can I figure out what is causing this?
The most common cause of this is using the web browser and the cache files it generates. Try emptying these first. If you are still having issues, type the following command in your home directory:

```
du -sh * | sort -h
```

Check the common "culprits" – ~/simulation and ~/SVDB folders!

I am getting an LVS error about not recognizing ports/pins.
Place the pin and its label in the Mx pin layer. For example, if your power rail is in the Metal 4 layer, you need to keep the pin and its label in the Metal 4 (M4) pin layer. Ensure the label is placed inside your pin.

I am getting an Invalid PATHCHK request LVS error. What is wrong?!
You should define VDD and VSS in your LVS run setup. For some small cells like custom capacitors, you might not have VDD/VSS pins, in which case you can safely ignore these errors.

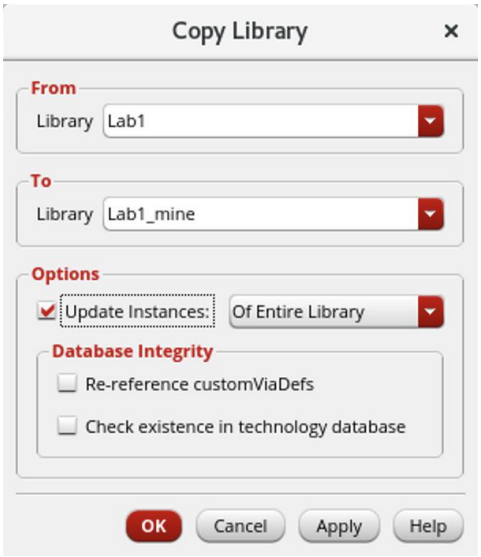
I am getting an LVS error about stamping.
This is usually caused by a guard ring not connected to VDD or VSS or a floating body. Check to ensure it is connected and that you have told Calibre the names of the power supply nets.

I get an error saying, "Failed to check out license 'Analog_Design_Environment_XL'." What is wrong?
This error is typically caused when you (accidentally) click "never" while checking out a license for ADEL/ADEXL. Check your .cdsenv file and ensure you have the following:

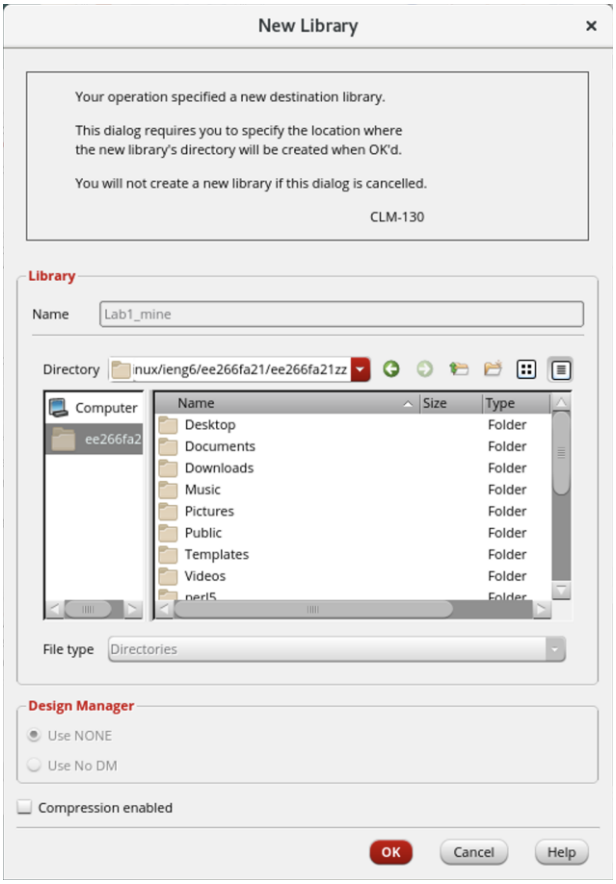
```
license VLSXL_UseNextLicense string "always"
license ADE_UseNextLicense string "always"
license ADEXL_UseNextLicense string "always"
license ADEL_UseNextLicense string "always"
license VSEL_UseNextLicense string "always"
```

When I open Lab1, it says, "read-only!" How do I fix this?

When you open Cadence, you will see the library, but it will be "read-only." Copy it to your folder to modify it (*i.e.*, to do the layout). To do this, in Library Manager, right-click on Lab1 and select Copy. This will bring up the following window:



Change the To library to a new name (*e.g.*, Lab1_mine). Make sure that Update Instances is checked! Then click OK.



This is where you choose where to save the new library. Put it in your home directory. If you mess up the starter code for any reason, you can recopy the entire library (as above) or individual cells.

How can I export an image with a ruler?
Cadence does not support this. As an alternative, you can use other screenshot apps. The figures are more readable when you invert the colors (white background).

Okay, so the transistors in the comparator schematics are sized at 60 nm. How is it possible in a "65 nm" PDK?!
The 65 nm PDK was originally released with L_{min}=65 nm in 2005, but a "true shrink" was done over time, reducing L_{min} to 60 nm. This is not always done, but it is sometimes done for a heavily used node (like 65 nm). This is done to improve gate density, typically for digital-heavy circuits.

Do we need guard rings everywhere, even if I have cells like an inverter/buffer?
Having a guard ring for good isolation for analog blocks is critical. For digital cells like an inverter/buffer, you can have a tap connection instead to save space, provided it doesn't create any noise issues for the neighboring cells.

The grading rubric says, "Points will be deducted for non-professional presentations at my discretion." What does that mean?
Anything you would not want to/be proud of presenting in front of your (current/future) employer! For example, unreadable/blurry figures, low-effort screenshots, no annotations, etc. Spend a few minutes and clean up your presentation; it likely won't be an issue!

The slide format does not let me elaborate enough on XXXXX. Can I add slides talking about it?
Yes, you can add anything you want to the appendix section! There is no guarantee that we grade/look at it, but if you need additional slides to convey something, this is the right place to add it. Do not change the pages otherwise!