2025 VLSI SYMPOSIUM

From Schematic to Silicon: ADC Tapeout in 10 Weeks

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JACOBS SCHOOL OF ENGINEERING

Course Overview

- 2-quarter course sequence
  - ECE 266A (Spring): Physical design and simulation
  - Chip fabrication (over the summer) <-- Critical for a quarter-based system!
  - ECE 266B (Fall): Measurement and characterization

- Designed for senior-level undergraduate and first-year graduate students

- First offered in Fall 2021, annually since, enrollment limited to 50
  - >18 chips taped out (!!!)
  - >200 students have completed the course (~25% PhD, 37% MS, 30% BS-MS, 8% UG)

What is ECE266?!

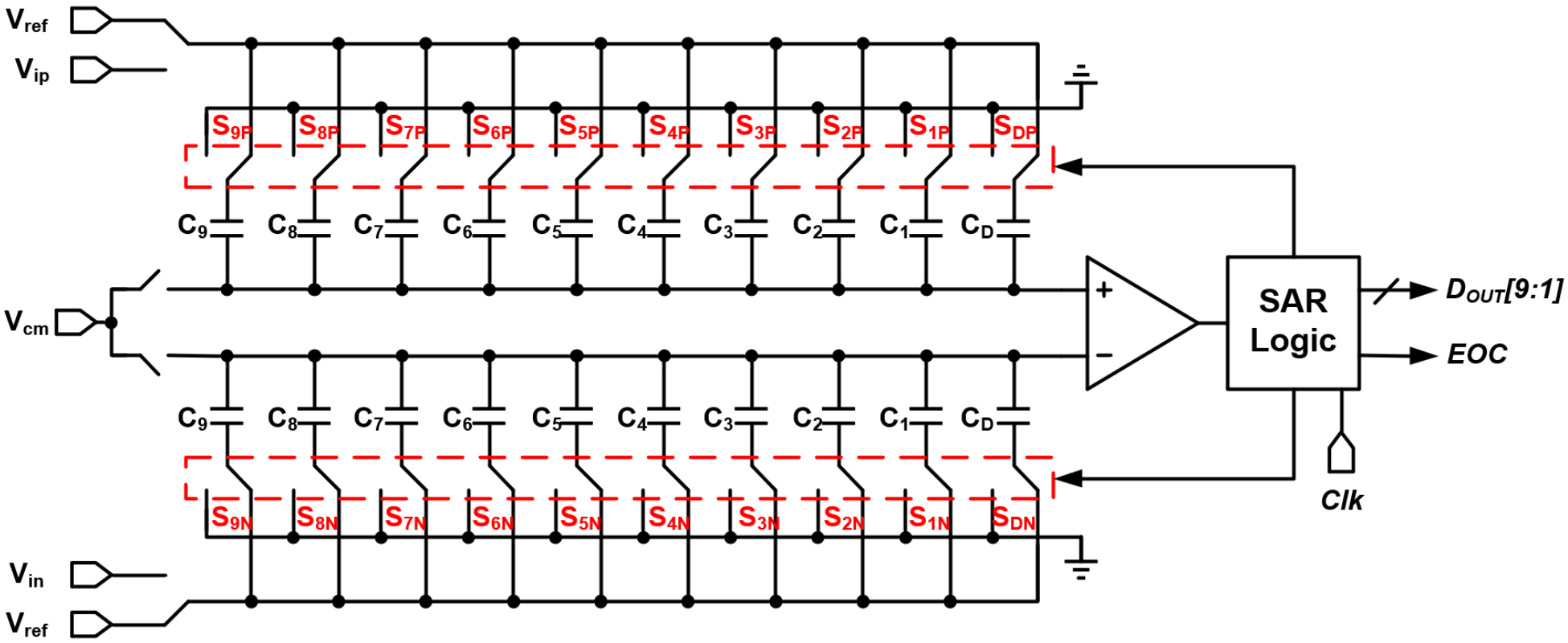
- A class meant to augment students' circuit design skills by teaching:
  - Physical design and layout techniques
  - Device matching techniques and the impact of parasitics
  - Special topics on RF layout, power converter, digital synthesis, etc.
  - Design-to-fab integrated circuit design flow
  - Packaging and PCB layout (ECE 266B)
  - Measurement equipment and automation (ECE 266B)

- A course to complement students' growing design experience with skills that are needed for IC designers

Why teach this kind of course?

- Traditional VLSI curricula emphasize *theory* but fall short on practical implementation
- This course provides hands-on experience across the full chip lifecycle, from schematic to silicon
- Prepares students to be complete engineers, not just theoreticians or tool operators
- Aligns with industry demand for graduates who understand tools, flows, and post-silicon validation
- Empowers undergraduates with experiences typically reserved for graduate-level research

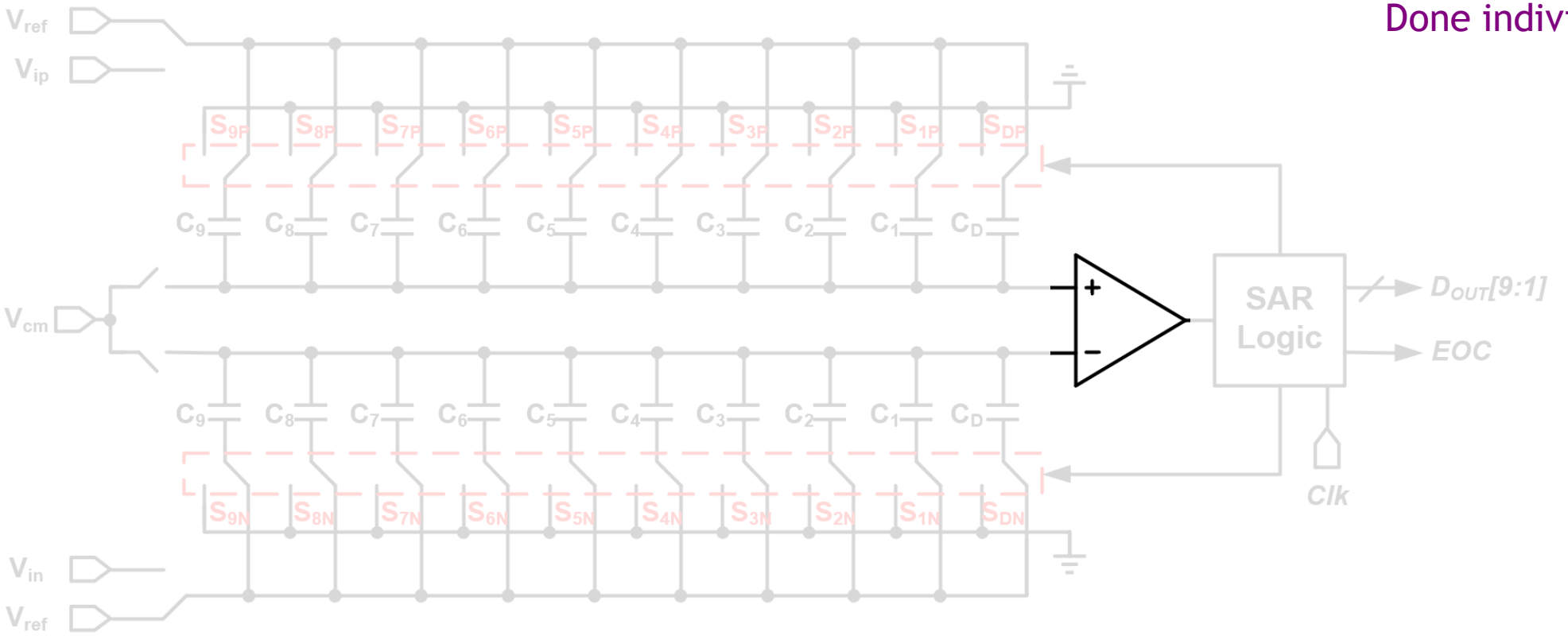
10MS/s, 9-bit Asynchronous SAR ADC



All schematics, testbenches, and Verilog code provided

Lab 1 - Layout the comparator

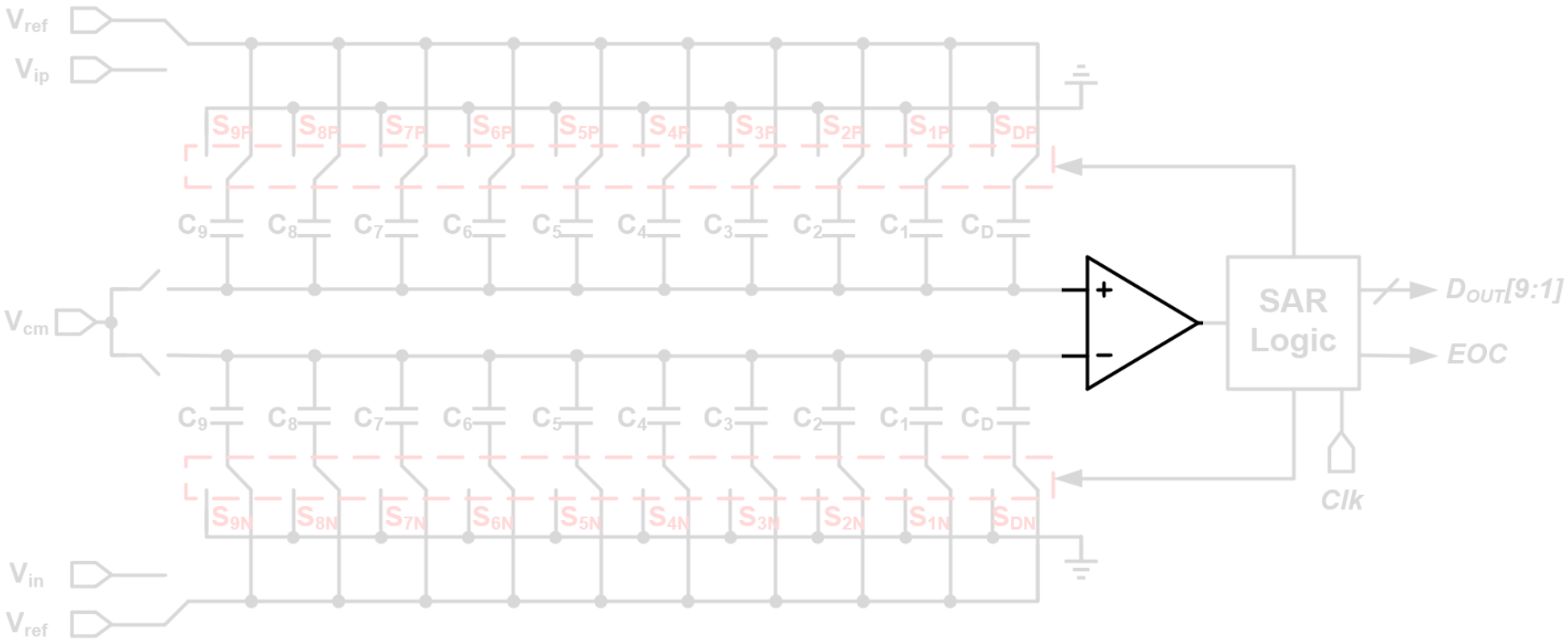
Done individually



Learning objectives: Using the tools (layout, layout vs. schematic)

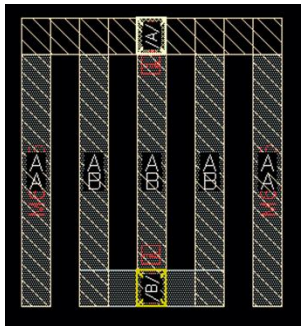
Lab 2 - Re-Layout the comparator

ams of 2



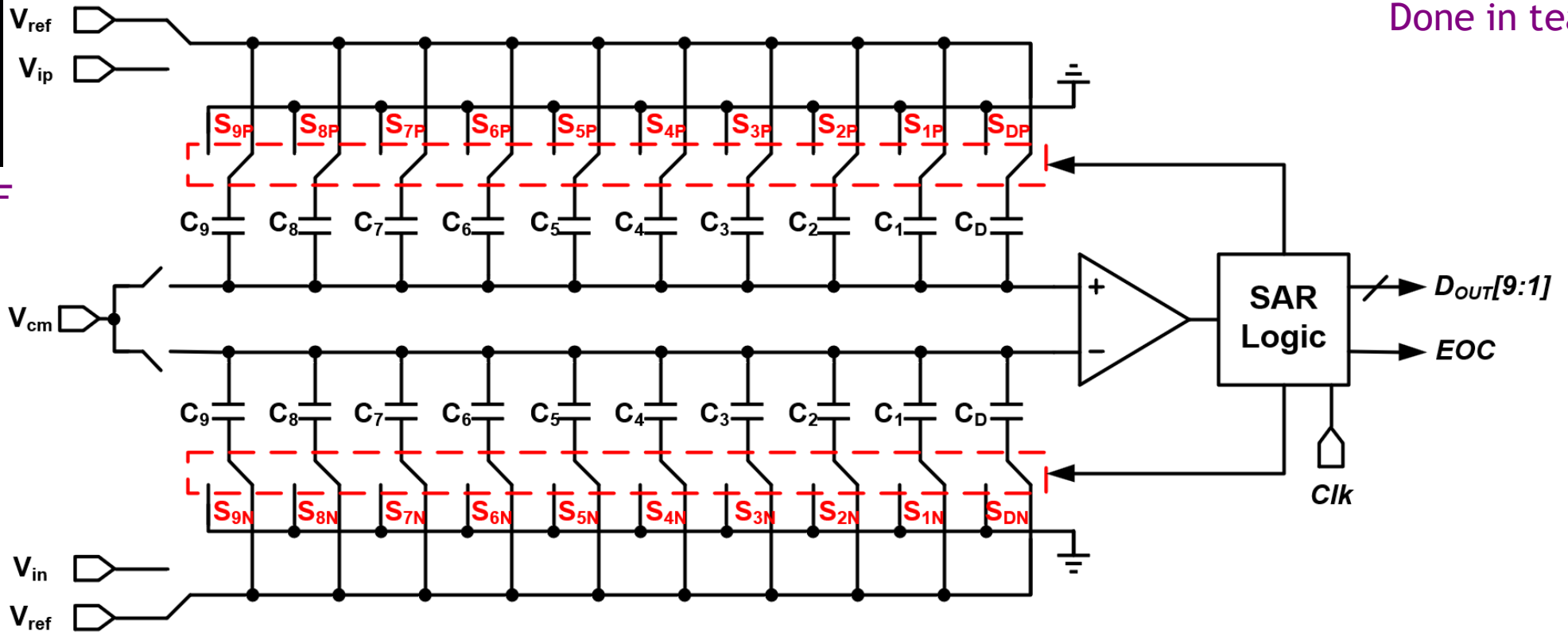
Learning objectives: Use matching techniques, post-layout extraction aware analog design (iterate & compare with Lab 1)

Lab 3 – CDAC & Switch Layout, Digital Synthesis



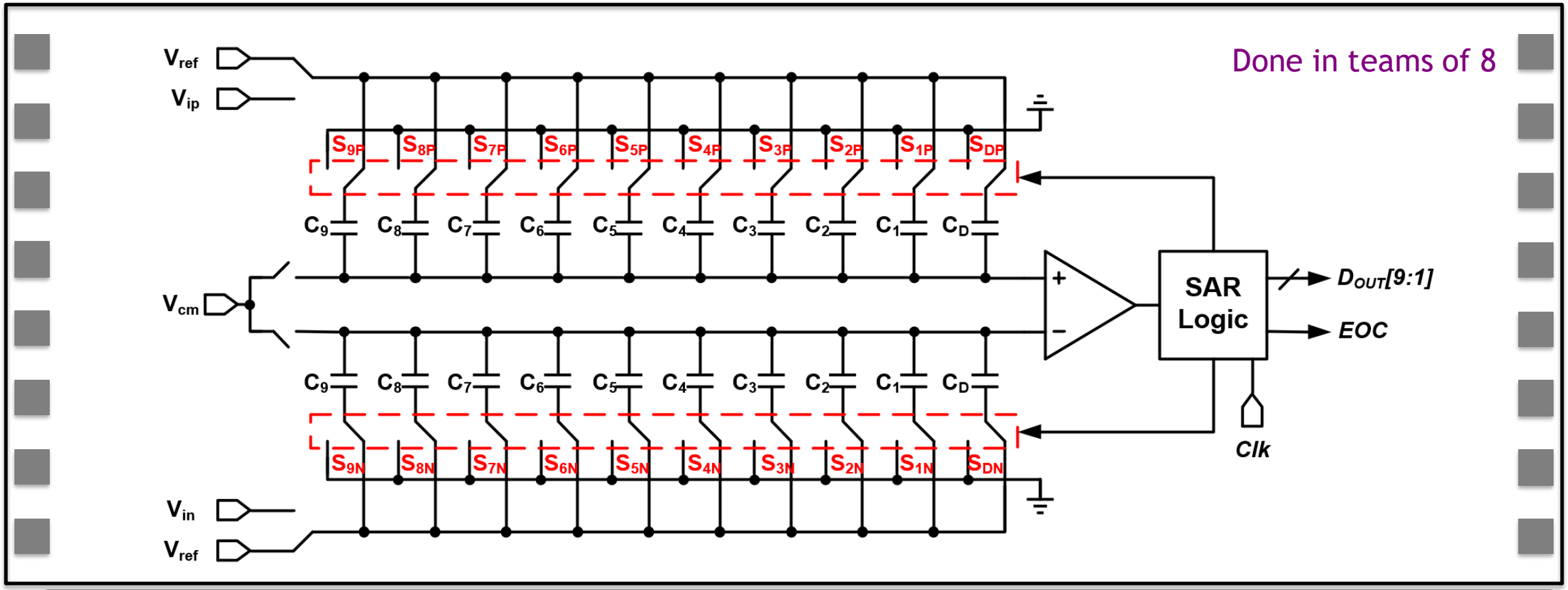
Custom ~5 fF MOM caps

Done in teams of 2



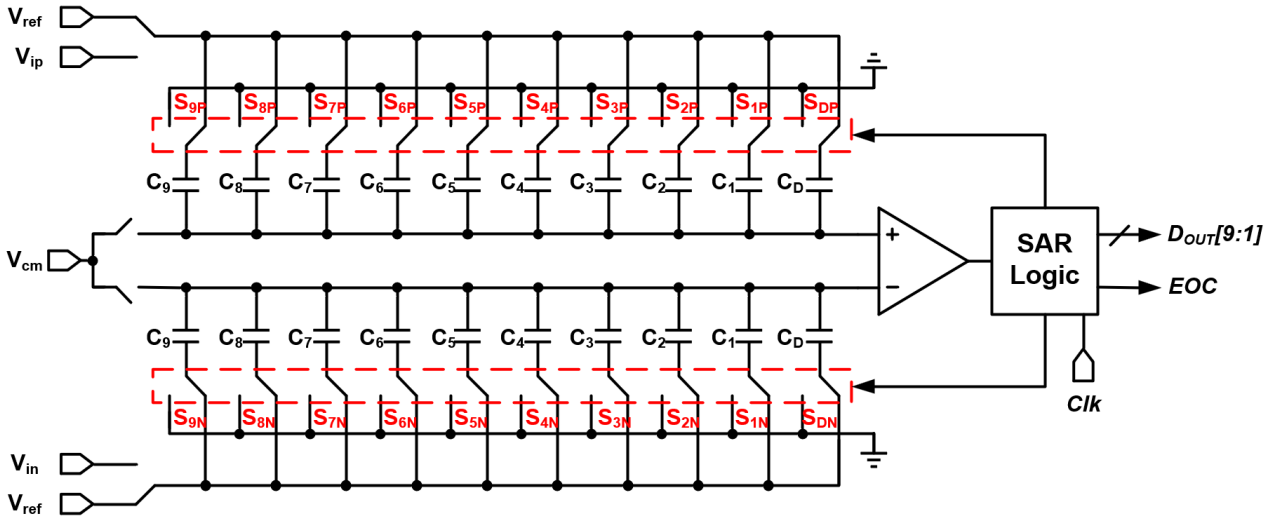
Learning objectives: Implement common centroid layout, achieve good CDAC matching (binary weighted), and run digital synthesis

Lab 4 - Padframe, ESD, and Fill



Learning objectives: Meet density rules, fixing antenna errors, add decoupling capacitors, integration (4 ADCs/chip), and teamwork

Project Extension Opportunities



Analog

- Bootstrapped sampling switches
- Split-capacitor DAC
- Delta-L DAC
- Noise-shaped SAR
- ExG (or another sensor) amplifier/PGA
- Time-interleaved SAR
- Comparator offset calibration

Digital

- Different DAC switching scheme
- ExG feature extraction/classifier
- Calibration engine (cap/comparator offset)
- Standardized serial interface (I2C, SPI, etc.)
- Digital top (synthesized pad-ring)
- Filtering/signal conditioning

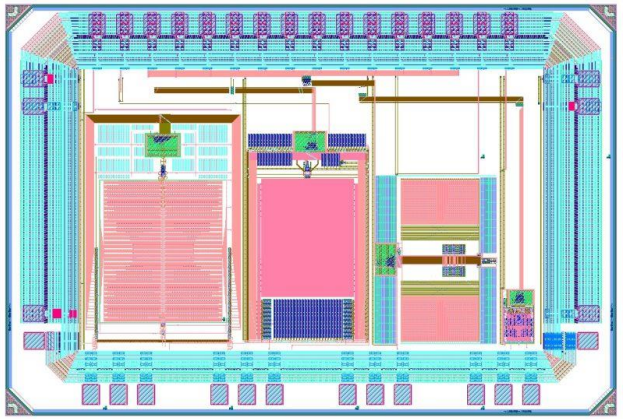
Tools and Technology

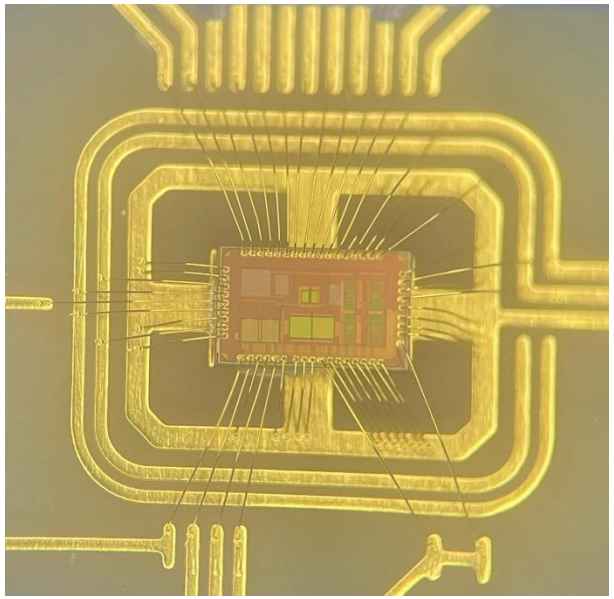
- Predominantly a Cadence workflow
  - Virtuoso, Layout, Analog Design Environment, Genus, Innovus, Xcelium, etc.
  - Siemens Calibre for verification (DRC, LVS, PEX)

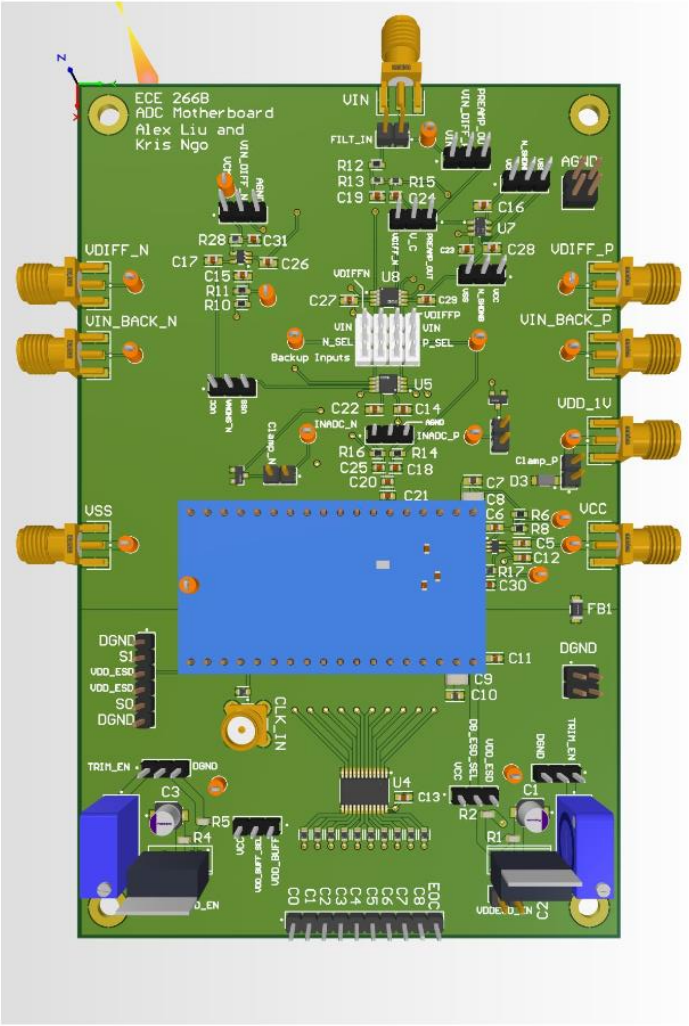
- Why not open source?
  - Relates to the objective of training students for research projects/industry

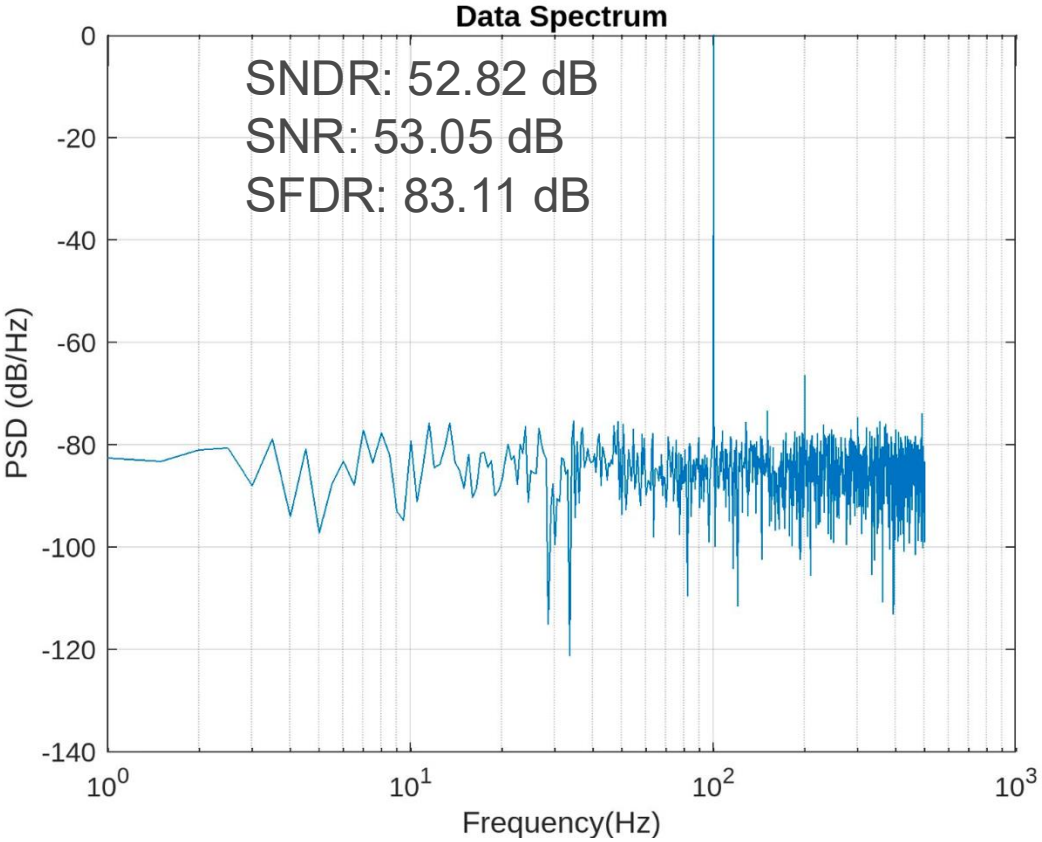
- TSMC 65 GP process node
  - Initially explored SkyWater, but could not get the Cadence PDK due to export control issues…
  - Tight turnaround schedule
  - Standard cell support (logic and ESD)
  - Good balance of layout-dependent effects without going overboard

Project Outcomes









Summary & Lessons Learned

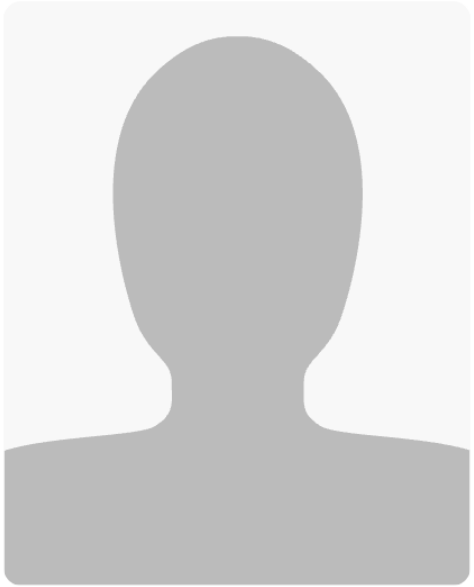
- “Hall’s Law”: In a large class, anything that can go wrong almost certainly will
- Allow students to explore and be creative -- within reason; they often don't know what they don't know!
- Emphasize iteration: design, test, fail, revise
- Reinforce core techniques by putting students in situations where they must apply them
- The project is intentionally structured to expose students to a wide range of design challenges while building on concepts taught
  - Remind students: **not every problem requires an advanced solution**
- Tapeouts are inherently stressful -- no matter how many you’ve done, **only the paranoid survive**
- Students learn as much from each other as they do from the instructor
  - Encourage this through structured peer interaction (*e.g.*, design reviews)
  - Bring in industry colleagues — they add real-world perspective and rigor
- **Industry support is essential**: tapeouts are expensive, and collaborative engagement sustains the course

Acknowledgments

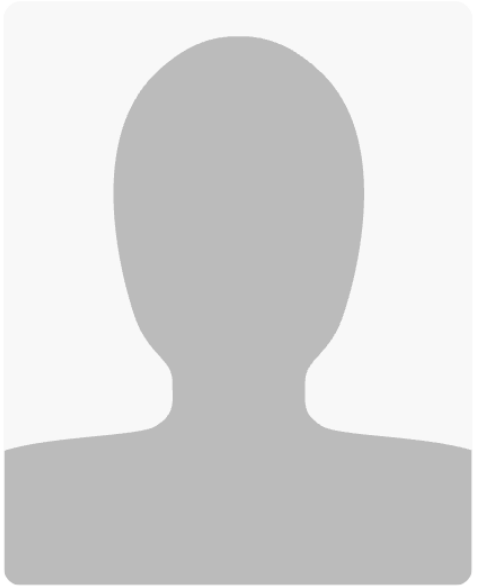
- TAs

Corentin Pochet

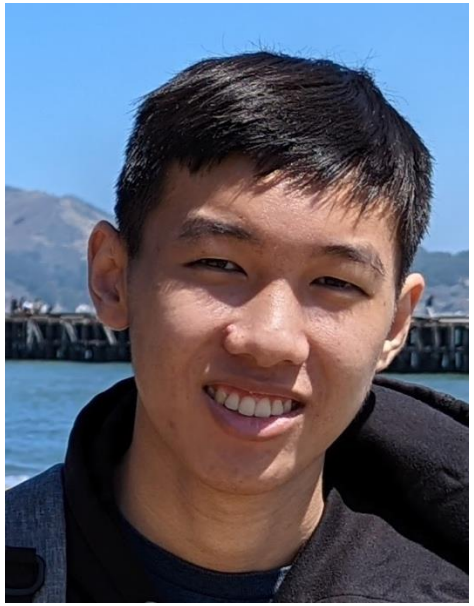
Omid Ghadami



Nuoyi Yang



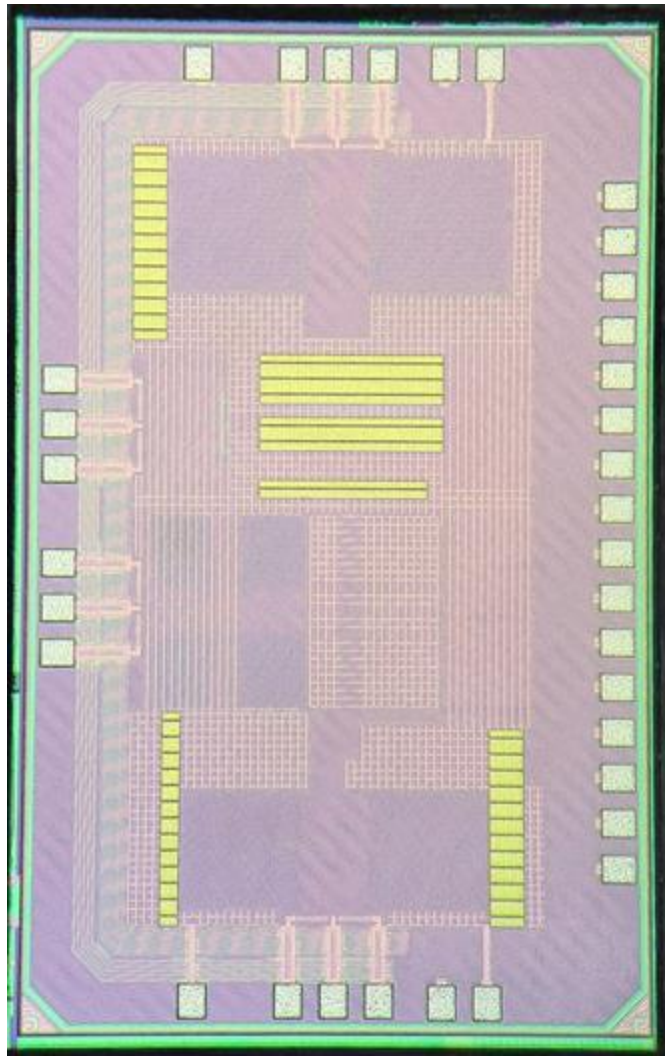
Darshan Balakrishna



Alex Liu

- Corporate Sponsors

Material Available!



SCAN ME

https://github.com/ProfDrewHall/SAR_ADC