

An Analog Gain Inflection Predistorter for Combined Back-Off Efficiency and Linearity With Doherty Power Amplifiers

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Abstract—In this work, a novel tri-branch Doherty analog predistorter (DAPD) for the linearization of gain inflection within Doherty power amplifiers (DPAs) is demonstrated. This proposed circuit topology features two nonlinear branches, which can follow the amplitude and phase characteristic of a DPA in a reverse manner. The first branch conducts whilst the carrier is active in the low power range, whilst both branches conduct when both the carrier and peaking are active in the high power range. A thorough evaluation of this new topology is provided, where the overall gain and phase characteristics of the circuit are mathematically defined. Analysis is provided on various configurations of the topology, where in each case the ability to accurately predistort the gain and phase nonlinearity associated with carrier compression within a DPA is shown. An accurate DAPD design is then detailed, by means of passive modeling, and the use of measured predistortion characteristics of the candidate DPA to be linearized. Measurements are then provided on the combination of the manufactured DAPD with the candidate DPA, through modulated, continuous-wave, and two-tone signal measurements. When considering an orthogonal frequency division multiplexing (OFDM) waveform with varying bandwidths of 20, 50, and 80 MHz, and varying peak-to-average power ratios (PAPRs) of 8.6, 10, and 11.6 dB, a minimum level of adjacent channel power ratio (ACPR) of -40.9 to -43.5 dBc is observed, over a bandwidth of 2.2–2.6 GHz. A minimum error vector magnitude (EVM) of 1.4%–3.8% is also observed, along with a maximum average efficiency of 59.2%–67.5%.

Index Terms—Analog predistortion, Doherty power amplifiers (DPAs), energy efficiency, linearization.

I. INTRODUCTION

MOBILE communications are advancing to service more users and provide higher data rates. This is leading to the use of more spectrally efficient complex modulation schemes, where current schemes combine higher orders of quadrature amplitude modulation (QAM) with orthogonal frequency division multiplexing (OFDM). This leads to waveforms with a high peak-to-average power ratio (PAPR), often exceeding 10 dB with the current generation 5G, leading

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to the adoption of load modulation techniques such as the Doherty Power Amplifier (DPA) within base station radio units [1], [2]. To achieve high efficiency with this technique, the DPA is driven into its nonlinear region of operation where a form of predistortion, typically digital predistortion (DPD), is then used to improve linearity to within limits set by mobile standards [3].

However, there are other recent developments in mobile communications which are contributing to application of DPD techniques, along with the DPA, more complex and power intensive to implement [4]. The first is the widening of the transmission bandwidth the power amplifier (PA) must accommodate, where 5G has introduced carrier aggregation bandwidths of 400 MHz for FR1, and 2000 MHz for FR2 [5]. The other compounding development is the shift toward Multiple-Input and Multiple-Output (MIMO) antenna solutions, where 32–64 transmit elements are typical, thereby lowering the overall power requirements of individual front-end Radio frequency (RF) PAs [6], [7]. The widening of bandwidths necessitates more high-performance DPD processing hardware with increased power consumption, including higher sampling rate digital-to-analog and analog-to-digital converters. This is then exacerbated further with MIMO, where each RF element requires its own DPD, along with a now lower power front-end RF PA, increasing the overall relative power overhead DPD requires from the whole radio unit system.

One way to reduce the complexity of the required DPD is to improve the linearity of the DPA itself through design [8], [9], [10], [11], [12]. This can be achieved by synthesizing an output network with an output phase mismatch, giving an improved AM–PM characteristic [10], [11], or by combining this output phase mismatch with some additional input phase mismatch [12]. In all examples [8], [9], [10], [11], [12], however, any carrier gain compression is limited to improve linearity, which reduces back-off drain efficiency to $\approx 40\%$. Also in [10] and [11], there are instances where small signal gain is low, 7 and 8 dB, likely due some intentional input mismatch used to accomplish higher phase linearity [13], which can reduce the overall power added efficiency (PAE).

Another option for the correction of amplifier amplitude and phase distortion is the use of analog predistortion (APD), either to allow for a reduction in required DPD complexity, or to provide an alternative. APD can use a variety of electronic devices, such as varactors, diodes, or field effect transistors (FETs). APD can be advantageous in its ability

to linearize large bandwidths, whilst also being energy efficient, though typically has lower adjacent channel power ratio (ACPR) correction capability, where DPD techniques are more accurate in providing the required inverse gain and phase predistortion characteristics. APD can generally be characterized as either a tunable diode-based nonlinearity, or an intermodulation distortion (IMD) generator [14]. In a tunable diode configuration, the diode is used to produce an expanding gain characteristic, while a linear delay path is used to provide an inverse phase characteristic of the PA being linearized, with examples in [15], [16], [17], [18], and [19]. An IMD generator is used to produce out-of-phase IMD products at the input to the PA, that cancel with those produced on the output, with examples seen in [20], [21], and [22]. All of these APD examples, however, are limited to linearizing single PAs, where DPAs often feature inflection within its gain characteristic. In [23], an APD was presented which can minimize gain inflection, though the focus of this work was on gain expansion occurring in high-efficiency PA classes, not gain inflection via the different mechanisms present within DPAs.

There are limited examples of the analog linearization of DPAs, with [24], [25]. In [24], an active linearizer amplifier is used, whose output is fed to combine with the output of the DPA, where an ACPR improvement of 11 dB is achieved. Nevertheless, the use of an active device within this work can reduce overall efficiency by around 20%. In [25], two independently tunable linearizers are used in parallel, with both linearizers featuring a parallel diode nonlinearity configuration. However, the system used in this work is complex, with multiple variable gain amplifiers, a phase shifter, and microcontrol unit, resulting in a power dissipation of 1 W.

In this article, a novel Doherty analog predistorter (DAPD) architecture is provided, extending on the initial work associated with the conference paper [26] presented at IMS 2024, Washington, D.C. This article first provides a new in-depth theoretical analysis of the DAPD linearizer. A more detailed discussion on the simulation and design of the DAPD is then provided, including the modeling of passive components and a comprehensive simulation workflow. New measurements to validate the combination of DAPD with DPA are then presented, including IMD and continuous-wave measurements, and additional modulation measurements with different bandwidths and PAPRs. The novel architecture is able to reduce gain inflection present within DPAs, caused by carrier PA compression in the back-off region. The DAPD is able to significantly reduce distortion in the back-off region, near the signal average, thereby reducing spectral regrowth with high-PAPR signals. When compared with other DPA linearizer solutions, this work has advantages in consuming no DC power, offering a purely passive and energy efficient APD solution for DPAs. The integration of the architecture into an overall amplification chain is also straightforward, where the impact of the DAPD's insertion loss can be minimized by recovering gain at low power where there is less impact on system power-added-efficiency (PAE). When comparing with purely design-based linear DPA solutions, the presented DAPD allows for a higher back-off drain efficiency

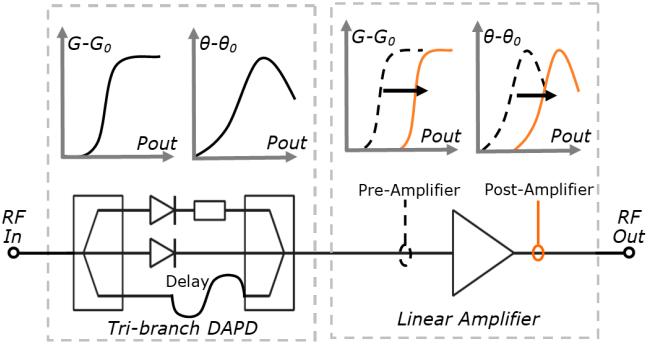


Fig. 1. APD system proposed for the linearization of DPAs, with two elements connected in series: A DAPD with inverse gain and phase characteristics of the DPA to be linearized, and a linear driver amplifier to translate characteristics to the required power level.

to be achieved, whilst still achieving comparable ACPR performance.

This article is organized as follows. First, in Section II, the overall features of the APD system implementation is provided, along with a mathematical derivation of DAPD ideal gain and phase characteristics. In Section III, the passive modeling of diodes, capacitors, and inductors is presented, along with the extraction of target predistortion characteristics of the candidate DPA to be linearized. The design of the DAPD is then detailed, through the use of large signal S-parameter (LSSP) simulations using Keysight's ADS tool. In the final Section IV, the experimental results of the work are detailed, where the combination of the manufactured DAPD and the candidate DPA were measured, using Gaussian pulse, 5G modulated, and two-tone signals.

II. THEORY OF DOHERTY APD

This section first outlines the features of the overall APD system implementation, along with the features of the particular DAPD topology. Detailed analysis is then provided, where the overall gain and phase characteristic of the circuit is mathematically derived. Then finally, various configurations of the topology are provided which achieve the required gain response for DPA carrier gain inflection linearization. The configurations provided also demonstrate the topologies flexibility in being able to linearize this inflection at different power levels, whilst also being able to provide a range of different phase corrections.

A. Proposed DAPD Topology

The aim of the DAPD is to linearize DPA gain inflection resulting from carrier PA compression within a DPA, whilst also predistorting the overall nonlinear phase response of the DPA. The desired outcome would be that the DAPD could allow for greater carrier compression, resulting in a higher efficiency being achieved at the average power of a modulated signal, whilst also maintaining linearity performance. It is required that the DAPD is connected into an overall system, as shown by Fig. 1, which comprises of the following.

- 1) A tri-branch DAPD circuit which provides the correct inverse gain and phase characteristics of the DPA to be linearized.

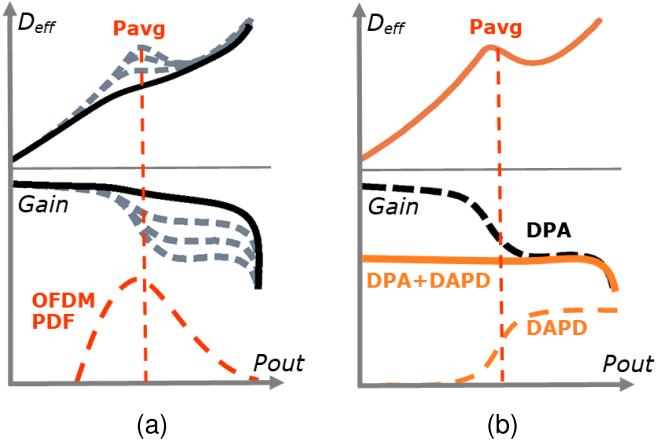


Fig. 2. In (a), greater carrier compression within a DPA allows for higher efficiency to be achieved at the power average of an OFDM waveform, where in (b), proposed DAPD linearizer is used provide an inverse gain characteristic of this gain inflection, to provide a flat gain response and allow for simultaneous efficiency and linearity performance.

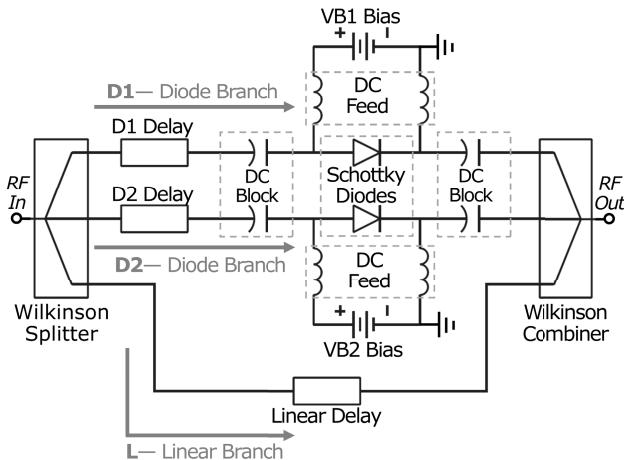


Fig. 3. Proposed tri-branch DAPD architecture, featuring two nonlinear branches with DC biased Schottky diodes, and a linear delay branch.

- 2) A linear amplifier which is used to translate the DAPD inverse characteristics to the required input power level for the DPA.

This overall APD system aims to linearize a DPA which features gain inflection from carrier compression, where this inflection has been predistorted to allow for high simultaneous back-off efficiency and linearity, as depicted in Fig. 2. The circuit block diagram adopted by the proposed DAPD is shown by Fig. 3 which comprises of the following.

- 1) A three-way splitter and combiner in the form of an isolated Wilkinson divider, to provide three signal branches.
- 2) One linear signal branch with a given delay line, allowing for control of the phase response of the overall DAPD.
- 3) Two nonlinear branches featuring reverse-biased series Schottky diodes, with voltages $VB1$ and $VB2$ supplied by DC feeds. Both branches feature delay lines, which can be used to control the overall gain and phase response of the DAPD.

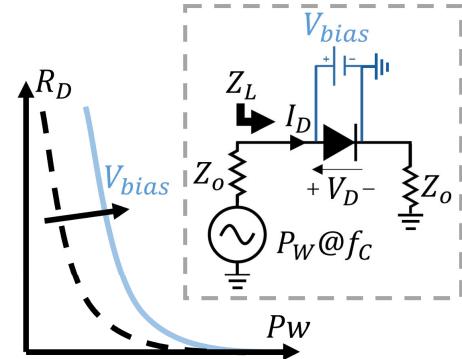


Fig. 4. Nonlinear branch consists of a series diode which has a variable resistance characteristic versus an applied RF power, based on the current flowthrough, and the voltage across the diode. The power at which the resistance varies can be adjusted by applying a negative voltage V_{bias} .

The principle behind this tri-branch architecture is that each nonlinear branch diode is biased differently, where one branch conducts at a lower power level to linearize DPA carrier PA compression. The second branch then conducts at a higher power level, with a different phase delay, such that the gain of both nonlinear branches cancel out to provide flat gain at a higher power level, whilst the peaking PA within a DPA is active.

B. Detailed DAPD Analysis

In this section, the proposed DAPD topology will be analyzed, where the overall gain and phase characteristic of the circuit will be defined. For a simplified analysis, a nonlinear branch within the topology consists of a diode which has a variable resistance versus input power, shown by Fig. 4. This resistance is based on an applied voltage across the diode, and a given current flowthrough the diode based on its IV characteristic. When applied with an increasing RF power, the resistance of the diode will swing from maximum to minimum, due to an increasing RF voltage across the diode causing more RF current conduction. The power range at which the resistance of the diode varies can be adjusted by applying a negative voltage across the diode, V_{bias} , where an increase in power is then needed to overcome this negative voltage for current conduction. This diode resistance can therefore be termed as

$$R_D = \frac{V_D - V_{bias}}{I_D}. \quad (1)$$

Depicted in Fig. 4 is the equivalent circuit of a nonlinear diode branch, where a characteristic impedance Z_0 is defined, and the impedance Z_L looking into the network combination of the diode with a load Z_0 can be determined as

$$Z_L = \frac{V_D - V_{bias} + I_D Z_0}{I_D}. \quad (2)$$

With s-parameters, the input reflection coefficient equation is defined as

$$\Gamma_{IN} = \frac{Z_L - Z_0}{Z_L + Z_0}. \quad (3)$$

By substituting the previously defined Z_L in (2), the input reflection coefficient of the diode branch can be defined as

$$\Gamma_{IN} = \frac{V_D - V_{bias}}{V_D - V_{bias} + 2I_D Z_0}. \quad (4)$$

The DAPD topology defined previously in Fig. 3 has two nonlinear branches, with separate bias voltages. These bias voltages are now termed as V_{Bn} , and each diode branch termed by D in D_n , where $n = 1, 2$ are the nonlinear branches. Based on the input reflection coefficient defined previously in (4), the magnitude transmission coefficient of the nonlinear diode branches can now be defined as

$$Dn_{|S21|} = 1 - \left| \frac{V_D - V_{Bn}}{V_D - V_{Bn} + 2I_D Z_0} \right|. \quad (5)$$

The transmission coefficient of each nonlinear branch can be represented as a complex quantity, accounting for the delay element associated with each branch, $Dn_{\angle S21}$

$$Dn_{S21} = Dn_{|S21|} \cdot [\cos(Dn_{\angle S21}) + j \sin(Dn_{\angle S21})]. \quad (6)$$

The linear path is assumed to be unattenuated, with transmission magnitude of 1, and a delay element of linear $\angle S21$, resulting in a linear transmission coefficient of

$$L_{S21} = \cos(L_{\angle S21}) + j \sin(L_{\angle S21}). \quad (7)$$

The overall complex transmission coefficient for the DAPD can then be calculated by combining the complex transmission coefficients of two nonlinear branches, in (6), with the complex transmission coefficient of a linear branch, in (7), whilst accounting for the power separation and combination in both the three-way splitter and combiner, $\approx 1/\sqrt{3}$, resulting in

$$DAPD_{S21} = \frac{D1_{S21} + D2_{S21} + L_{S21}}{3}. \quad (8)$$

Then finally, to obtain the overall phase and gain response of the DAPD, the following are defined:

$$DAPD_{gain} = 20 \log(|DAPD_{S21}|) \quad (9)$$

$$DAPD_{phase} = \tan^{-1} \left[\frac{\text{Re}(DAPD_{S21})}{\text{Im}(DAPD_{S21})} \right]. \quad (10)$$

C. DAPD Phase and Gain Characteristics

In this section, the previously provided mathematical analysis is used to examine typical gain and phase characteristics provided by the DAPD. First, a typical diode IV characteristic is calculated using the Shockley diode equation, which is close to that used by SPICE models, where the diode current is defined as

$$I_D = I_S (e^{(V_D/nV_T)-1}) \quad (11)$$

where I_S is the reverse-bias saturation current and n is the emission coefficient, which are 2×10^{-13} and 1.2, respectively, as supplied by MACOM for the MA4E1310 Schottky diode. V_D is the voltage across the diode, whilst V_T is the thermal voltage, defined as

$$V_T = \frac{kT}{q} \quad (12)$$

where k is the Boltzmann's constant, T is the junction temperature, and q is the charge of an electron.

The next step was to calculate a comprehensive array of DAPD configurations, to then find particular configurations which would provide the appropriate gain response. This gain response would need to have the ability to linearize carrier gain inflection within a DPA, where a gain expansion of ≈ 3 dB was targeted, whilst also providing a flat gain response after this expansion. These calculations were completed for various bias voltages, V_{B1} and V_{B2} , and delay line lengths for each branch, $D1^\circ$, $D2^\circ$, and Linear $^\circ$. To do so, the diode I_D characteristic is calculated using a specified V_D and (11). This is then used to find the complex transmission coefficient of each branch using (5) and (6) for each arrangement. The overall gain for each configuration was then calculated using (8) and (10).

The resulting gain and phase response from two specific configurations are highlighted in Fig. 5(a) and (b), where in each case the delay line lengths for each branch, $D1^\circ$, $D2^\circ$, and Linear $^\circ$, are fixed. In each case, the ability to shift the power level at which carrier PA gain compression can be linearized is demonstrated. This is achieved by changing the first branch voltage V_{B1} , whilst the delta between the two nonlinear branch voltages, V_{B1} and V_{B2} , is unchanged, therefore maintaining a gain expansion of ≈ 3 dB in each case. To change the value of gain expansion, the delta between the two nonlinear branch voltages can be changed. Two further configurations are highlighted in Fig. 5(c) and (d), where in each case the two nonlinear branch voltages, V_{B1} and V_{B2} , are fixed. In each case, the ability to shift the amount of phase correction that DAPD can achieve is demonstrated. In the example configurations, this is achieved by adjusting Linear $^\circ$ by 30 $^\circ$, whilst $D1^\circ$ and $D2^\circ$ are adjusted by 15 $^\circ$.

III. DESIGN PROCEDURE FOR DAPD

This section first outlines how the passive modeling of diodes, capacitors, and inductors was undertaken, before detailing the measurements taken of the candidate DPA, where ideal predistortion characteristics are extracted for the design of the DAPD. Finally, the design of the DAPD for the candidate DPA is detailed, by combining the derived passive models with target predistortion characteristics, along with optimization using Keysight's ADS simulation tool.

A. Passive Modeling

This section outlines the modeling activity which occurred during the design phase to enable an accurate design. The proposed DAPD architecture features no mechanism for phase adjustment in the final circuit, where other APDs such as [20] and [25] typically feature a digital phase shifter. This therefore places great importance on the accuracy of simulations, where the required delay line lengths are fixed during the design. The initial step undertaken in the design, therefore, was the full characterization of the passive devices to be used. This was conducted using thru-reflect-line (TRL) calibration between 1–15 GHz, on the design substrate Rogers 4350B

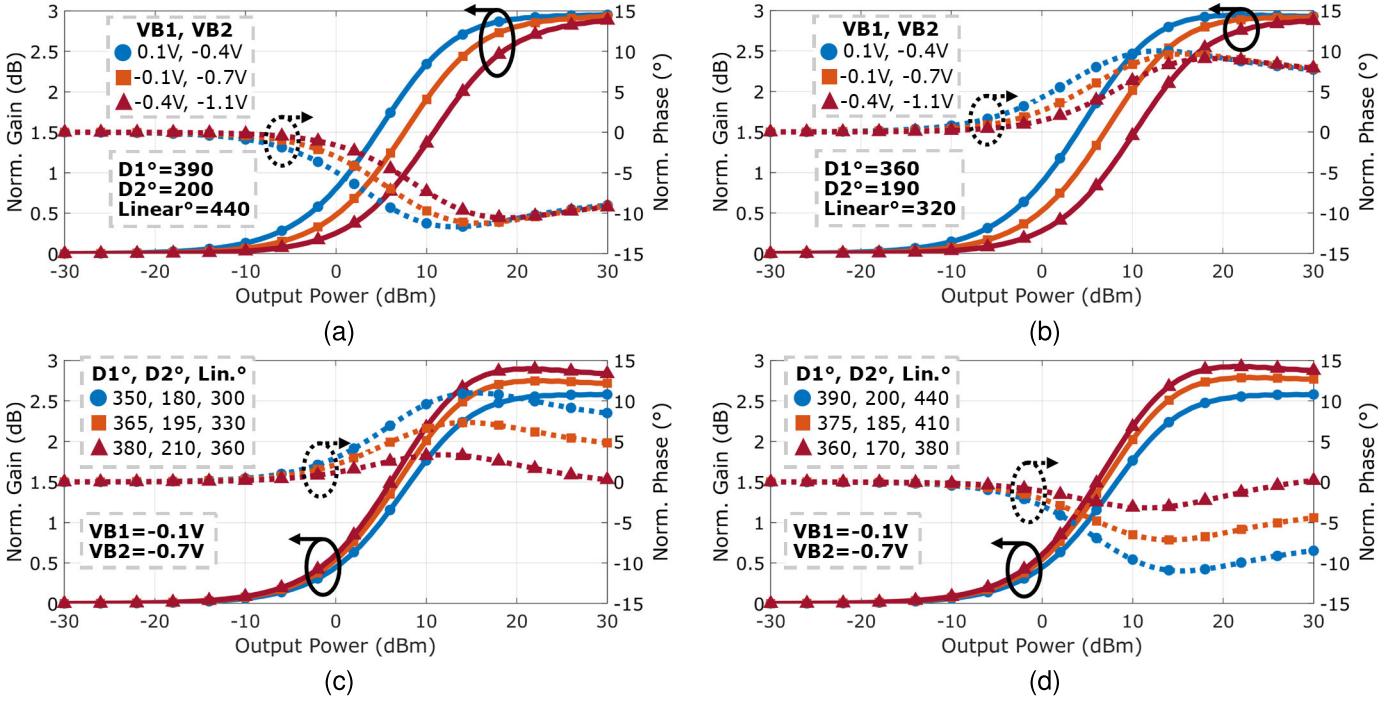


Fig. 5. Various configurations of the DAPD which provide the required gain response for DPA carrier gain inflection linearization. Both (a) and (b) demonstrate the ability to shift the power level at which the inflection can be linearized, using V_{B1} and V_{B2} . Demonstrated in (c) and (d) is the ability to shift the amount of phase correction that DAPD can achieve, through adjusting Linear $^\circ$, $D1^\circ$, and $D2^\circ$.

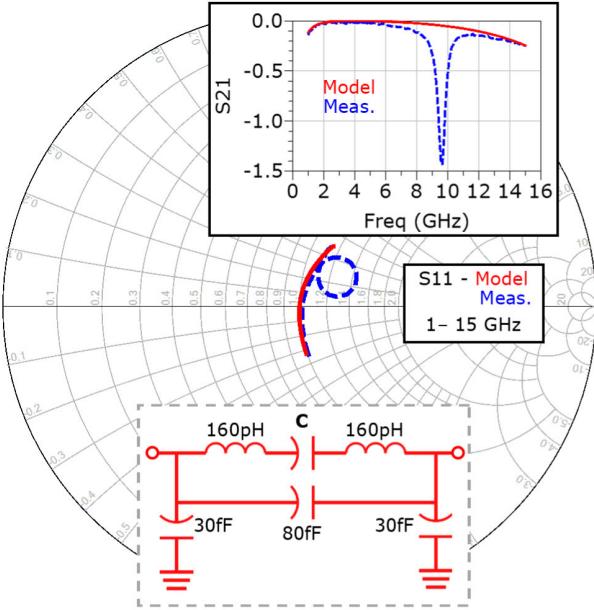


Fig. 6. 501R14S8R2 capacitor model versus measurements, where parasitic inductance and capacitances have been extracted in simulation to match model with measurements.

with 0.51 mm thickness. From these measurements, a model for the Schottky diode (MACOM MA4E1310), Johanson capacitors (R14S), and Murata inductors (LQP03HQ) were made.

The 501R14S8R2 8.2 pF capacitor which was to be used in the DAPD circuit as a block in the DC biasing of the diodes was first modeled. Measurements were conducted on multiple capacitors of this value to decouple capacitance and lead

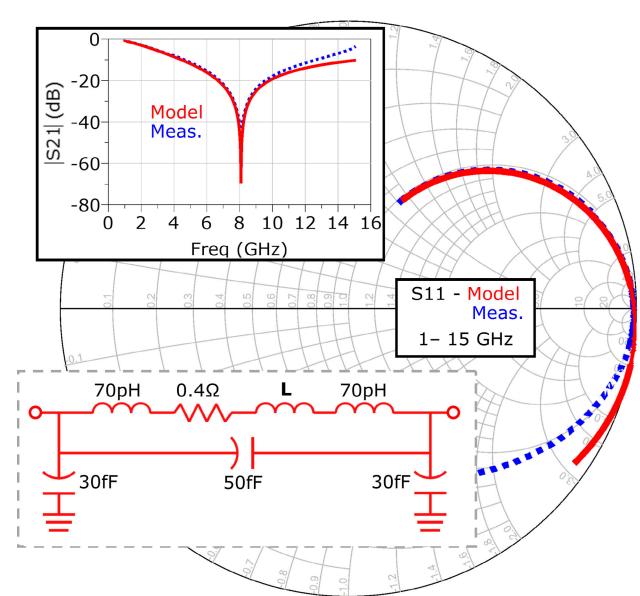


Fig. 7. LQP03HQ8N2 inductor model versus measurements, where parasitic inductance and capacitances have been extracted in simulation to match model with measurements.

inductance tolerance, whilst verifying component and mounting repeatability. A circuit model was fit to measurements in simulation using ADS, where the model consists of shunt extrinsic capacitance due to the substrate used, along with series inductance consisting of a combination of extrinsic and internal lead inductance. The resulting model, with parasitic inductance and capacitances, is shown by Fig. 6. The proposed model shows a good agreement to measurements.

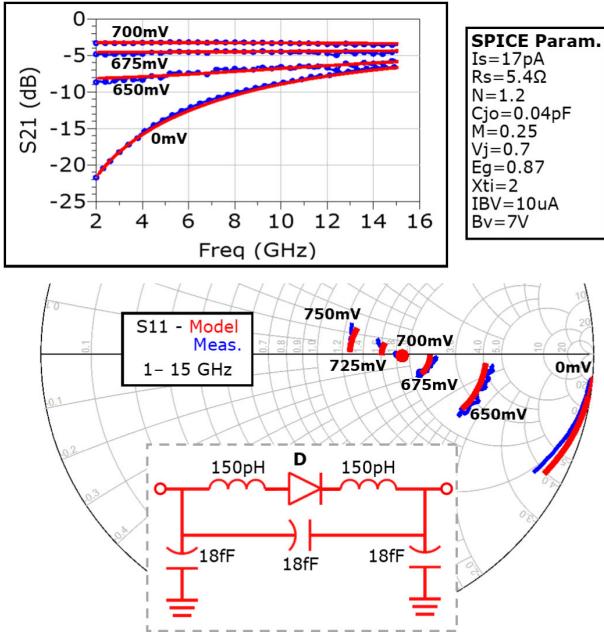


Fig. 8. MA4E1310 Schottky diode model versus measurements at various voltage bias points, along with SPICE parameters of diode. Parasitic inductance and capacitances have been extracted in simulation to match model with measurements.

Some resonance, however, does appear in the measurements at around 9 GHz which is not modeled. This resonance is possibly due to modes which can be excited within the substrate when using the Anritsu 3680 Series Universal Test Fixture. This is detailed within the manual of the test fixture, where within a low dielectric constant substrate, such as the one used, secondary modes can reach the edge boundaries and become resonant. Grounded metal planes were used on the TRL PCB test structures to dampen these modes, however, as seen by the measurements, not fully. The same process was repeated for the LQP03HQ8N2 8.2 nH inductor which was to be used as a feed in the DC biasing of the diodes, where multiple measurements were conducted and a model with the same parasitic inductance and capacitance elements were used. The model used for the LQP03HQ8N2 inductor is shown by Fig. 7.

The final step was to develop an accurate model for the MA4E1310 GaAs Schottky diode. Also using TRL calibration, measurements were conducted on the diode at various bias points, with zero bias at 0 V, and 25 mV steps from 650 to 750 mV. This allowed for the extraction of parasitic inductance and capacitance in simulation, where a circuit model was fit to measurements in simulation using ADS, consisting of the same parasitic elements as the capacitor model used previously. The measurements were also used for the extraction of the diode's reverse-bias saturation current I_S and ohmic resistance R_S SPICE parameters, which both impact the diode's forward voltage in simulation. The resulting model is shown in Fig. 8, along with its comparison with measurements at various bias voltages, and SPICE parameters used for the diode model. The choice of parasitic inductance and capacitances, along with SPICE parameters, has allowed for a model which shows a good agreement with measurements.

TABLE I
APD OPERATING VOLTAGES IN SIMULATION

Frequency (GHz)	2.2	2.3	2.4	2.5	2.6
V_{B1} (V)	-0.6	-0.56	-0.4	-0.45	-0.56
V_{B2} (V)	-1.68	-2.86	-2.48	-1.71	-2.58

B. DPA Characterization

This section outlines the characterization activity which was undertaken during the design phase, where a set of measurements were used to design the DAPD circuit in simulation. Before focusing on the design, the candidate DPA to be linearized [27] was fully characterized. This DPA operates between 2.1–3.2 GHz, with a power output of between 43.9–44.5 dBm, with asymmetrical operation resulting in a back-off level of 9 dB. A frequency range of 2.2–2.6 GHz was chosen for the design of the APD.

To characterize the DPA, a National Instruments (NI) Vector Signal Transceiver (VST), PXIe-5646, was used, featuring 200 MHz bandwidth with a maximum center frequency of 6 GHz. A driver (ZHL-16W-43) is used to provide the required 34 dBm input power into the DPA. During the measurement of the DPA, the carrier amplifier is supplied with a drain voltage of 18 V, with a gate voltage supplied for a quiescent current of 40 mA. The peaking amplifier is supplied with a drain voltage of 32 V and a gate voltage of -6.4 V. The DPA was characterized using Gaussian pulse measurements to excite the full output power range of the DPA, conducted at 100 MHz steps. At each frequency step, a simple memoryless polynomial DPD was calculated by comparing the input and output pulse signals. The resulting gain and phase difference between the original input signal, and the calculated DPD input signal were then determined. These gain and phase responses would then form the ideal predistortion characteristics used for the design of the DAPD. These ideal responses are shown in blue by the plots demonstrated in Fig. 9.

C. DAPD Design

The final step was the design of the DAPD for the candidate DPA using Keysight's ADS simulation tool. This design was accomplished by combining the theoretical analysis provided in Section II, along with the passive models developed in Section III-A, and the ideal measured predistortion characteristics of the candidate DPA defined in Section III-B. Initially, the target DPA predistortion characteristics were combined with the theory presented in Section II, within MATLAB to find the best starting configuration for simulations. The optimum configuration had the circuit parameters of $V_{B1} = -0.5$ V, $V_{B2} = -1.6$ V, $D1^\circ = 20$, $D2^\circ = 170$, and $\text{Linear}^\circ = 420$, with a linear gain of 20 dB. The next step in the design was the EM simulation of the input splitter and output combiner, where a cascade of two Wilkinson power splitters were used to provide an equal three-way split, along with the appropriate isolation. A LSSP simulation is then used within ADS using the initial optimum configuration, along with passive models, the EM simulated input splitter and output combiner, and ideal transmission lines for each

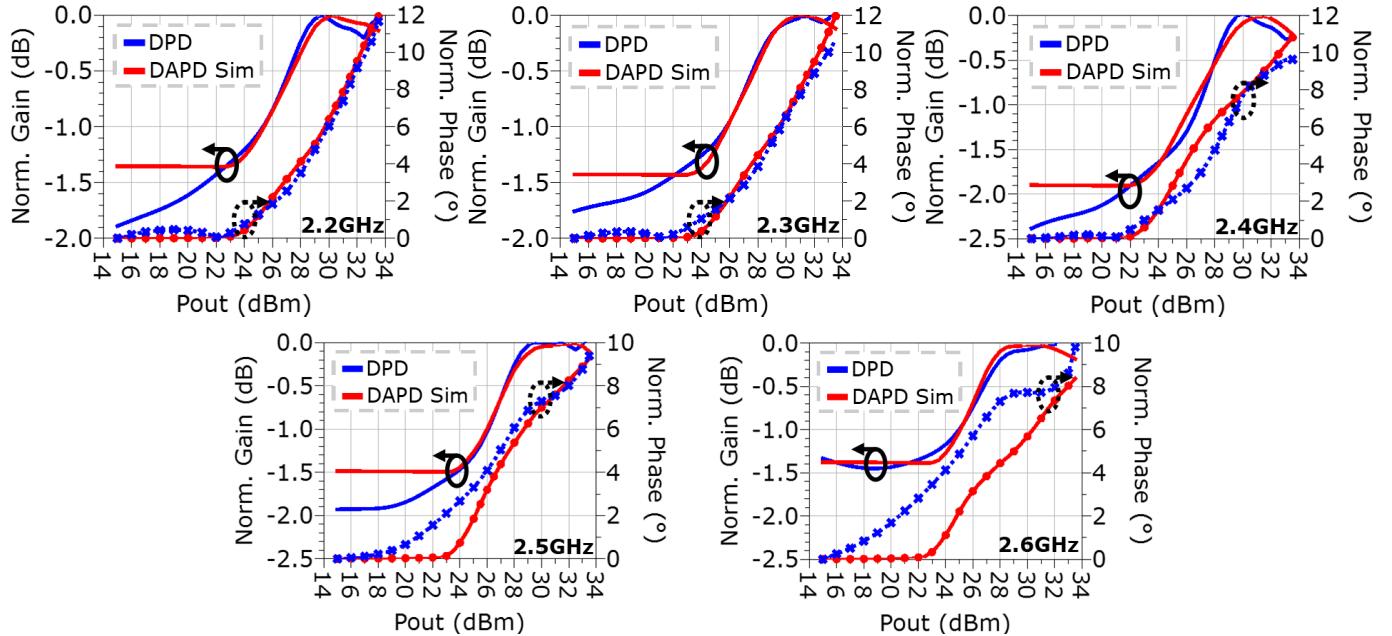


Fig. 9. Simulated DAPD versus measured ideal DPD gain and phase responses. The calculated DPD ideal predistortion characteristics were calculated using measurements of the candidate DPA. The simulated DAPD responses are of the final EM simulated layout using a LSSP simulation.

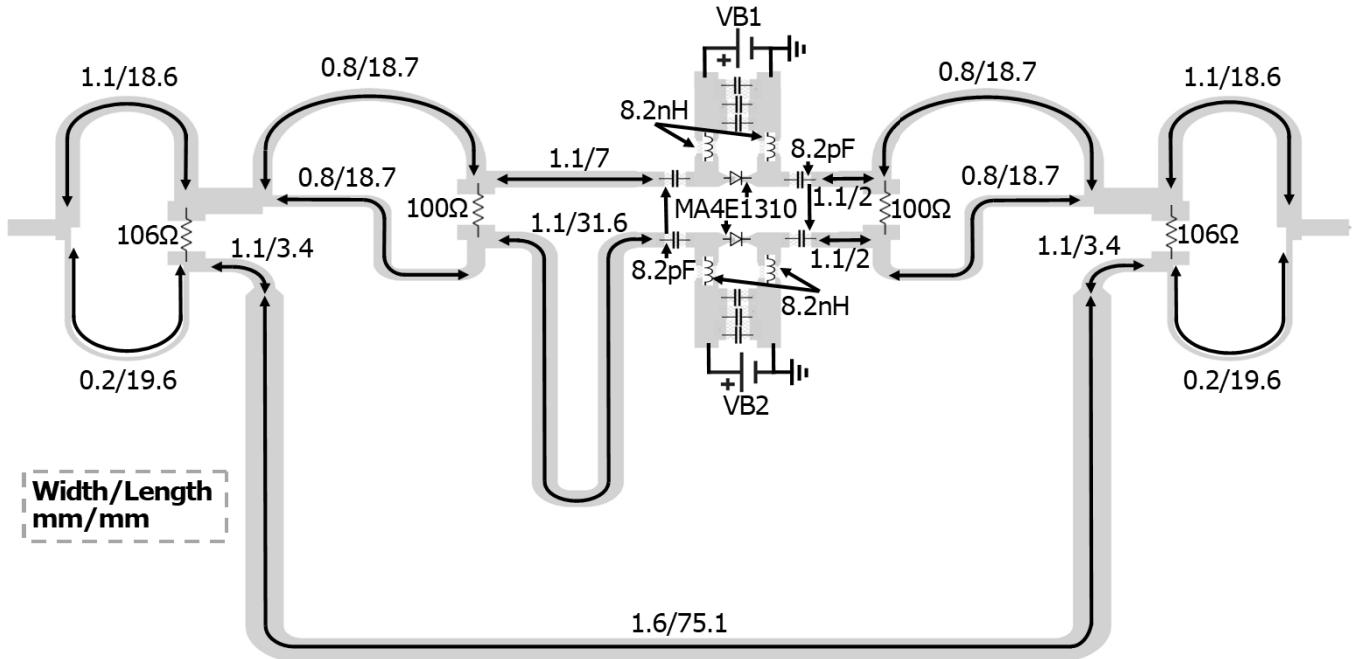


Fig. 10. Final EM simulated layout of the DAPD on Rogers 4350B substrate with 0.51 mm thickness, where passive DC blocks of 8.2 pF have been highlighted, along with passive DC feeds of 8.2 nH.

required branch delay line. Optimization is then used to further tune these ideal transmission line delay lengths, and also both bias voltages for each frequency, to further match the ideal predistortion characteristics. The resulting gain and phase response from a LSSP simulation of the final EM simulated DAPD is shown in Fig. 9, with the final EM simulated layout shown in Fig. 10, whilst the operating voltages used are shown in Table I. These results show good agreement with the gain and phase responses specified by DPD.

IV. EXPERIMENTAL RESULTS

This section outlines the experimental results of the work, where the combination of the manufactured DAPD and the candidate DPA were measured, using Gaussian pulse, continuous wave, 5G modulated, and two-tone signals.

A. Gaussian Pulse Measurements

The first measurements taken of the DAPD were Gaussian pulse signal measurements. The full details of the Gaussian

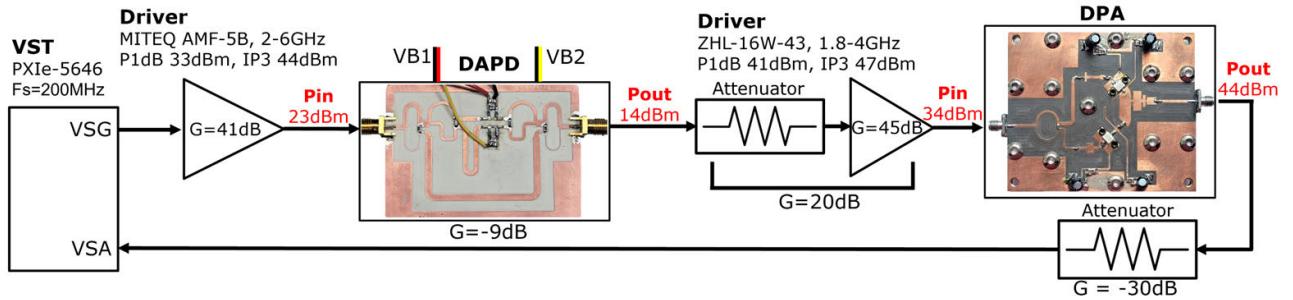


Fig. 11. Gaussian pulse and modulated signal test setup, featuring an NI VST, two high IP3 drivers, and attenuators. The first driver is used to drive the APD with 23 dBm, whilst the second driver is used with attenuator to provide 20 dB of gain, and a power of 34 dBm to drive the DPA. The input powers supplied in red are the maximum saturated power levels upon which any normalized input Gaussian or modulated signal are relative to.

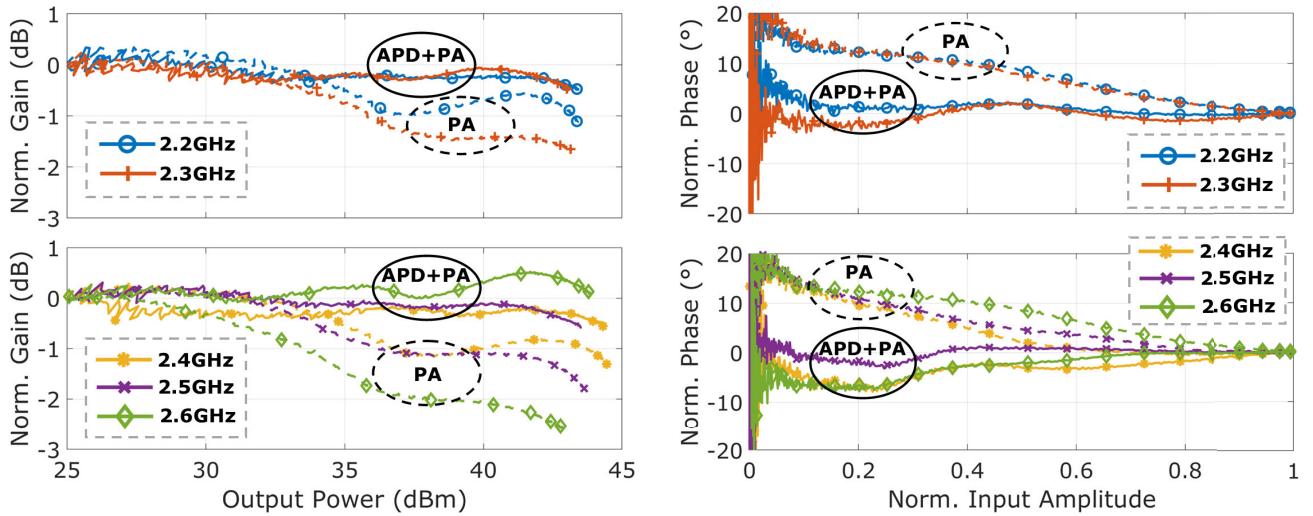


Fig. 12. Normalized gain and phase plots from Gaussian pulse measurements of the DPA, with and without DAPD, demonstrated at all frequencies ranging 2.2–2.6 GHz. Measurements of the DPA are shown in dotted lines, whilst the combination of the DAPD with DPA are shown with solid lines. These plots show the DAPD's ability to linearize both the gain and phase of the DPA, where gain is linearized to within an error of 0.2–0.5 dB, whilst the phase is linearized to within an error of 2°–7°.

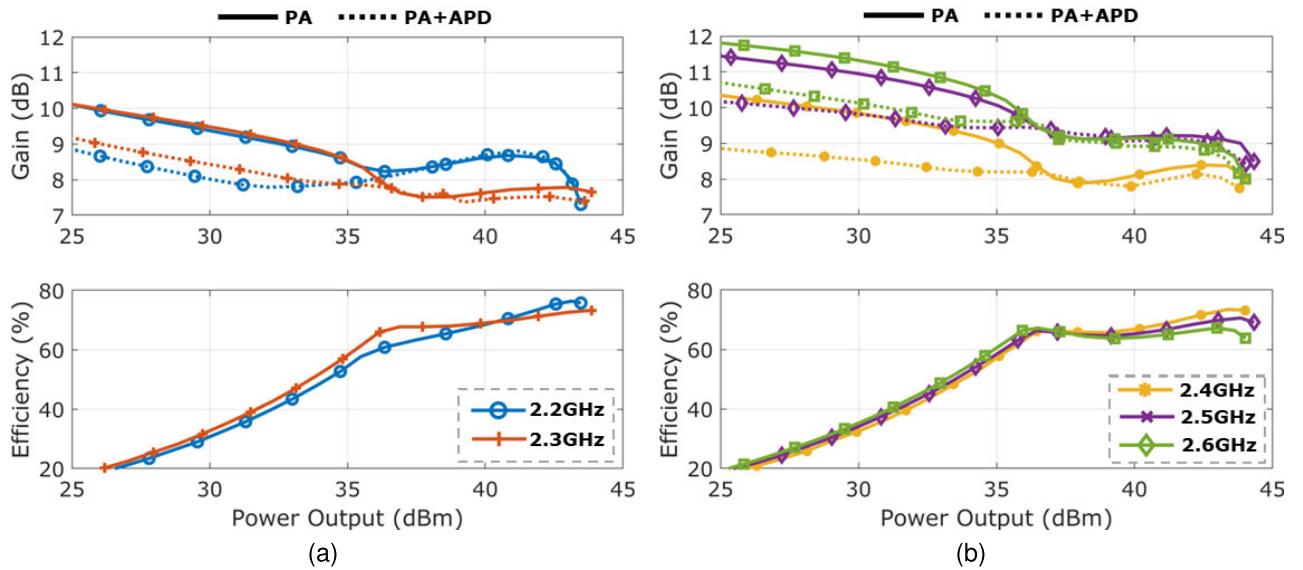


Fig. 13. Continuous wave measurements of the DPA featuring gain, with and without DPA, for 2.2 to 2.3 GHz (a), and for 2.4 to 2.6 GHz (b). For drain efficiency plots, the same efficiency is achieved with and without DAPD, where no power is consumed from the DAPD.

pulse used can be found in [28], where here a pulselength of 4 μ s is used. An overview of the Gaussian pulse and modulated

signal test setup is shown in Fig. 11. As with the characterization activity outlined in Section III-B, an NI VST is used for

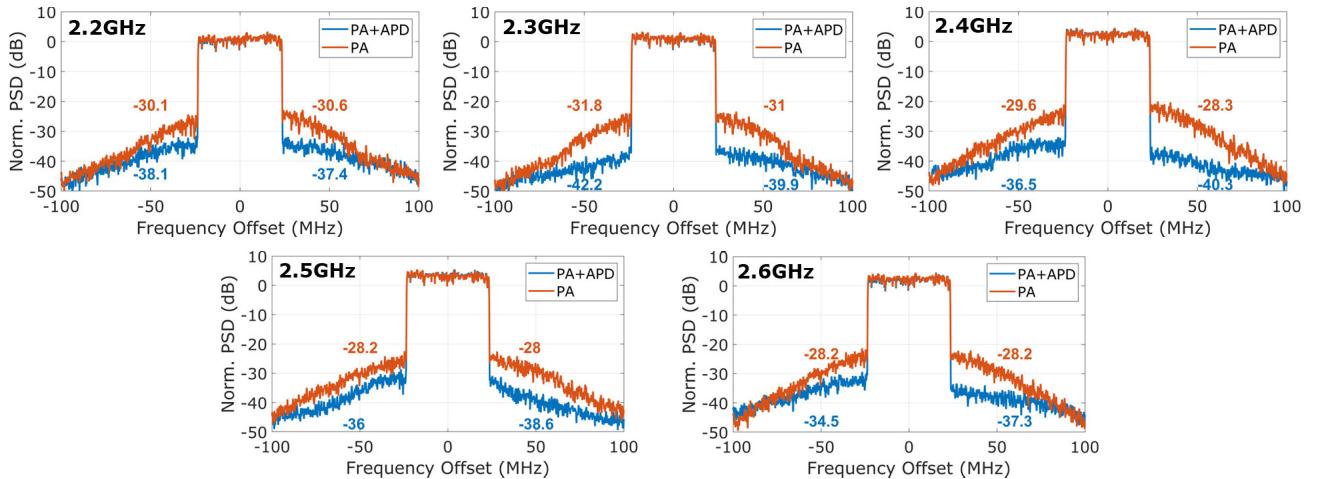


Fig. 14. Power spectrum density measurements of the DPA with and without DAPD, using a 50 MHz 5G downlink signal with a PAPR of 10 dB, with an average output power of between 33.2–35 dBm. Values shown on plots are the average power of the adjacent channel, where an average ACPR improvement of between 7.3–9.6 dB is observed over all frequencies.

modulated signal testing. To ensure linearity with the VST, a driver (MITEQ AMF-5B) is used to provide the required 23 dBm into the input of the APD. The insertion loss of the DAPD is 9 dB, therefore requiring a second driver (ZHL-16W-43) to provide the required 34 dBm input power into the DPA. The test setup was tested for linearity, where very minimal phase and amplitude distortion was observed when using both drivers. Both drivers present good linearity performance, with both featuring a high third-order intercept point. The same biasing is used for the DPA as used during characterization, where the carrier amplifier is supplied with a drain voltage of 18 V, with a gate voltage supplied for a quiescent current of 40 mA. The peaking amplifier is supplied with a drain voltage of 32 V and a gate voltage of -6.4 V. To obtain the optimum bias voltages, the linearizer was first characterized over a full power range using Gaussian pulse measurements, for frequency steps of 100 MHz between 2.2–2.6 GHz, at varying DAPD bias voltages, V_{B1} and V_{B2} . These measurements are then compared with the optimum DPD characteristics of the DPA to find the optimum bias voltages for each frequency. The resulting optimum bias voltages are shown by Table II.

The next measurements taken were the combination of the DAPD with the candidate DPA using Gaussian pulse measurements. The measurement results for testing the DPA, with and without the linearizer are shown by Fig. 12, showing both normalized gain and phase measurements. The DAPD has no ability to correct memory present within the DPA, so to observe the absolute amplitude and phase correction the DAPD provides, a mean of the rising and falling power edges of the pulse are taken to remove memory. These results show the DAPD's ability to linearize both the gain and phase of the DPA, where gain is linearized to within an error of 0.2–0.5 dB, whilst the phase is linearized to within an error of 2° – 7° .

B. Continuous Wave Measurements

To further verify the combination of DAPD with the candidate DPA, and to observe any potential power consumption from the DAPD, measurements were taken using a continuous

TABLE II
APD OPERATING VOLTAGES AND ACPR CORRECTION
VERSUS FREQUENCY

Frequency (GHz)	2.2	2.3	2.4	2.5	2.6
V_{B1} (V)	-0.6	-0.6	-0.7	-0.35	-0.45
V_{B2} (V)	-1.7	-3.2	-2.8	-1.7	-3.3
ACPR PA (dBc)	-31.6	-32.8	-31.4	-31.3	-30.8
ACPR PA+APD (dBc)	-38.1	-41.2	-41	-40.2	-38.6
ACPR Correction (dB)	7.3	9.6	9.5	9.1	7.7

wave signal. For these measurements, Rohde and Schwarz NRP40P pulse power sensors were used to measure both input and output power. A pulsed continuous wave signal of 10% duty cycle and 1 μ s pulselength was used. The results for these measurements are demonstrated in Fig. 13. The gain plots verify the results shown previously with Gaussian pulse measurements, where the ability of DAPD to linearize carrier gain is demonstrated. The drain efficiency of the DPA is also shown in Fig. 13, where the same efficiency is achieved with and without DAPD, where no DC power is consumed by the DAPD.

During these measurements, no current draw was observed from the DC supply for the DAPD. For further verification, this was also observed with a second measurement using a high pulselength of 5 s to negate any averaging occurring within the DC power supply. Current flow was observed through a multimeter connected between the DC supply and the DAPD, around 1–10 mA, however, this can be attributed to being a small amount of RF rectified DC generation through the diode.

C. Modulated Signal Measurements

The combination of DAPD and DPA was then further verified using modulated signal measurements. The first modulated signal measurements were taken using a 50 MHz 5G NR downlink signal, generated for testing using MATLAB's 5G waveform generator. This waveform featured a PAPR of 10 dB, where an average output power of between 33.2–35 dBm was observed from the DPA. The power spectrum results for testing the DPA, with and without DAPD, are

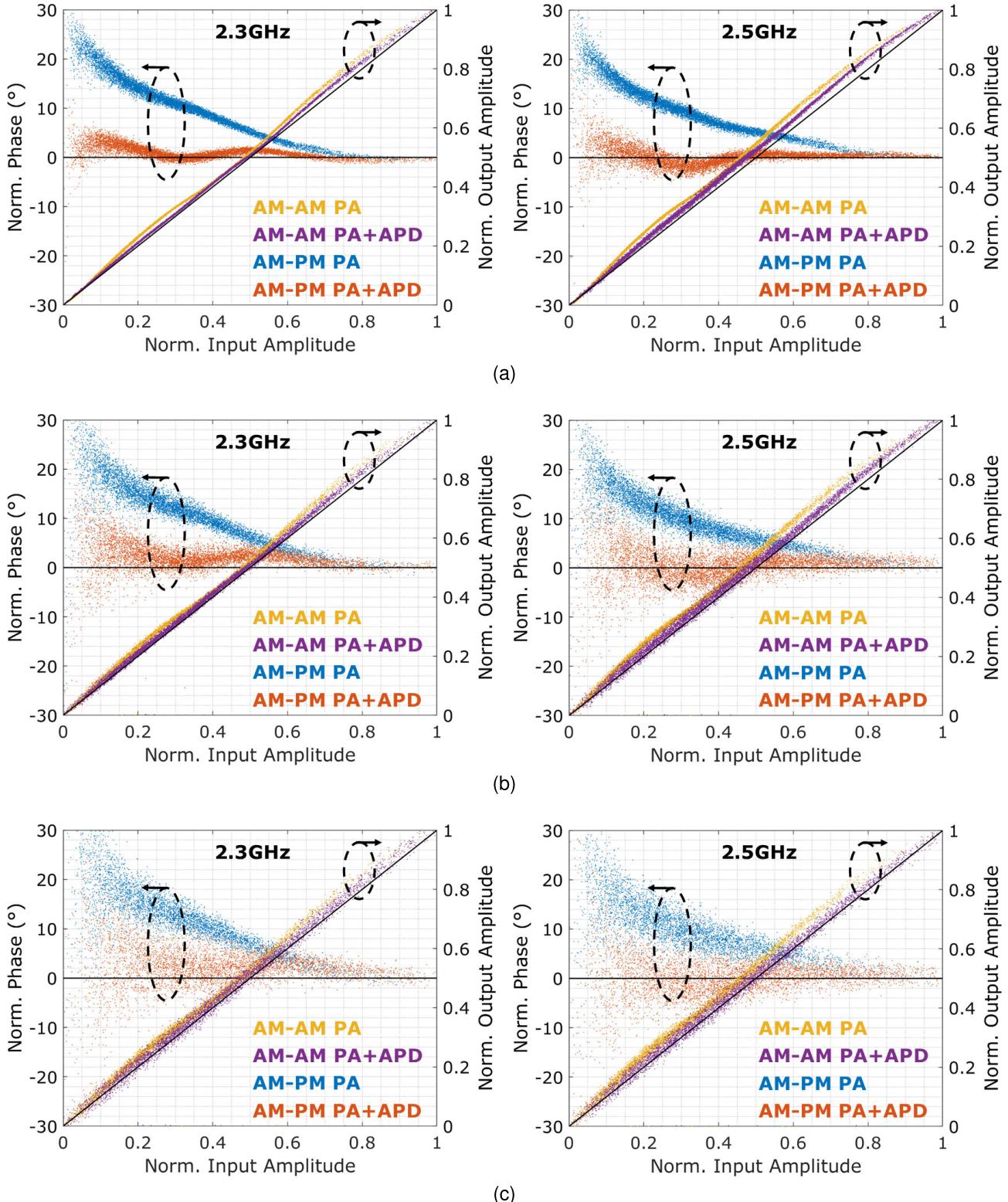


Fig. 15. AM-AM and AM-PM plots based on the measurements of the combination of DPA and DAPD using a modulated signal, with a PAPR of 10 dB, at 2.3 and 2.5 GHz, with a bandwidth of 20 MHz (a), 50 MHz (b), and 80 MHz (c). The plots show the correction of both amplitude and phase for a modulated signal.

shown by Fig. 14, where amplitude-to-amplitude modulation (AM-AM) and amplitude-to-phase modulation (AM-PM) are shown by Fig. 15. These measurements show a reduction in ACPR when using the DAPD linearizer for all frequencies,

demonstrating a reduction in ACPR of 7.3–9.6 dB, as reported in Table II. The measurements also further demonstrate the correction of both amplitude and phase with both AM-AM and AM-PM plots.

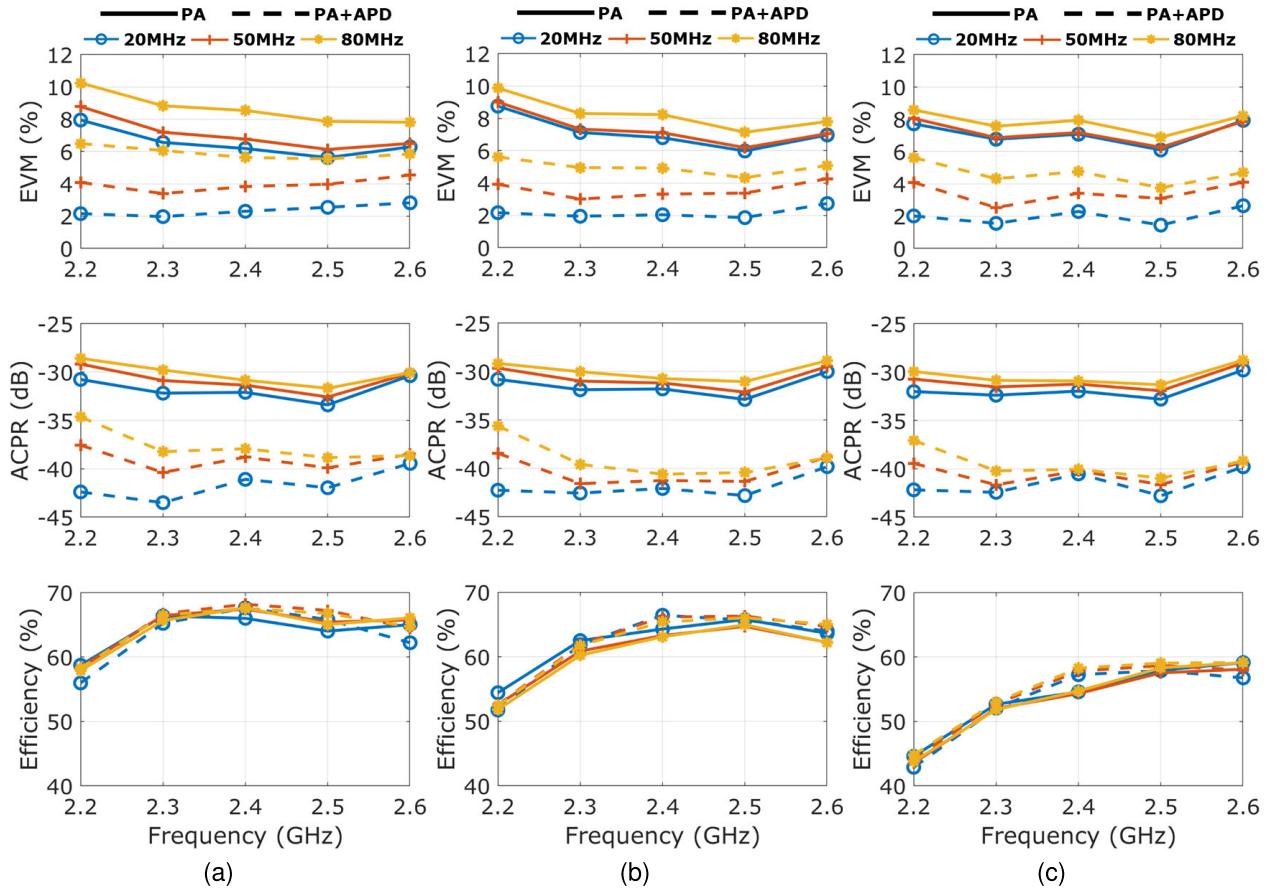


Fig. 16. EVM, ACPR, and drain efficiency measurements from OFDM modulated signal tests, featuring different channel bandwidths of 20, 50, and 80 MHz, with different PAPRs of (a) 8.6, (b) 10, and (c) 11.6 dB. The combination of DPA and DAPD results in a reduction in both EVM and ACPR for all channel bandwidths and PAPRs. A maximum bandwidth of 80 MHz is tested due to a limitation in available instrumentation.

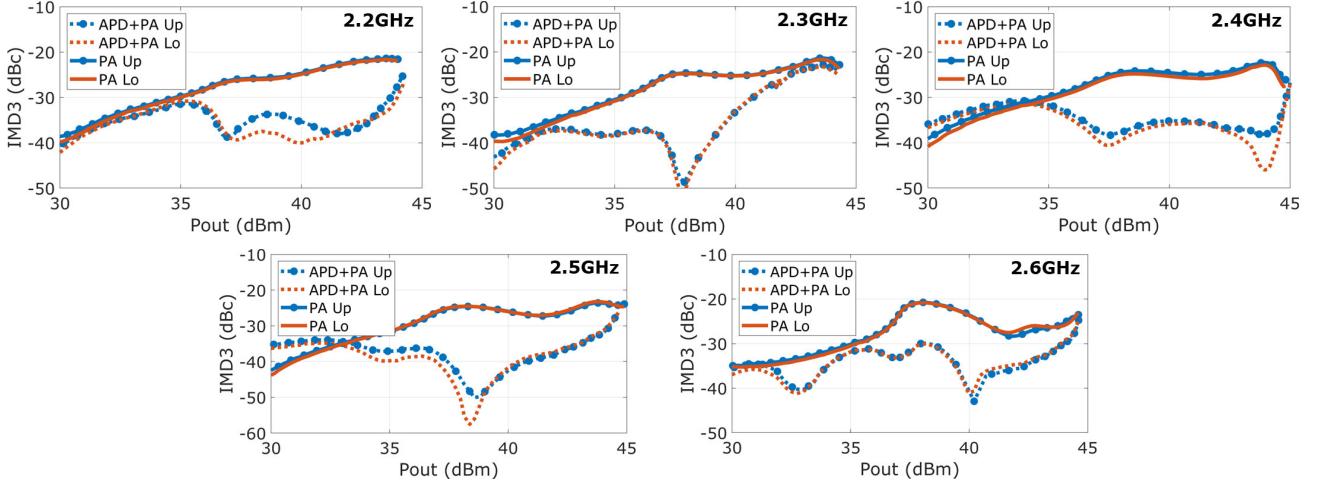


Fig. 17. Third-order intermodulation plots from two-tone signal measurements of the DPA, with and without DAPD, demonstrated at all frequencies ranging 2.2–2.6 GHz. Lo and Up represent the lower and upper third order intermodulation products, respectively. The plots demonstrate the DAPD's ability to reduce IMD3 in the higher power range of the DPA's output power, where maximum corrections of between 15–20 dB are observed, over the frequency range of 2.2–2.6 GHz.

Further modulated signal measurements were then conducted using 16 quadrature amplitude modulation with OFDM. The OFDM subcarrier spacing and number of subcarriers were varied to produce waveforms with different channel bandwidths of 20, 50, and 80 MHz, and with different PAPRs of 8.6, 10, and 11.6 dB. The measurement results for testing

each combination of channel bandwidth and PAPR with the DPA, with and without DAPD, are shown in Fig. 16. With the combination of DPA and DAPD, EVM is reduced to an absolute value of 1.4%–2.8% for a 20 MHz channel bandwidth, 2.5%–4.5% for a 50 MHz channel bandwidth, and 3.8%–6.4% for a 80 MHz channel bandwidth. ACPR

TABLE III
COMPARISON OF GaN-BASED LINEAR DPA DESIGNS

Ref.	Topology	Frequency (GHz)	Instantaneous Bandwidth (MHz)	PAPR (dB)	Avg. Pout (dBm)	Avg. PA DE (%)	ACPR w. no DPD (dBC)	EVM (%)	Linearizer ACPR Correction (dB)	Bandwidth (MHz)
This Work	DAPD	2.3	50	10	35.3	61.7	-41.2	3.1	9.6	400
[9]	Linear DPA Design	2.14	20	8.6	33.9	44	-40.5	NR	N/A	Narrow-band
[10]	Linear DPA Design	5	40	7.4	32	42	-43.8	NR	N/A	500
[11]	Linear DPA Design	3.2	100	6	37	42.2	-43	2.2	N/A	500
[24]	Linearization Amplifier	0.8	40	8.3	33	44	-40.7	3.9	11.8	150
[25]	Tunable Linearizer	3.5	20	7	37	46	-44.9	NR	12.6	200

is reduced to an absolute value of -39.4 to -43.5 dBc for a 20 MHz channel bandwidth, -37.5 to -41.2 dBc for a 50 MHz channel bandwidth and -34.6 to -40.9 dBc for a 80 MHz channel bandwidth. A slight difference of efficiency is observed, though this can be attributed to a change in average operating power from a small difference in input power.

D. Two-Tone Measurements

The final set of measurements taken of the DPA, and its combination with the DAPD linearizer, were two-tone signal measurements. The same test setup as before in Fig. 11 is used, however, a Keysight E8267D VSG with two-tone generation functionality is used in place of the VST, along with a R&S FSW spectrum analyzer to measure IQ samples from the DPA output. The two-tone measurement is conducted at power steps of 0.1 dB, up to the maximum input power of 34 dBm, with a spacing of 20 MHz between both tones. Output power is then observed, along with the relative power level of the lower and upper third-order intermodulation products. The results of these two-tone measurements are shown by Fig. 17. The plots demonstrate the DAPD's ability to reduce IMD3 in the higher power range of the DPA's output power, where maximum corrections of between 15–20 dB are observed, over the frequency range of 2.2–2.6 GHz.

E. Comparison With State-of-the-Art

Finally, this work is compared with the state-of-the-art, where Table III summarizes the performance of the proposed combination of DAPD with DPA alongside results from literature reported GaN-based linear DPAs. There are two literature examples of a DPA linearizer in [24] and [25]. However, within both of these works, there is an increased power consumption from the linearizers used, where [24] features an active linearizer which can reduce the efficiency of the PA by 20%. The work within [25] features multiple variable gain amplifiers, a phase shifter, and microcontrol unit, which consumes 1 W. The work presented is purely a passive solution and has advantages in consuming no DC power. This work also achieves a higher operating and instantaneous bandwidth than [24] and [25].

The other works, [9], [10], [11], feature a DPA which is designed to be inherently linear, where this work achieves a comparable ACPR. However, these linear DPA solutions achieve their linearity through limited carrier compression, which can reduce the efficiency of these solutions when comparing with this work. Due to the use of a candidate DPA that is highly efficient through the use of continuous modes [27], a higher average back-off drain efficiency is achieved. The use of DAPD with a highly efficient DPA shows that around 15%–19% higher drain efficiency than the state-of-the-art can be achieved, whilst still achieving comparable ACPR performance.

V. CONCLUSION

This work has demonstrated a novel tri-branch DAPD for Doherty power amplifiers (DPAs). A thorough analysis of this new topology was provided, where the overall gain and phase characteristics of the circuit were mathematically defined. Also through analysis, various configurations of the topology were provided, demonstrating the topologies ability to accurately predistort the gain and phase nonlinearity associated with carrier compression within a DPA. An accurate DAPD design was then detailed, accomplished by combining the provided theoretical analysis with passive modeling, and ideal measured predistortion characteristics of the candidate DPA. Measurements were provided, where a correction of ACPR of between 7.3–9.6 dB over a bandwidth of 2.2–2.6 GHz was demonstrated, when considering a 50 MHz 5G NR modulated signal. There are multiple areas for further work with this new topology, including the co-design of the DAPD with a DPA for more favorable gain and phase characteristics, the implementation of DAPD alongside DPD, and also the implementation of this topology at FR2 frequencies, where aggregated bandwidths make the implementation of DPD difficult, and ACPR restrictions are less demanding.

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