

A Digitally Controlled Analog Predistortion Linearizer for the Correction of Deep and Shallow Class-AB RF Power Amplifiers

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Abstract—This article presents a digitally controlled dual-branch dual-transistor analog predistortion (APD) for the linearization of RF power amplifiers (PAs). This APD is capable of complementing the gain expansion and compression of deep class-AB PAs (also known as “gain peaking”). This APD is based on a dual-branch architecture with a main and peaking amplifier connected to an isolated combiner. Bipolar transistors and emitter degeneration techniques are adopted to match the APD profile to the PA gain and phase trajectory. Amplifier stability is analyzed over the APD tuning range, and the design parameters are optimized to achieve optimum fit with PA trajectories over the bandwidth. The APD is first evaluated in dual-input mode for the augmented testing range. Using Gaussian pulses, the APD optimal settings are found for a variety of frequencies and powers. Measured results demonstrate the ability of the APD to compensate for a wide range of biases with an independent amplitude and phase control. When combined with a PA with low bias current, a gain ripple of ± 0.3 dB and phase variation of $\pm 3^\circ$ are observed. The APD is then converted to a single-input/single-output block for testing in a realistic base-station environment. Using the standard-compliant waveform analysis software, the APD is demonstrated with 5G downlink 100-MHz signals between 1.8 and 2.2 GHz, attaining an adjacent channel leakage ratio (ACLR) of less than -46.1 – -46.6 dBc, an error vector magnitude (EVM) of 0.8%, and a remarkably low power consumption of only 18 mW.

Index Terms—Analog linearization, analog predistortion (APD), multibias APD, RF power amplifier (PA).

I. INTRODUCTION

THE push toward higher and higher data rates in 5G networks is driving the need for significantly wider signal bandwidths—up to 100 MHz in the sub-7.125-GHz range and 400 MHz in the mm-wave spectrum. Meeting these requirements poses increasing challenges for the RF transmitters, particularly in terms of linearity, output power, and efficiency. The limiting component is usually the RF power amplifier (PA), which causes in- and out-of-band spectral regrowth, deteriorates error vector magnitude (EVM), and causes channel interference. High-capacity communication links, such as those found in 5G deployments, typically use

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constellation-dense modulations with orthogonal frequency division multiplexing (OFDM) schemes. However, these modulations generate signals with probability density functions (pdfs) that are densely located in the PA back-off region.

Digital predistortion (DPD) is a well-known technique used to improve the PA linearity. DPD allows for the correction of nonlinear dynamic effects with high accuracy over tenth-of-MHz bandwidths [1], [2]. Although DPD provides high flexibility and linearity, these come at the cost of expensive and power-hungry hardware. The typical DPD bandwidth expansion of 4–5× the signal bandwidth requires the adoption of high-throughput signal processors, fast digital-to-analog converters, and wideband RF upconverters [3]. As discussed in [4], the dynamic power consumption of a DPD on a field-programmable gate array (FPGA) increases linearly with the clock frequency and the memory order. Regarding the digital-to-analog converter, for example, the Analog Devices AD9176 consumes 2.77 W when operating at 12 GBPS. However, this power consumption decreases to 1.34 W when the sampling rate is 4 GBPS [5]. DPD also requires wideband upconverters, drivers, and PAs, which will further increase the overall transmitter size, weight, power, and cost (SWaP-C).

Analog predistortion (APD) is a long-established technique that is now being revived to decrease the consumption and hardware complexity of RF transmitters. The primary advantage of APD is in its inherent simplicity: the PA nonlinear correction can be directly implemented in the RF signal path, either with a hybrid or an integrated circuit. APD relaxes the computational burden on the digital baseband, as this can now operate at the original sampling frequency. The bandwidth expansion is offloaded to the RF domain, where large-signal bandwidths can be easily managed by RF circuitry, possibly leveraging high-figure-of-merit III-V semiconductor compounds for enhanced performance.

APD architectures typically employ single, double, or triple nonlinearities on a single, double, or multiple branches. Single-branch APDs provide AM/AM correction but have no control over the phase distortion, which can either rotate in a favorable direction or not, depending on the nonlinearity. For example, a diode-based APD was used to linearize a 28-GHz PA, improving the 1-dB compression point by 1.5 dB and achieving a power-added efficiency (PAE) of 26% [6]. Recently, two similar papers [7], [8] presented a single-branch double-diode APD that achieved an adjacent channel leakage ratio (ACLR) of -45 – -44 dBc for a narrowband Doherty PA at 3.6 GHz. In

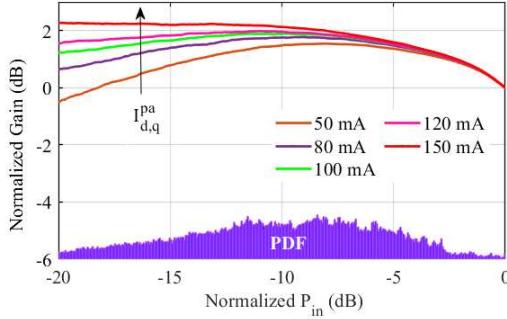


Fig. 1. Gain characteristics of a PA biased in deep and shallow class-AB. At low bias currents, as usually employed in high-efficiency switching PAs [25], the gain exhibits a “hump” that degrades linearity over a large output power range, as evidenced by the amplitude histogram of a 10-dB PAPR signal.

[9], a single-branch predistortion circuit with passive tuning elements improves the 1-dB output compression point from 35.2 to 38.9 dBm, while increasing efficiency by 8.5%.

Dual-branch APDs can independently control the AM/AM and AM/PM, with various degrees of tunability range. In [10], a transistor-based APD demonstrated 10-dB improvements in the third-order intermodulation distortion at 2.4 GHz. In [11], a Schottky diode APD achieved 5.9-dB gain expansion and 26.5° phase variation between 92.5 and 97.5 GHz. In [12], an integrated reflector-based APD operating at Ku-band achieved a maximum gain expansion and phase variation of 9 dB and 50°, respectively. In [13], a dual-branch APD based on tunable diodes with independent control of gain and phase achieved 11–22-dB improvement in the third-order intermodulation distortion at 27–31 GHz. In [14] and [15], a dual-branch single-diode APD for K-band PAs showed improvements in the noise-power ratio by 8.5 dB for a 750-MHz signal at 19 GHz. This APD was also used to analyze the output power and efficiency improvements for the same PA linearity in [16]. In [17], a dual-branch APD was able to improve the ACLR by 7–13 dB of a class-AB GaN PA with 1-MHz modulated signal at a central frequency of 1.7 GHz. A dual-branch dual-diode APD was introduced for correcting a Doherty PA with a 100-MHz signal bandwidth at a central frequency of 3.4 GHz in [18]. In [19], a Doherty PA was used as a predistortion circuit, which is architecturally similar to the proposed approach. As it will be later shown, this APD employs an isolated combiner to achieve independent AM/AM and AM/PM tuning and wideband response, similar to a sequential amplifier.

Finally, triple-branch APDs inherit the same independent amplitude and phase tunability of dual-branch APDs but can use an extra branch for increased tunability. This concept was exploited in [20] to compensate for the gain inflection of Doherty PAs [21], [22]. This resulted in ACLRs of –40.9/–43.5 dBc with 80-MHz signals between 2.2 and 2.6 GHz.

In theory, for a bias point in class-A, the peak efficiency is 50%, but this efficiency drops to 5% at 10-dB back-off [23]. When, instead, the bias point is chosen near the threshold, i.e., in class-B, the peak efficiency increases from 50% to 78.5% and the 10-dB back-off efficiency improves considerably, i.e., from 5% to 27%, but the back-off gain and maximum output

power are reduced [23]. For these reasons, class-AB PAs are the most utilized ones, with biases spanning from shallow to deep class-AB, depending on the targeted efficiency, gain, and power. This gives rise to a variety of gain profiles as the ones shown in Fig. 1. In GaN, this expanding and compressing behavior is also exacerbated by the device’s electron-trapped charges that modulate the back-off gain [24]. Superposed to Fig. 1, the amplitude histogram of a 10-dB peak-to-average power ratio (PAPR) OFDM signal is also shown. Notably, the signal average is located in correspondence of the gain “hump” or “peaking” point. This “hump” can be easily corrected with a DPD algorithm; a solution with analog techniques is yet to be found, and this is the focus of this article.

This manuscript presents a digitally controlled APD circuit that can correct both shallow and deep class-AB PAs, also exhibiting the gain “peaking” phenomenon. This APD is designed to operate at L-/S-band and uses two nonlinear branches (instead of the typical linear + nonlinear branch) implemented as amplifiers. The main amplifier¹ nonlinearity is biased in class-AB, while the peaking amplifier nonlinearity operates in class-C. The main amplifier is used to correct for the PA gain expansion, and the peaking amplifier corrects for the PA gain compression. A source degeneration resistor in the main amplifier is used to widen the APD gain “valley” and match this with the width of the PA gain “hump.” This APD can be adapted to a wide range of PA biases over a 400-MHz bandwidth by tuning the APD base/collector voltages through a splitter with amplitude and phase control.

This article is organized as follows. Section II presents the theory at the basis of the proposed APD. This model can predict the APD behavior for a variety of bias conditions and highlight different tuning strategies. Section III describes the design and simulation of the APD circuit using measured PA characteristics as a target nonlinearity. An optimization method is then used to rapidly find the optimal APD parameters that best fit the PA nonlinear trajectories in amplitude and phase for multiple frequencies. Section IV presents a new measurement setup based on two RF vector signal transceivers that is capable of individually measuring the APD nonlinearity and PA nonlinearity. Section V reports the conversion of the presented APD to a single-input/single-output block and validates the APD+PA chain with standard-compliant 5G signals.

II. THEORY

This section presents a large-signal model that can be used to study the APD behavior and evaluate different tuning strategies. The block diagram of the model is shown in Fig. 2. Two nonlinear amplifiers, main and peaking, are fed by two input signals, and their outputs are combined. Each amplifier is described by a strong–weak model, commonly used to study the PA large-signal behavior at different biases [23], [26]. The input signals to the two amplifiers can be written as

$$V_{\text{be}}^m(t) = V_{b,q}^m + \frac{V_{\text{in}}}{\sqrt{2}} \cos(\omega_0 t)$$

¹We choose to call main and peaking amplifiers in analogy with the Doherty/sequential amplifier to enhance readability and understanding.

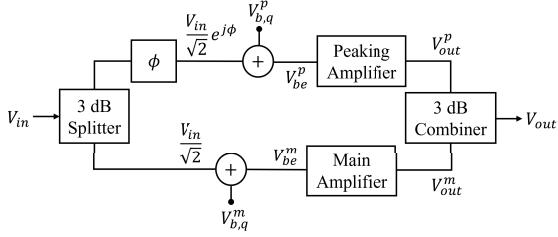


Fig. 2. Block diagram of the proposed APD model.

$$V_{be}^p(t) = V_{b,q}^p + \frac{V_{in}}{\sqrt{2}} \cos(\omega_0 t + \phi) \quad (1)$$

where V_{in} denotes the APD input voltage, $V_{b,q}^m$ and $V_{b,q}^p$ are the quiescent base voltages of the main and peaking amplifiers, respectively, ω_0 is the carrier frequency, and ϕ is the phase offset. As the proposed APD is realized using bipolar junction transistors (BJTs), the strong–weak model can be formulated as

$$I_c(t) = \begin{cases} I_{\max} \exp[k(V_{be}(t) - 1)], & 0 \leq V_{be}(t) \leq 1 \\ I_{\max}, & V_{be}(t) > 1 \\ 0, & V_{be}(t) < 0 \end{cases} \quad (2)$$

where I_{\max} is the maximum current of the transistor, $V_{be}(t)$ is the transistor input voltage, and k is a parameter that models the transistor's turn-on slope. This model accounts for weak nonlinearity due to transconductance variation at the turn-on (first equation), as typical in class-B or deep class-AB amplifiers, and accounts for strong nonlinearity due to current clipping (second equation). By doing so, different amplifier classes, i.e., from class-A to class-C, can be described.

The transistor output voltage at the fundamental can be calculated using Fourier analysis. Assuming the sinusoidal input of (1), the output current of (2) can be expressed as

$$I_c(t) = I_{c,0} + \sum_{n=1}^{\infty} I_{c,n} \cos(n\omega_0 t) \quad (3)$$

where the Fourier coefficients can be calculated with

$$I_{c,n} = \frac{\omega_0}{\pi} \int_0^{\frac{2\pi}{\omega_0}} I_c(t) \cos(n\omega_0 t) dt \quad (4)$$

where $I_{c,0}$ is the collector dc current and $I_{c,1}$ is the current at the fundamental frequency. Therefore, the main and peaking amplifiers' output voltages can be calculated with

$$V_{out}^m = R_l^m I_{c,1}^m, \quad V_{out}^p = R_l^p I_{c,1}^p \quad (5)$$

where R_l^m and R_l^p are the load resistances at the fundamental frequency of the main and peaking amplifiers, respectively. The outputs of the two amplifiers are summed using a 3-dB combiner, and the APD output voltage is given by

$$V_{out} = \frac{1}{\sqrt{2}} V_{out}^m + \frac{1}{\sqrt{2}} V_{out}^p. \quad (6)$$

It follows that the APD output voltage is a function of the input voltage, quiescent base voltages, transistor's k , I_{\max} parameters, and phase offset. Therefore, we can express the APD gain G_{apd} as follows:

$$V_{out} = G_{apd} \left(V_{in}, V_{b,q}^m, V_{b,q}^p, k^m, k^p, I_{\max}^m, I_{\max}^p, \phi \right) V_{in}. \quad (7)$$

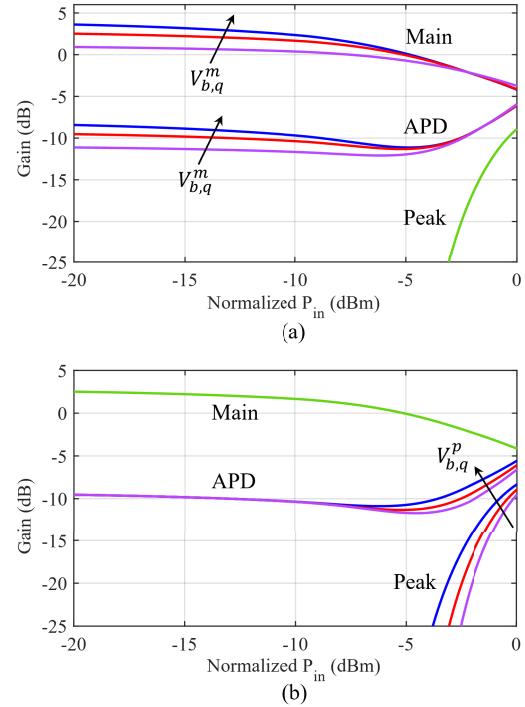


Fig. 3. (a) APD gain for varying main base voltages ($V_{b,q}^m = [0.4, 0.5, 0.6]$ V), while the peaking amplifier base voltage is constant ($V_{b,q}^p = -1$ V). (b) APD gain for varying peaking base voltages ($V_{b,q}^p = [-0.8, -1, -1.2]$ V), while the main amplifier base voltage is constant ($V_{b,q}^m = 0.5$ V).

To verify the basic concept of the proposed APD, we evaluated the model with $V_{in} = 1$ V, $I_{\max}^m = I_{\max}^p = 1$ A, $k^m = k^p = 1$ V $^{-1}$, $R_l^m = R_l^p = 1$ Ω , and $\phi = 180^\circ$.

Fig. 3(a) shows the APD gain for the main amplifier biased in class-AB and the peaking amplifier biased in class-C. As evidenced by the plot, this asymmetry in the base quiescent voltages creates a gap or a “valley” in the APD gain profile. The depth of the valley can be adjusted by biasing the main amplifier in deeper or shallower class-AB and by introducing an emitter resistor that reduces the gain at higher input powers (this approach was followed in the design).

Fig. 3(b) shows the impact on the APD gain by varying the bias of the peaking amplifier while keeping the bias of the main amplifier constant. This bias can be used to shift the APD gain expansion to higher or lower power levels. These results suggest the suitability of the proposed APD concept to correct the gain profiles of Fig. 1. We note this model does not consider the AM/PM behavior of the APD circuit, as this would be highly device-specific, and so, the resulting model would be complex and unsuited for a global evaluation of the proposed approach. The AM/PM part, necessary for an accurate PA linearization, will instead be considered in Section III, which describes the design of the APD circuit.

III. DESIGN

This section presents the design procedure of the APD circuit. As evidenced by the theory, two nonlinear branches are needed to synthesize the compressing and expanding behavior

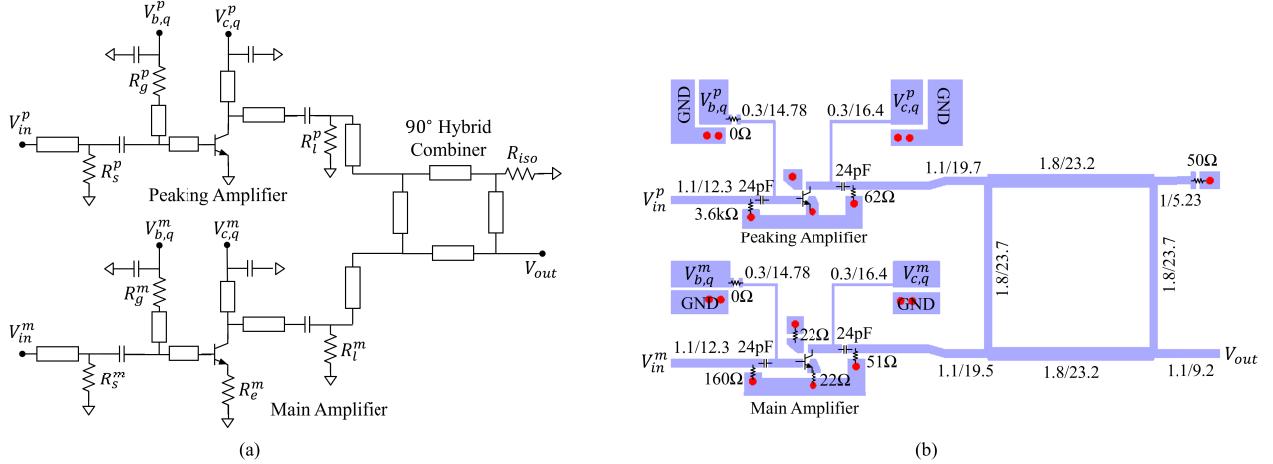


Fig. 4. (a) Schematic of the dual-input APD for class-AB gain linearization. The bias point and terminations of the nonlinear amplifiers are individually optimized to generate the inverse PA nonlinear characteristic in amplitude and phase. The outputs of the two amplifiers are combined with 90° branchline hybrid. (b) Layout of the APD with indication of transmission line geometries (width/length in mm), component values, and bias voltages; also, red circles show via holes. The layout size is 76.9 × 55.4 mm.

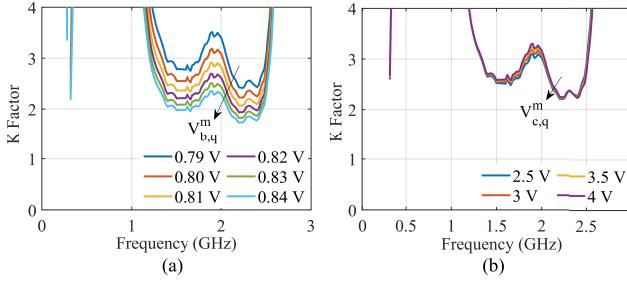


Fig. 5. K -factor curves used for different (a) base quiescent voltages and for different (b) collector quiescent voltages. Source and load resistors are selected to ensure unconditional stability of the main amplifier in the worst case for the stability of $V_{b,q}^m = 0.84$ V and $V_{c,q}^m = 2.5$ V.

that corrects the PA gain peaking. To demonstrate this, we design an APD for the linearization of an L/S-band PA with the goal of attaining a linearity comparable to a standard DPD, while requiring minimal power consumption. Given the low-frequency operation, we adopted BJTs instead of field-effect transistors because of their higher efficiency at low voltages and lower noise figure. The Infineon BFR183 bipolar transistor was selected and biased with a collector voltage of 3 V. This transistor achieves an f_T of 8 GHz and a noise figure of 1.4 dB at 1.8 GHz, which makes it well suited for a low-power APD block that can be inserted at the beginning of the transmitter chain. Fig. 4(a) shows the schematic of the APD circuit.

The first step is the design of the amplifier stability network. As highlighted by the model, the main amplifier needs to be biased in class-AB, and so, the stability can be evaluated using the K -factor method. Unlike a typical stability study, here, the stability must be verified for variable base and collector voltages, as these voltages may be tuned to match the APD characteristics to the PA. After evaluating various stabilization circuits, a source and load stability resistor is the one that maximizes the APD tuning range. To reduce the dc power dissipation without affecting RF stability, these resistors were placed outside the dc block capacitors. Fig. 5 shows the

K -factor curves for different base voltages in the main amplifier. A small reduction of the K -factor is found at increasing collector voltages. The large-signal stability of the peaking amplifier is verified using the STAN tool in Microwave Office.

It is important to mention the role of the emitter degeneration resistor R_e^m in the main amplifier. This resistor is used to introduce a negative feedback that reduces the gain at higher input voltages [27], and this was used to expand the “valley” created by the APD circuit and match the “hump” of the PA. This resistor also helps to reduce the thermal runaway affecting the low-frequency stability of a bipolar transistor (problematic only in the main amplifier). As shown by Fig. 5, the amplifier stability degrades at higher base voltages that correspond to higher collector bias currents. The resulting K -factor curves satisfy a safe limit of $K > 1.5$ for multiple biases.

Next, the circuit layout is designed using a Rogers 4350B substrate of 0.51 mm thickness, $\epsilon_r = 3.66$, and $\tan \delta = 0.004$. In the layout of Fig. 4(b), the interconnections are all 50 Ω (1.1 mm width), and their length is chosen to interconnect the components. A 90° branch-line coupler is used to combine the amplifier’s outputs, with the differential port terminated on a 50-Ω resistor. A 90° branch-line coupler is used because of the 90° phase difference at the outputs of the digital splitter (pSemi 46120) that will be later used. The branch-line coupler is designed to provide 15 dB of isolation within 1.8–2.2 GHz to avoid load-modulation effects between the two amplifiers and so achieve independent amplitude and phase tuning.

Next, the APD base voltages, gain values, and phase offset are optimized to match the PA gain and phase nonlinear trajectories at a given frequency. To this aim, the PA is characterized at 1.8, 2.0, and 2.2 GHz with $I_{d,q}^{pa} = 90$ mA, and its characteristics are imported into the simulator and used as a target trajectory. The architecture used for this optimization is shown in Fig. 6(a). The APD inputs are generated with an ideal 3-dB splitter, and their amplitudes and phase offset are adjusted by two gain blocks, G_m and G_p , and a phase shifter, ϕ . The blocks before the APD will be later implemented using an off-the-shelf monolithic amplitude and phase controller (see

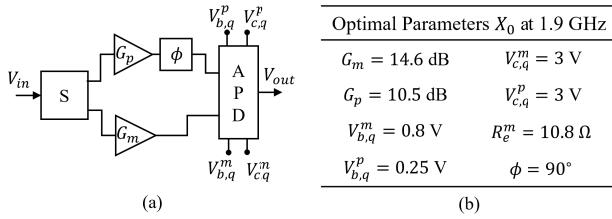


Fig. 6. (a) Block diagram used for the APD parameters optimization. (b) Optimal parameters for 1.9 GHz that were found by the algorithm.

Section V). Therefore, we define the following parameter array to optimize the APD response:

$$X(f) = [G_m, G_p, V_{b,q}^m, V_{b,q}^p, R_e^m, \phi]. \quad (8)$$

These parameters were constrained to ensure they did not exceed the maximum limits of the selected transistor. Assuming an APD maximum input power of \$P_{in}^{\max} = 0\$ dBm, the \$G_m\$ and \$G_p\$ gains are constrained to limit the maximum base-emitter voltage swing to 2-V peak-to-peak, and the quiescent voltages are limited to [0, 0.9] V, so that the transistor's maximum power dissipation (dc + RF) did not exceed 450 mW. The emitter resistor in the main amplifier is constrained between 0 and 12 \$\Omega\$, and the phase offset is limited to [-180°, 180°]. The cost function of the optimization problem is defined as

$$J(X(f)) = \sum_{P_{in}=0}^{P_{in}^{\max}} |G_{apd}(P_{in}, f, X(f)) - G_{tgt}(P_{in}, f)|^2 \quad (9)$$

where \$G_{tgt}\$ is the APD target characteristic that corresponds to the inverted PA gain and phase response. This target function can be obtained by simulations or by directly measuring the PA (approach followed in this article).

As the circuit optimizer operates on real and imaginary values, the \$G_{tgt}(P_{in}, f)\$ function has to be converted into Cartesian form, namely

$$G_{tgt}(P_{in}, f) = G_{tgt}^{re}(P_{in}, f) + jG_{tgt}^{im}(P_{in}, f). \quad (10)$$

Therefore, the argument of the sum in (9) can be redefined in terms of real and imaginary parts as follows:

$$|G_{apd} - G_{tgt}|^2 = (G_{apd}^{re} - G_{tgt}^{re})^2 + (G_{apd}^{im} - G_{tgt}^{im})^2. \quad (11)$$

In this last equation, the dependency on the parameters is suppressed for brevity. Therefore, the cost function can be broken into two parts that can be defined in the circuit simulator as follows:

$$\begin{aligned} J_{re}(X(f)) &= \sum_{P_{in}=0}^{P_{in}^{\max}} (G_{apd}^{re}(P_{in}, f, X(f)) - G_{tgt}^{re}(P_{in}, f))^2 \\ J_{im}(X(f)) &= \sum_{P_{in}=0}^{P_{in}^{\max}} (G_{apd}^{im}(P_{in}, f, X(f)) - G_{tgt}^{im}(P_{in}, f))^2. \end{aligned} \quad (12)$$

The optimization algorithm searches for the parameters \$X_0(f)\$ that minimize the sum of the real and imaginary cost functions over the selected powers at a frequency \$f\$. As this design is a multimodal problem with many local minima, the

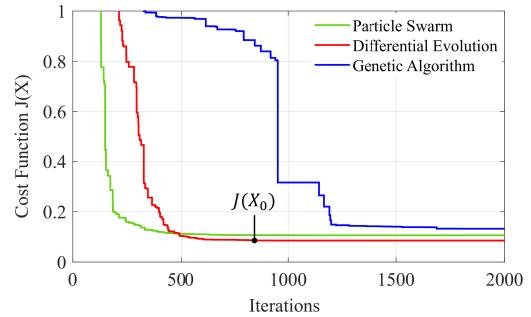


Fig. 7. Evolution of the average cost function for 1.9 GHz obtained by averaging ten trials with random initialization. On average, differential evolution is the algorithm achieving the lowest cost function for this problem.

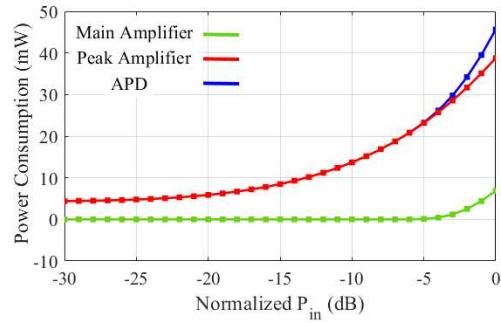


Fig. 8. Simulated dissipated power of the main amplifier, peaking amplifier, and APD circuit with parameters \$X_0\$ at 1.9 GHz. When the input power is at the maximum, the APD power dissipation is 45 mW, while at small signal, the dissipation is 5 mW.

choice of the optimization algorithm affects the convergence rate and optimality of the solution [28]. Fig. 7 shows the average cost function for ten different trials using three nature-inspired optimization algorithms, all starting from a random initialization of the parameters. Differential evolution is the algorithm that (on average) converges to the lowest cost function. The optimized parameters are listed in Fig. 6(b).

The overall APD power consumption is the sum of the dc power consumption of the main amplifier, peaking amplifier, and of the input splitter

$$P_{dc}^{apd} = V_{dc}^m I_{dc}^m + V_{dc}^p I_{dc}^p + V_{dc}^{spl} I_{dc}^{spl}. \quad (13)$$

With the parameters \$X_0\$, the power consumption is shown in Fig. 8. Overall, the simulated APD consumption is 5 mW at small signal and 45 mW at the maximum input power, where both the main and peaking amplifiers are active. Such low values are the result of a bipolar transistor choice, a stability network that does not dissipate static power, and a low collector bias voltage of 3 V.

With the parameters \$X_0\$, Fig. 9 shows the large-signal frequency response of the APD circuit in amplitude and phase. We note that for best broadband performance, the parameters \$X\$ should be optimized for every frequency point. Finally, Fig. 10 shows the simulated versus target characteristics in amplitude and phase for 2 and 2.2 GHz, demonstrating a nearly precise match, which ensures amplitude and phase flatness of the APD + PA response. As seen, this algorithm is effective at finding a

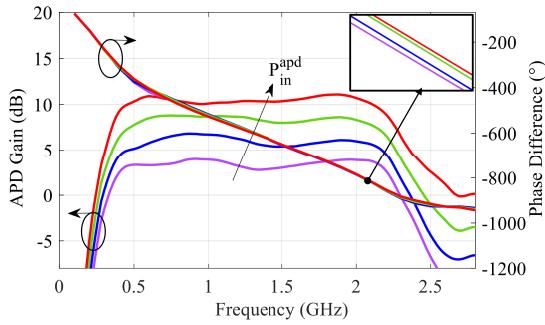


Fig. 9. Simulated APD gain and phase characteristics for different input powers and for the parameters X_0 . Within the APD bandwidth of 0.4–2.3 GHz, the gain and phase expansion are about 7 dB and 15° , respectively. Despite the wide bandwidth available, this APD will be demonstrated in single-input/single-output mode over the 1.8–2.2-GHz range.

set of parameters that approximates the target trajectories over the frequency range and power levels.

IV. DUAL-INPUT APD AND PA CHARACTERIZATION

A. Measurement Setup

To evaluate the performance of the APD and PA with modulated signals, the test setup of Fig. 11 was created. This setup uses two vector signal transceivers with 1.2-GHz bandwidth (Keysight VXTs M9411A) to generate and analyze complex modulated signals. The two VXTs are operated with phase coherency by using a 10-MHz reference signal and are synchronized at baseband with a trigger, similar to [29], [30], and [31]. With this setup, the APD was characterized in dual-input mode to confirm results from circuit simulations and explore different driving strategies. The simulated APD input power P_{in} was converted to the two input powers P_{in}^m and P_{in}^p with

$$\begin{aligned} P_{\text{in}}^m &= P_{\text{in}} + G_m - 3 \text{ dB} \\ P_{\text{in}}^p &= P_{\text{in}} + G_p - 3 \text{ dB}. \end{aligned} \quad (14)$$

The phase difference between the two VXTs was de-embedded using a combiner that was precalibrated with a vector network analyzer. Therefore, the simulated phase offset ϕ is also the same in the measurement setup.

The APD output signal is sensed with a 3-dB power divider. Because the APD output power changes with the input amplitudes, bias voltages, and phase offset, a variable attenuator is introduced after the APD to maintain a constant input power to the PA. The variable attenuator (pSemi PE43711) provides up to 31.75 dB of attenuation, configurable at steps of 0.25 dB. The attenuator is followed by a dc-2250-MHz low-pass filter (Mini-Circuits VLF-2250+) to remove the harmonics generated by the APD. A driver (Mini-Circuits ZHL-42W) increases the PA input power to 30 dBm. After the driver, a 1.7–2.5 GHz isolator is introduced to improve the match.

The PA is based on a 10-W GaN transistor (Macom CGH40010F) designed to operate in class-AB with a drain bias of 50–150 mA at 28 V, which corresponds to 3%–10% of the transistor's maximum drain current. The amplifier has a compressed gain of 10–11 dB over the bandwidth and achieves

a maximum output power of 41 dBm when the input is at 30 dBm. The efficiency of the PA is over 65%. When used with deep class-AB biases, this PA exhibits the typical gain expansion followed by a compression of Fig. 1. The setup was calibrated with a power meter at multiple power levels and at different frequency points between 1.8 and 2.2 GHz.

B. Pulsed Measurements

The APD and PA are first characterized by using 1- μ s Gaussian pulses to investigate linearity, verify tunability range, and correlate results with theory and simulations. The Gaussian pulse shape was found to be optimal for capturing nonlinear effects in a reduced measurement time, as a single pulse is needed instead of multiple pulses at different amplitudes, as in conventional techniques [32]. Therefore, the Gaussian pulse shape was adopted to evaluate the APD and PA with a narrowband signal before performing broadband measurements.

The APD-only nonlinear characteristics are measured for different quiescent base voltages and phase offsets. As found in simulations, the base voltage of the main amplifier can be used to increase/decrease the back-off gain of the APD, as evident in Fig. 12(a). The base voltage of the peaking amplifier can instead be used to anticipate or delay the gain expansion of the APD. By suitably adjusting the turn-on of the main and peaking amplifiers, it is possible to achieve a “spoon” shape that is complementary to the PA gain “hump.” We note this APD is also able to correct for the typical compressing gain of class-A or shallow class-AB amplifiers by adjusting the APD backoff gain until it becomes constant [red curve in Fig. 12(a)]. In fact, when the main amplifier is turned off, it effectively becomes a linear branch, as the APD presented in [14] and [15]. Regarding the phase nonlinearity, this can be tuned by changing the phase offset ϕ , as shown in Fig. 12(d).

Importantly, when tuning the amplitude or phase nonlinearities, the phase or amplitude nonlinearities remain approximately constant, as highlighted by Fig. 12(b) and (c). This independent tunability of the nonlinear characteristics is achieved by designing a combiner with high isolation (>15 dB) over the APD bandwidth. However, the individual amplitude and phase nonlinearities [Fig. 12(a) and (d)] are determined by the transistor nonlinearity, bias, and so on and must be tailored to match the specific PA characteristics.

Next, the APD + PA chain was evaluated for multiple PA bias points. Fig. 12(e) and (f) shows the APD, PA, and APD + PA nonlinearities at 2 GHz captured by the measurement setup for different PA bias currents between 50 and 150 mA. The proposed APD is effective in correcting for the PA gain expansion–compression and phase shift for different PA bias currents. The combined APD + PA gain and phase are ± 0.3 dB and $\pm 3^\circ$ around zero. Specifically, the proposed APD is effective in: 1) enhancing the gain in the backoff region when the PA is in a deep class-AB ($I_{d,q}^{\text{pa}} = 50$ mA or 3% of $I_{d,\text{max}}^{\text{pa}}$); 2) achieving a complementary gain “valley” matching the PA gain “hump”; and 3) expanding the gain to cancel out the PA gain compression. When the PA is in mid-class AB ($I_{d,q}^{\text{pa}} = 150$ mA or 10% of $I_{d,\text{max}}^{\text{pa}}$), the same APD is still able to linearize the PA in both amplitude and phase: 1) in

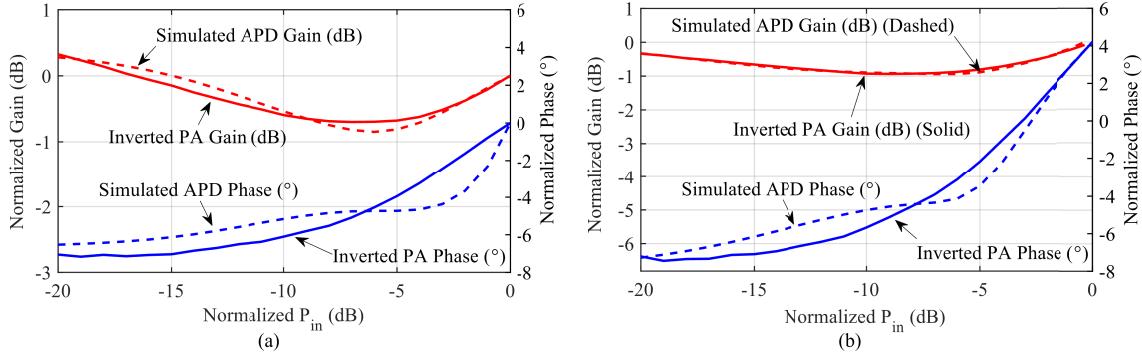


Fig. 10. Simulated APD gain/phase and target trajectories at (a) 2 and (b) 2.2 GHz for two different sets of parameters. The target trajectories were obtained by measuring the PA at 2 and 2.2 GHz. A good agreement was found using the proposed APD circuit in both amplitude and phase.

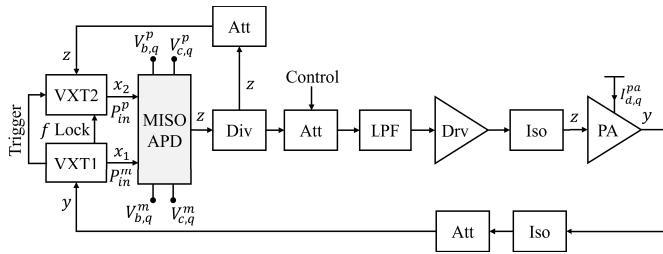


Fig. 11. Setup for the APD in dual-input mode. Two synchronized transceivers generate the APD inputs. This setup allows for the simultaneous acquisition of the APD only, PA only, and APD + PA characteristics.

the back-off region, the APD provides a linear and opposed gain to the PA; and 2) during the PA compression, the APD performs a matched gain expansion that linearizes the chain response. A similar discussion can be performed for the phase nonlinearities, where the APD is demonstrated to be effective on a wide range of PA bias currents. We note that the gain and phase dispersion become more evident in the deep backoff region (near -20 dB of normalized input power), but this will have a low impact as the signal average is usually located at around -10 dB from the peak power.

V. APD AND PA CHARACTERIZATION WITH 5G WIDEBAND SIGNALS

In this section, the APD is evaluated in a typical base-station scenario with 5G waveforms by using standard-compliant analysis software. To this purpose, the dual-input APD was converted to a single-input/single-output block by using a monolithic phase and amplitude controller (pSemi 46120) shown in Fig. 13. This controller splits the RF input signal into two outputs with 0° and 90° phase shifts. The 90° phase difference is compensated by the 90° hybrid branch-line coupler at the APD output, so that the differential phase ϕ between the two channels can be directly programmed with the controller. The controller integrates on the first output a phase shifter of 0° – 87.2° , configurable at steps of 2.8° . On the second output, a variable attenuator of 0° – 7.5 dB (0.5-dB steps) and a phase shifter of 0° – 87.2° (2.8° steps) are available. Therefore, the differential phase ϕ can be configured between -87.2° and 87.2° . The controller operates between 1.8 and

2.2 GHz, and its power consumption is less than 2 mW when supplied with 5 V. The controller is programmed via a 14-bit serial interface connected to an FTDI FT232RL chip that provides USB connection to the controller.

A downlink 5G orthogonal frequency-division multiplexing (OFDM) signal of different channel bandwidths (5–100 MHz) was created using a waveform generation software (Keysight Waveform Builder Pro). In this signal, a single frame was embedded, the symbols are modulated with 256 quadrature amplitude modulation (QAM), and the carrier spacing was 30 kHz (numerology $\mu = 1$). The resulting signal presents a Rayleigh pdf and a PAPR of 10.5 dB. Later, in this article, results with a 100-MHz OFDM signal with 256-QAM are presented, which represents the widest FR1 bandwidth and QAM order in the latest 5G release [33]. According to the 5G standard [33], the transmitter output must achieve an ACLR lower than -45 dBc on both sides, measured with 100-kHz resolution bandwidth and with 1.72-MHz guard bands [33]; 3GPP also sets a minimum requirement of 3.5% on the average EVM for 256 QAM [33]. Such metrics are measured on the single-input/single-output APD + PA transmitter by means of standard-compliant software (Keysight PathWave X-Series 5G/NR Application).

The first step was finding the optimal APD configuration for a given average power. This entailed determining the controller attenuation and phase settings, the APD biases, and the output attenuation for a given carrier frequency. The procedure used to determine APD settings is as follows.

- 1) Set the PA quiescent current $I_{d,q}^{\text{pa}}$ to a bias point in shallow or deep class-AB.
- 2) Configure the setup with the APD in dual-input mode as in Fig. 11. Starting from the APD voltages determined during the APD design, find the optimal input amplitudes and phase offset that ensure the best APD + PA gain and phase flatness.
- 3) Adjust the APD biases while keeping the input amplitudes and phase offset constant. Repeat steps 1)–3) until satisfactory results are obtained.
- 4) Find the external attenuator value for the selected carrier frequency that ensures the required $P_{\text{in}}^{\text{pa}}$ to the PA.

It is important to point out that tuning the APD with wideband signals may result in different settings as compared

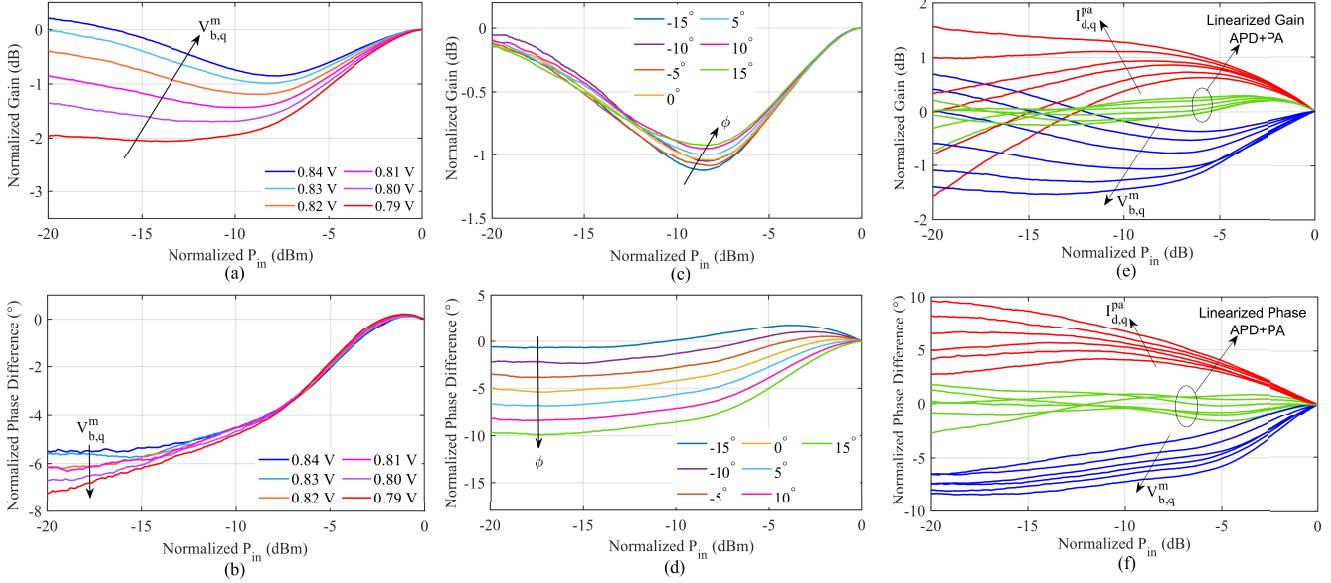


Fig. 12. APD (a) gain and (b) phase nonlinearities for varying $V_{b,q}^m$ and fixed phase offset. APD (c) gain and (d) phase nonlinearities for varying phase offsets ϕ and fixed $V_{b,q}^m$. The small gain variation with ϕ also demonstrates that amplitude and phase can be tuned independently. (e) Gain and (f) phase nonlinearities for the PA-only, APD-only, and APD + PA obtained with pulse measurements for $I_{d,q}^{pa} = [50, 70, 90, 110, 130, 150]$ mA and optimized $V_{b,q}^m \in [0.78, 0.83]$ V to match the characteristics. The APD demonstrates adaptability from shallow to deep class-AB biases.

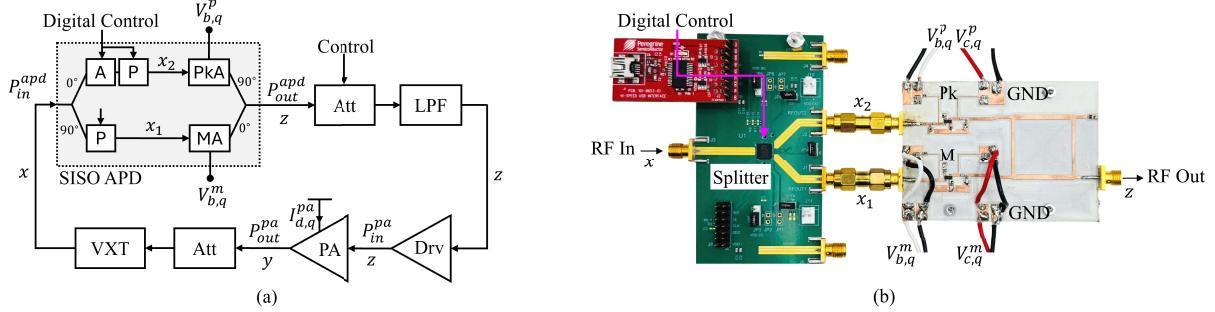


Fig. 13. (a) Block diagram of the setup used for the characterization of the single-input/single-output APD with 5G modulated signals. The control signals and tuning voltages are indicated on the block diagram. (b) Photograph of the single-input/single-output APD.

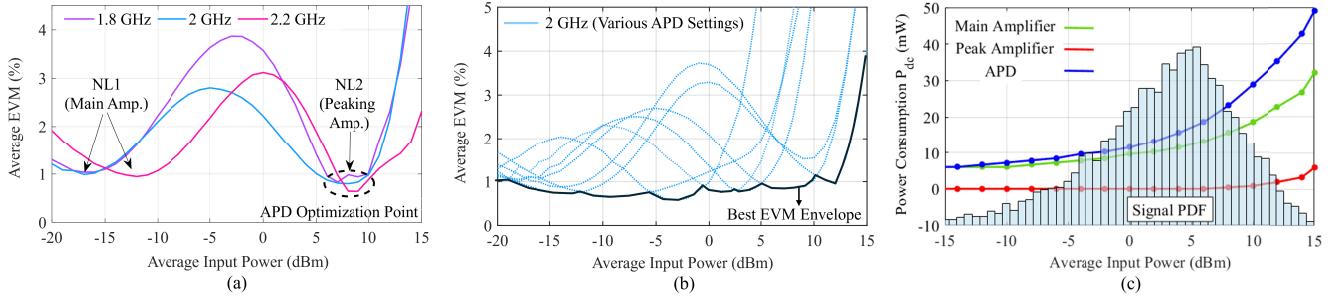


Fig. 14. (a) Average EVM with the APD optimized for 7-dBm average input power at 1.8, 2, and 2.2 GHz. Independently of the frequency, the APD achieves an EVM of less than 1% (3.5% is the limit for 256-QAM signals [33]). (b) Average EVM with the APD optimized for different power levels at a fixed frequency of 2 GHz. (c) Power consumption of the main amplifier, peaking amplifier, and APD circuit at 2 GHz. Superposed to the curves is the pdf of the 5G 100-MHz signal used.

to the pulse characterization, possibly because of the different thermal and trap states in the PA [34]. We note this operation is not different from what is routinely done with iterative adjustments of DPD as the signal changes.

This APD is able to maintain low EVM over the APD + PA bandwidth at a set power level. This is demonstrated by

Fig. 14(a), which shows a sub-1% EVM for the APD optimized for the same power level (5–10 dBm) at three different frequencies (1.8, 2, and 2.2 GHz). It is interesting to note the presence of two minima points, the first at -17/-12 dBm and the second at 5–10 dBm. This is because the first nonlinearity is active at small signals (main amplifier), whereas the second

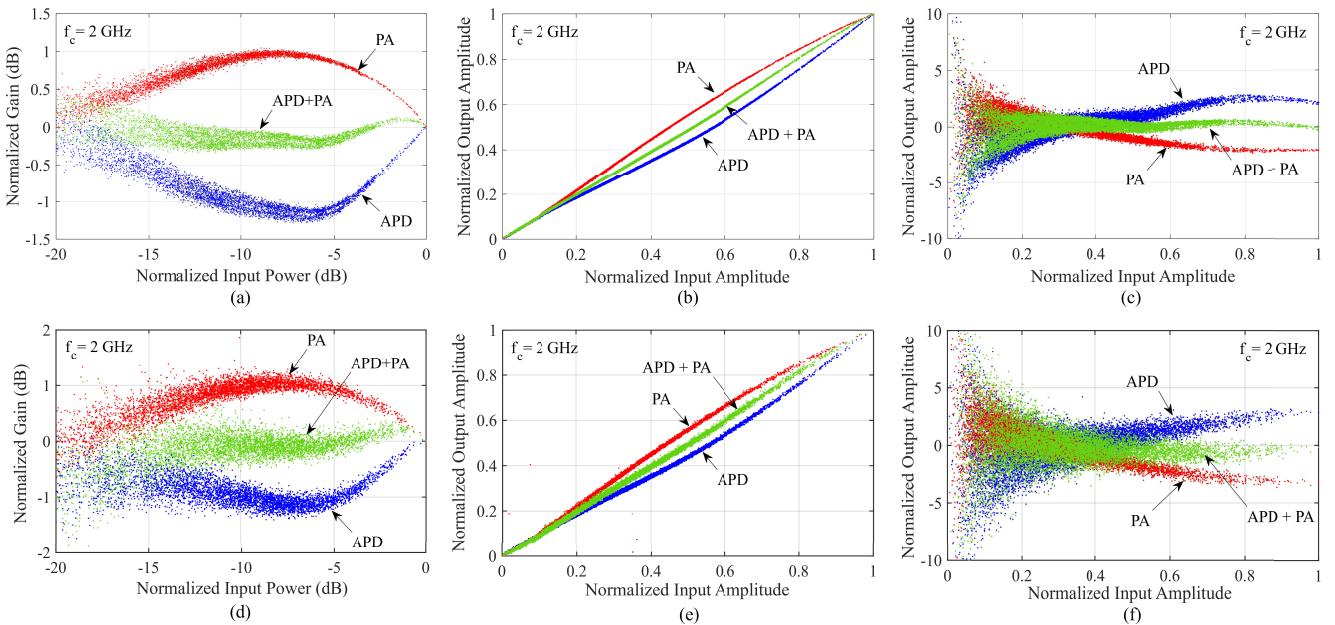


Fig. 15. Measured characteristics with wideband-modulated signals. The dynamic gain is shown in (a) and (d), AM/AM in (b) and (e), and AM/PM is shown in (c) and (f), respectively. These characteristics were obtained with 20-MHz (a)–(c) and 100-MHz, and (d)–(f) 5G OFDM signals with 10.5-dB PAPR centered at 2 GHz. For these measurements, the PA is biased with 90 mA.

nonlinearity is active at small and large signals (main and peaking amplifier). We note that this alternation of local minima and local maxima is no different from what happens with DPD, as DPD is also optimized for a given average power.

This APD can maintain an EVM below 1% for a wide range of powers at a set carrier frequency. This is demonstrated by Fig. 14(b), where all the curves correspond to different APD settings that were optimized to introduce a minimum at a different power level. Here, most of the curves present two minima points because of the two nonlinearities in the APD. When the curve instead presents a single minimum, this is because the two base voltages are close together, and so, the two nonlinearities become a single one. We note, in this plot, that for powers below -15 dBm, the EVM increase can be explained by the degraded signal-to-noise ratio. Instead, for powers above 12 dBm, the EVM is rapidly increasing, and this is due to the compression of the peaking amplifier.

This APD achieves a remarkably low power consumption [Fig. 14(c)]. Such a result is due to the utilization of low-power bipolar transistors and the choice of an input controller with low dc consumption (max 2 mW). For the considered 5G waveform with 10.5-dB PAPR, the APD dissipation is 18 mW, including the consumption of the controller.

As demonstrated with Gaussian pulses, this APD is able to compensate for the gain expansion and compression of a deeply biased PA excited by wideband signals. Fig. 15 shows the obtained characteristics, which present minimal dispersion in both amplitude and phase, thus suggesting very broadband operation. The small residual ripple in the APD + PA characteristic can be explained with the nonperfect matching of APD characteristics with the PA gain “hump.” We note that the proposed APD is able to linearize any shallow

TABLE I
PERFORMANCE SUMMARY WITH 100-MHz 5G OFDM SIGNAL

	Avg. EVM (%)	Peak EVM (%)	Left/Right ACLR (dBc)	ACLR Improvement (dB)	PA Bias Current (mA)	P_{dc} APD (mW)
PA Only	2.5	14.0	-37.0/-37.6	-	45	-
DPD (MP) + PA	0.7	3.4	-48.3/-48.8	11.3/11.2	45	-
APD + PA	0.8	3.1	-46.1/-46.6	8.5/9.0	45	18

biased PAs, as demonstrated by narrowband pulses [Fig. 12(e) and (f)], but the results of these are omitted due to space limitations.

The PA output spectra are shown in Fig. 16 for the 80- and 100-MHz channel bandwidths. These spectra show the PA-only output, the PA combined with DPD, and PA combined with proposed APD. A memory polynomial model is used for DPD, with a nonlinearity order of 9 and a memory order of 2. Both APD and DPD were optimized to provide the best linearity for the same average power of 30 dBm (40.5 dBm at peak). The base voltage of the main amplifier in the APD was tuned to reduce asymmetry in the side bands. We note a small asymmetry of 0.5 dB in the ACLRs (-46.1 / -46.6 dBc) for the 100-MHz signal at 2 GHz, which is, however, below the -45 -dBc requirement [33], as reported in Table I. DPD provides the lowest ACLRs between all cases, achieving -48.3 / -48.8 dBc, which is, however, unnecessary given the requirement of -45 dBc [33]. APD and DPD are also comparable in terms of peak and average EVM. Most importantly, the dc power consumption of APD is only 18 mW, including the controller. Overall, these results suggest that APD is a viable alternative to DPD for FR1 5G signal bandwidths.

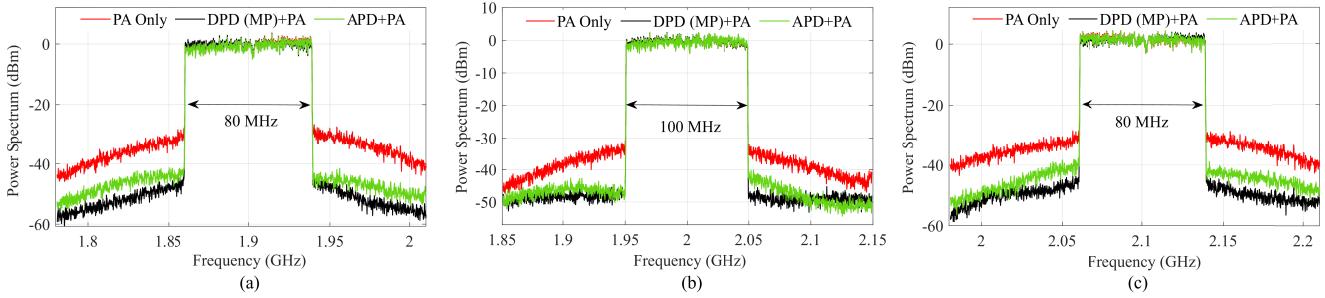


Fig. 16. 5G-modulated signal spectrum analysis for (a) 1.9-GHz, (b) 2-GHz, and (c) 2.1-GHz carrier frequencies with 80- and 100-MHz bandwidths to measure the spectral efficiency, ACLR, and compared with only PA, DPD(MP) + PA, and APD + PA to demonstrate the performance of the proposed APD with realistic communication signals.

TABLE II
COMPARISON WITH THE STATE-OF-THE-ART APDs

Related Works	PA Type	APD Type	Relative Bandwidth (%)	Central Frequency (GHz)	APD Bandwidth (MHz)	Signal Bandwidth (MHz)	Left/Right ACLR (dBc)	ACLR Improvement (dB)	Average EVM (%)	EVM Improvement (pp)	Power Consumption (mW)
Song, 2024-25 [7] [8]	Doherty	1-branch 2-diode	2.2	3.6	80	80	-45.1/-44.1	10	2.2	-	344
Kumar, 2024 [18]	Doherty	2-branch 2-diode	23.5	3.4	800	100	-47.6/-47.8	-	-	-	255
Pitt, 2025 [20]	Doherty	3-branch 3-diode	17.4	2.3	400	80	-40.9/-40.9	6	5.0	-	-
Cappello, 2024 [15]	Class-AB	2-branch 1-diode	33.3	18.0	6000	750	-	7	-	-	-
Yu, 2025 [17]	Class-AB	2-branch 2-diode	35.2	1.7	600	1	-45.5/-45.2*	12	-	-	-
This Work	Class-AB	2-branch 2-transistor	20.0	2.0	400	100	-46.1/-46.6	9	0.8	11	18

* Data obtained from a plot.

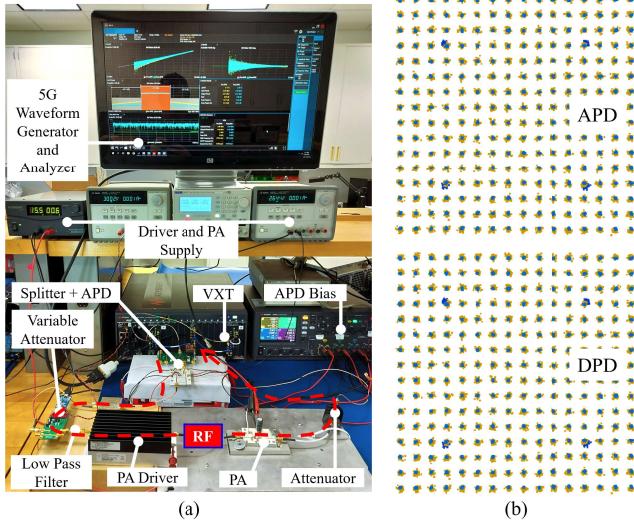


Fig. 17. (a) Photograph of the APD setup with standard-compliant analysis software. (b) Measured constellations of a 5G 100-MHz OFDM signal for the PA only (yellow dots), with DPD and APD (blue dots).

The constellations of the demodulated symbols and setup are shown in Fig. 17. The AM/AM and AM/PM distortion in PA-only case is manifest as a cloud of points around the reference symbols of the considered 256-QAM modulation. Such dispersion results in degraded average and peak EVM,

as evidenced by Table I. A sub-1% EVM is observed for this APD, which is comparable to the values found for the DPD case. ACLRs are also below -45 dBc as required by the standard [33]. Such results demonstrate the viability of the proposed APD for L/S-band 5G base stations. As previously anticipated, the advantage of APD is in reduced complexity, cost, and power consumption of the digital baseband, due to the reduced/removed needs of high-speed DACs, high-throughput DSP/FPGAs, and wideband upconverters.

For bandwidths below 100 MHz, the ACLR values improve significantly, as shown in Fig. 18. An ACLR lower than -49 dBc is observed for the widely used 20-MHz channel bandwidth. These two plots also show the main amplifier base voltage ($V_{b,q}^m$) that was optimized to reduce ACLR. As shown in the bottom plot, this voltage can be used to reduce the asymmetry between the left and right ACLRs, which is typically symptomatic of memory effects.

In Table II, the proposed circuit is compared to other state-of-the-art APDs. The proposed digitally assisted APD exhibits a remarkable fractional bandwidth of 20%, especially considering the low central frequency of 2 GHz. After careful testing with 5G waveforms, this APD satisfies 5G requirements with ACLRs of -46.1 – -46.6 dBc and an average EVM of 0.8% with 100-MHz 256-QAM signals, measured using the standard-compliant software. A much wider bandwidth could be achieved by accepting ACLRs lower than -45 dBc, but this

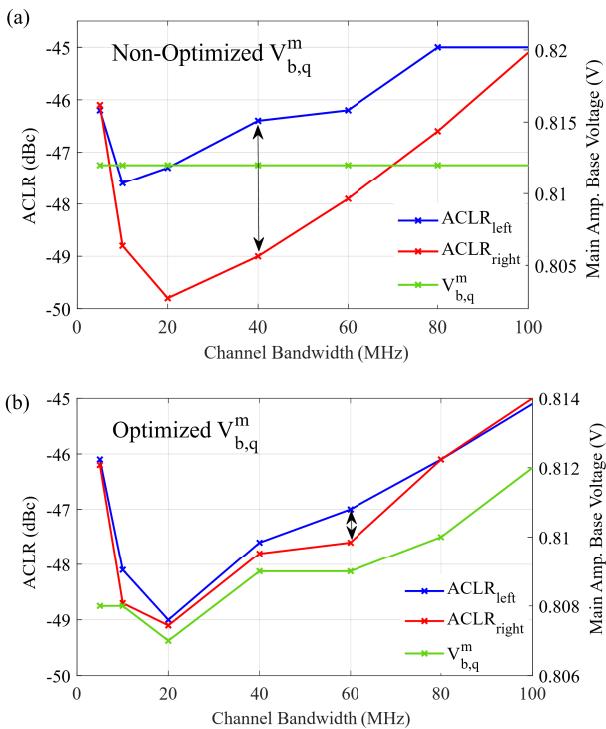


Fig. 18. ACLR for varying channel bandwidths between 5 and 100 MHz while keeping the main amplifier base (a) voltage constant and while optimizing (b) voltage to reduce asymmetry.

would not be compliant with 5G regulations. Due to the use of low-power BJT transistors and digital controllers, this APD also results in a remarkably low power consumption of only 18 mW, which is much lower than other diode-based APDs. Such low power consumption also suggests the suitability of APD for PAs of subwatt power levels, e.g., for low-power IoT nodes or for mobile handsets.

VI. CONCLUSION

This article presents a digitally controlled APD linearizer for RF PAs, based on a dual-branch dual-transistor with an isolated output combiner. This APD is able to accurately compensate for gain and phase distortions of a broad range of PA biasing conditions, from shallow to deep class-AB, and for a wide range of PA output powers and carrier frequencies.

Extensive experimental validation and optimization in the 1.8–2.2-GHz range is performed using first narrowband Gaussian pulses and then with a 100-MHz 5G downlink signal. Using standard-compliant test equipment and software, the proposed APD achieved an ACLR below –46 dBc and an EVM of 0.8%, while consuming only 18 mW. When the same transmitter lineup is linearized by a memory-polynomial DPD, similar performance is attained, i.e., an ALCR of –48 dBc and EVM of 0.7%.

Given these results, the proposed APD can be used in 5G L-/S-band transmitters and contribute to reducing the form factor, power consumption, and cost, while maintaining 5G-compliant linearity. Given also the low input drive requirements (approximately 10 dBm), low supply voltage

(3 V), and low power consumption (18 mW), this solution can be used at the beginning of the amplification chain for maximum system simplification. Ongoing research is aimed at developing a monolithically integrated version of this APD for FR2 frequencies, where instantaneous bandwidths are too large for DPD solutions.

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