FINOLEX ACADEMY OF MANAGEMENT AND TECHNOLOGY, RATNAGIRI
DEPARTMENT OF INFORMATION TECHNOLOGY
SUB:LOGIC DESIGN (SE IT)

ASSIGNMENT NO. 02 (ROLL NO. 01-10)

1 Design a asynchronous 2 bit up- down counter.

2 Convert SR to T FF.

3 Design BCD counter using JK FF.

4 Write a VHDL code for multiplexer.

ASSIGNMENT NO. 02 (ROLL NO. 11-20)

1 Design synchronous 2 bit up-down counter

2 Convert SR FF to D FF.

3 Design a counter which will pass through states 0-2-5-6.

4 Write a VHDL code for basic gates.

ASSIGNMENT NO. 02 (ROLL NO. 21-30)

1 Design synchronous 3 bit up counter.

2 Convert JK FF to D FF.

3 Design Mod 8 counter using JK FF.

4 Write a VHDL code for multiplexer

ASSIGNMENT NO. 02 (ROLL NO. 31-40)

1 Design 3 bit up-down counter.

2. Convert JK FF to T FF.

3 Design Mod 6 counter using JK FF..

4 Write a VHDL code for multiplexer

ASSIGNMENT NO. 02 (ROLL NO. 41-50)

1 Design synchronous 3 bit down counter

2 Convert SR to JK FF.

3 Design Mod 9 counter using JK FF..

4 Write a VHDL code for basic gates.

ASSIGNMENT NO. 02 (ROLL NO. 51-60)

1 Design synchronous 3 bit up-down counter

2 Convert D FF to T FF.

3 Design a Mod 4 up counter using JK FF.

4. Write a VHDL code for multiplexer

ASSIGNMENT NO. 02 (ROLL NO. 61-67)

1 Design synchronous 3 bit up counter

2 Convert T FF to D FF

3 Design a Mod 5 up counter using JK FF..

4 Write a VHDL code for basic gates