Finolex Academy of Management and Technology, Ratnagiri

Department of Information Technology

Subject:	**LOGIC DESIGN (ITC 302)**		
Class:	**SE IT / Semester – III (CBGS) / Academic year: 2017-18**		
Name of Student:			
Roll No:		**Date of performance (DOP) :**	
Assignment/Experiment No:	**3**	**Date of checking (DOC) :**	
Title: Working with IP tables			
Marks:		**Teacher's Signature:**	

1.Aim: Study and Design of half adder, full adder, half subtractor, full subtractor.

2. Prerequisites:
Logic gates

3. Hardware Requirements:

1. IC 7404, 7408, 7432, 7486
2. Digital Trainer kit
3. Breadboard and connecting wires, probes

4. Software Requirements: --

5. Learning Objectives:

1. To understand what is half adder, full adder, half subtractor, full subtractor
2. To understand how design half adder, full adder, half subtractor, full subtractor

6. Course Objectives Applicable: CO 2, CO 3, CO4

7. Program Outcomes Applicable:

8. Program Education Objectives Applicable:

9. Theory: **<Preferably given as handwritten work for students>**

10. Results:

<Source code and screenshots of the output to be added here.>

11. Learning Outcomes Achieved

1. Understanding mounting of logic circuit on breadboard
2. Understanding of what is half adder, full adder, half subtractor, full subtractor.
3. Understanding of how to design half adder, full adder, half subtractor, full subtractor.

12. Conclusion:

13. Experiment/Assignment Evaluation

SR	Parameters	Weight	Excellent	Good	Average	Poor	Not as per requirement
		Scale Factor ->	5	4	3	2	0
1	Technical Understanding	25					
2	Performance / Execution	25					
3	Question Answers	20					
4	Punctuality	20					
5	Presentation	10					
	Total out of 100 --> #(to be converted as per term-work evaluation applicable to the subject)		**∑ (Weight * Scale Factor)/5 = _____**				

References:

[1] Fundamentals of digital circuits by A. Anand Kumar.

Viva Questions

1. What is mean by logic gates?
2. Explain gates with TT and Symbol.
3. What is half adder, full adder, half subtractor, full subtractor? Explain with TT nad logic diagram.
4. How to implement full adder using half adders?