Finolex Academy of Management and Technology, Ratnagiri

**Department of Information Technology**

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|---|---|---|---|
| **Subject:** | **LOGIC DESIGN (ITC 302)** | | |
| **Class:** | **SE IT / Semester – III (CBGS) / Academic year: 2017-18** | | |
| **Name of Student:** | | | |
| **Roll No:** | | **Date of performance (DOP) :** | |
| **Assignment/Experiment No:** | **10** | **Date of checking (DOC) :** | |
| **Title: Working with IP tables** | | | |
| **Marks:** | | **Teacher's Signature:** | |

**1.Aim**: Verify logic gates, half adder, full adder, half subtractor, full subtractor, 4:1mux,8:1 mux using Xilinx ISE 9.2i

**2. Prerequisites**:

Logic gates, half adder, full adder, half subtractor, full subtractor, 4:1mux,8:1 mux

**3. Hardware Requirements**: PC

**4. Software Requirements:** Xilinx ISE 9.2i

**5. Learning Objectives:**

1. To Verify logic gates, half adder, full adder, half subtractor, full subtractor, 4:1mux,8:1 mux using Xilinx ISE 9.2i

**6. Course Objectives Applicable: CO5, CO6**

**7. Program Outcomes Applicable:**

**8. Program Education Objectives Applicable:**

**9. Theory:** **<Preferably given as handwritten work for students>**

**10. Results:**

<Source code and screenshots of the output to be added here.>

**11. Learning Outcomes Achieved**

1. Verification of logic gates, half adder, full adder, half subtractor, full subtractor, 4:1mux,8:1 mux using Xilinx ISE 9.2i

**12. Conclusion:**

## 13. Experiment/Assignment Evaluation

| SR | Parameters | Weight | Excellent | Good | Average | Poor | Not as per requirement |
|---|---|---|---|---|---|---|---|
| | | **Scale Factor ->** | 5 | 4 | 3 | 2 | 0 |
| 1 | Technical Understanding | 25 | | | | | |
| 2 | Performance / Execution | 25 | | | | | |
| 3 | Question Answers | 20 | | | | | |
| 4 | Punctuality | 20 | | | | | |
| 5 | Presentation | 10 | | | | | |
| | Total out of 100 --> #(to be converted as per term-work evaluation applicable to the subject) | | **∑ (Weight * Scale Factor)/5 = _____** | | | | |

# References:

[1] Fundamentals of digital circuits by A. Anand Kumar.
[2]VHDL basics to programming by Gaganpreet Kaur

# Viva Questions

1. What are logic gates, half adder, full adder, half subtractor, full subtractor, 4:1mux,8:1 mux ?
2. What is VHDL.
3. How to write program in VHDL (including entity and architecture)