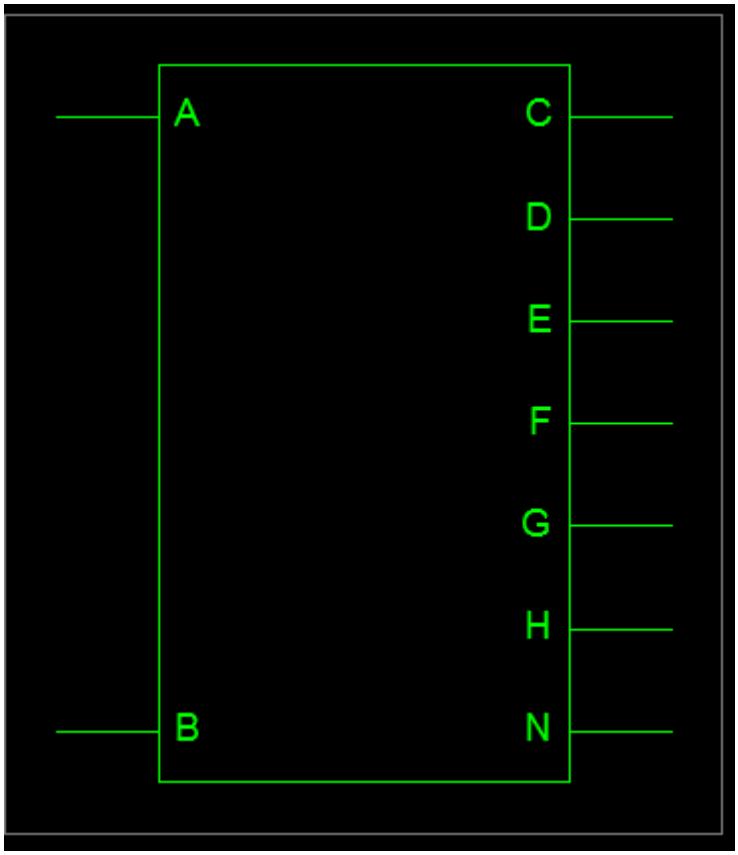
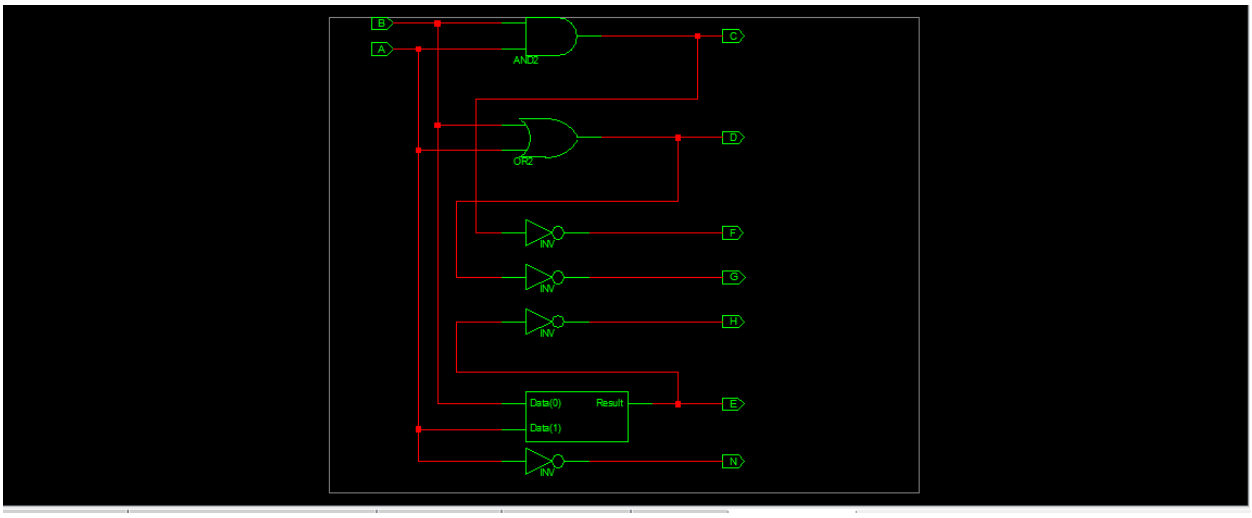
BASIC GATES: SOURCE CODE:

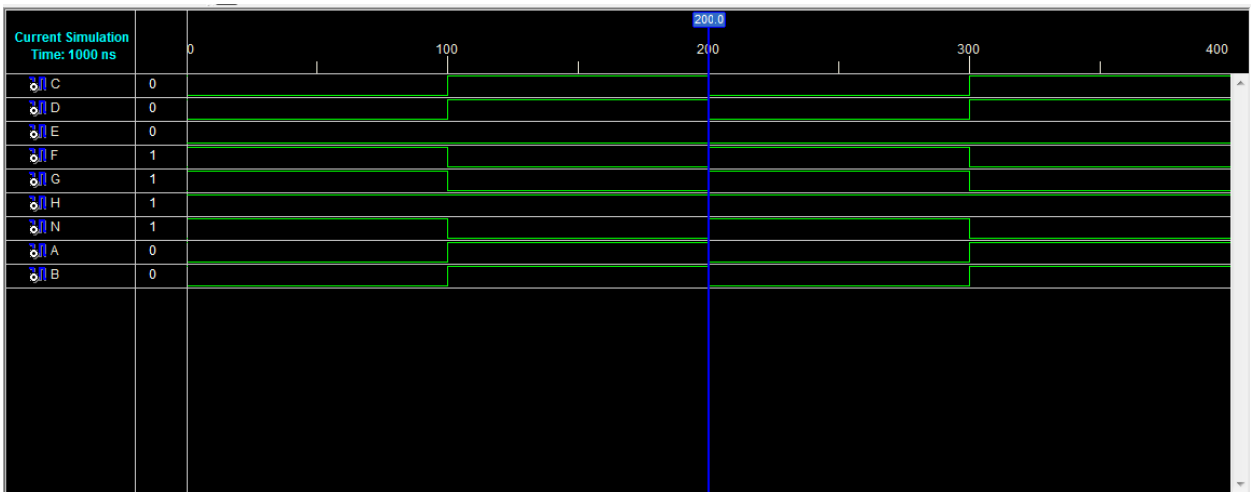
```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    19:28:30 08/20/2011
-- Design Name:
-- Module Name:    basic_gates - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
```

```
entity basic_gates is
   Port ( A : in  STD_LOGIC;
          B : in  STD_LOGIC;
          C : out  STD_LOGIC;
          D : out  STD_LOGIC;
                              E : out  STD_LOGIC;
          F : out  STD_LOGIC;
                              G : out  STD_LOGIC;
                              H : out  STD_LOGIC;
          N : out  STD_LOGIC);
end basic_gates;

architecture Behavioral of basic_gates is

begin
C<= A AND B;
D<= A OR B;
E<= A XOR B;
F<= A NAND B;
G<= A NOR B;
H<= A XNOR B;
N<= NOT A;

end Behavioral;
```

OUTPUT:


A
B
C
D
E
F
G
H
N


B
A
AND2
C
OR2
D
INV
F
INV
G
INV
H
Data(0)
Data(1)
Result
E
INV
N

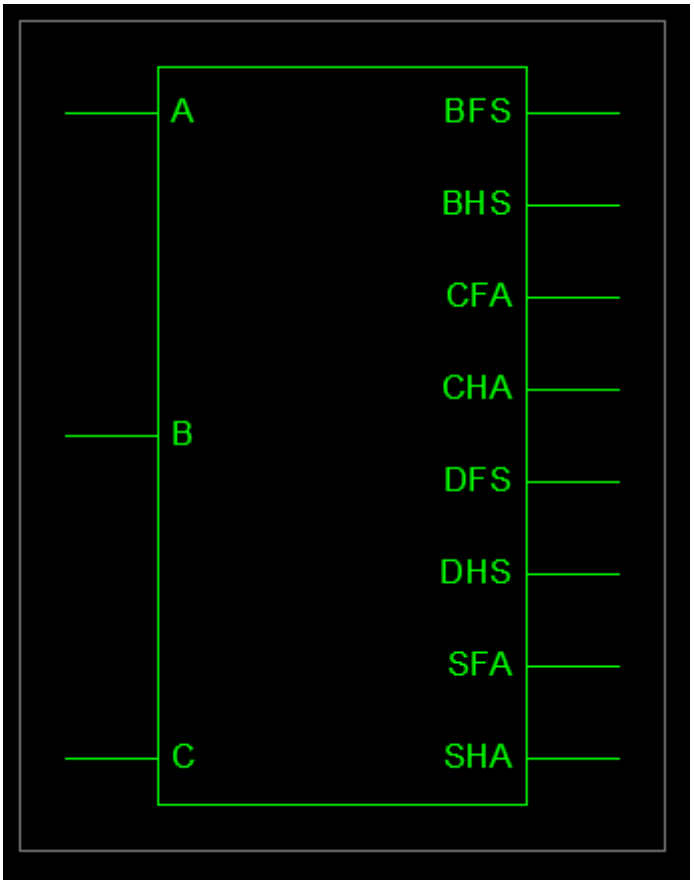

Current Simulation Time: 1000 ns
200.0
0
100
200
300
400
C
0
D
0
E
0
F
1
G
1
H
1
N
1
A
0
B
0

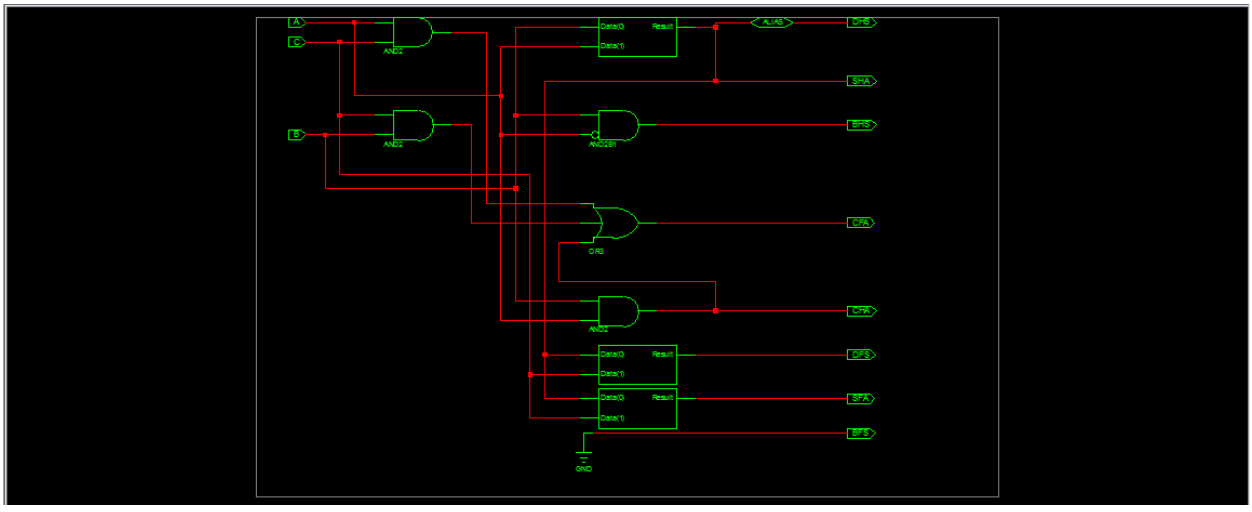
ADDERS AND SUBTRACTORS: SOURCE CODE:

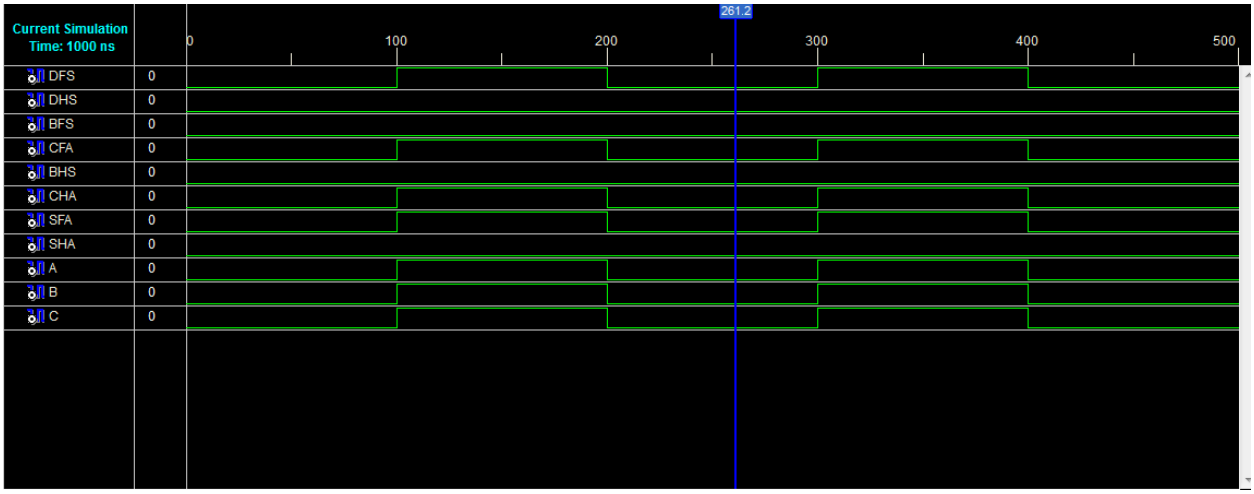
```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    19:55:11 08/20/2011
-- Design Name:
-- Module Name:    all_adders_subtractors - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
```

```
entity all_adders_subtractors is
    Port ( A : in  STD_LOGIC;
           B : in  STD_LOGIC;
           C : in  STD_LOGIC;
           SHA : out  STD_LOGIC;
           SFA : out  STD_LOGIC;
           CHA : out  STD_LOGIC;
           CFA : out  STD_LOGIC;
           DHS : out  STD_LOGIC;
           DFS : out  STD_LOGIC;
           BHS : out  STD_LOGIC;
           BFS : out  STD_LOGIC);
end all_adders_subtractors;

architecture Behavioral of all_adders_subtractors is

begin
SHA<= A XOR B;
SFA<= A XOR B XOR C;
CHA<= A AND B;
CFA<= (A AND B) OR (B AND C) OR (C AND A);
DHS<= A XOR B;
DFS<= A XOR B XOR C;
BHS<= (NOT A) AND B;
BFS<= (NOT A) AND (B XOR C) AND (B AND C);
end Behavioral;
```

OUTPUT:


A
B
C
BFS
BHS
CFA
CHA
DFS
DHS
SFA
SHA


A
C
B
AND2
AND2
AND2B1
OR3
AND2
Data(0)
Data(1)
Result
Data(0)
Data(1)
Data(0)
Data(1)
Result
GND
A1/A0
DHS
SHA
BHS
CFA
CHA
DFS
SFA
BFS

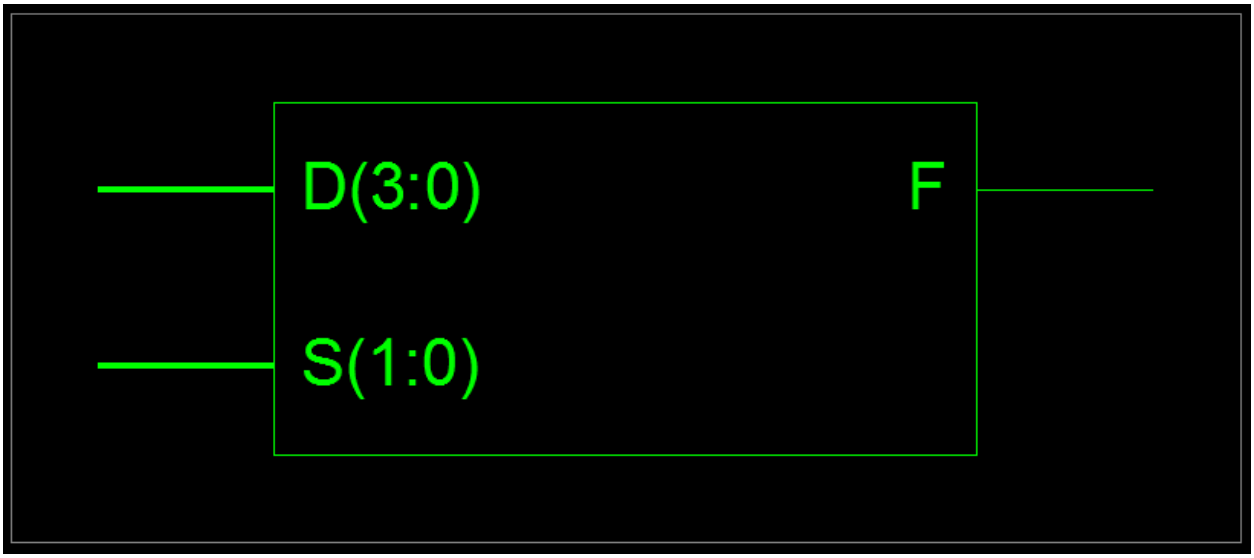

Current Simulation Time: 1000 ns
261.2
0
100
200
300
400
500
DFS
DHS
BFS
CFA
BHS
CHA
SFA
SHA
A
B
C
0

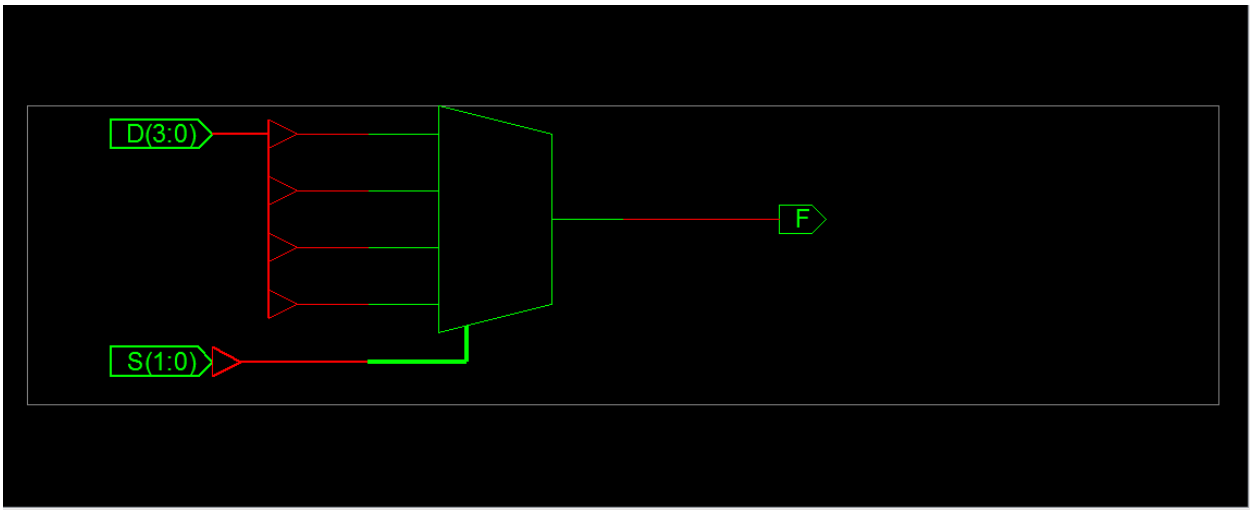
4:1 MUX: SOURCE CODE:

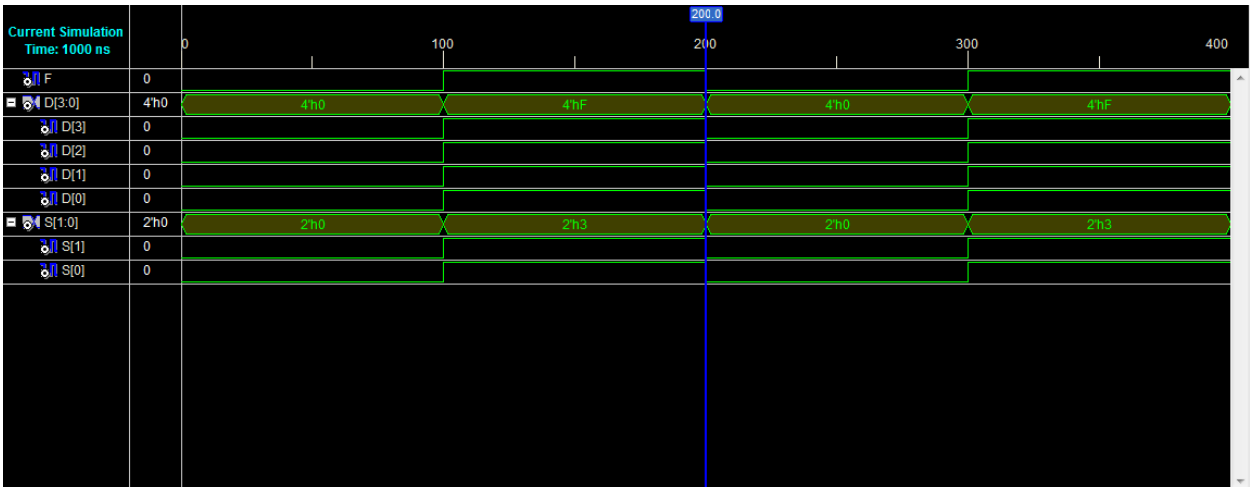
```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    20:35:25 08/20/2011
-- Design Name:
-- Module Name:    MUX11 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
```

```
entity MUX11 is
   Port ( D : in  STD_LOGIC_VECTOR (3 downto 0);
          S : in  STD_LOGIC_VECTOR (1 downto 0);
          F : out  STD_LOGIC);
end MUX11;

architecture Behavioral of MUX11 is

begin
WITH  S SELECT
F<= D(0) WHEN "00",
            D(1) WHEN "01",
             D(2) WHEN "10",
             D(3) WHEN OTHERS;

end Behavioral;
```

OUTPUT:


D(3:0)
F
S(1:0)


D(3:0)
F
S(1:0)

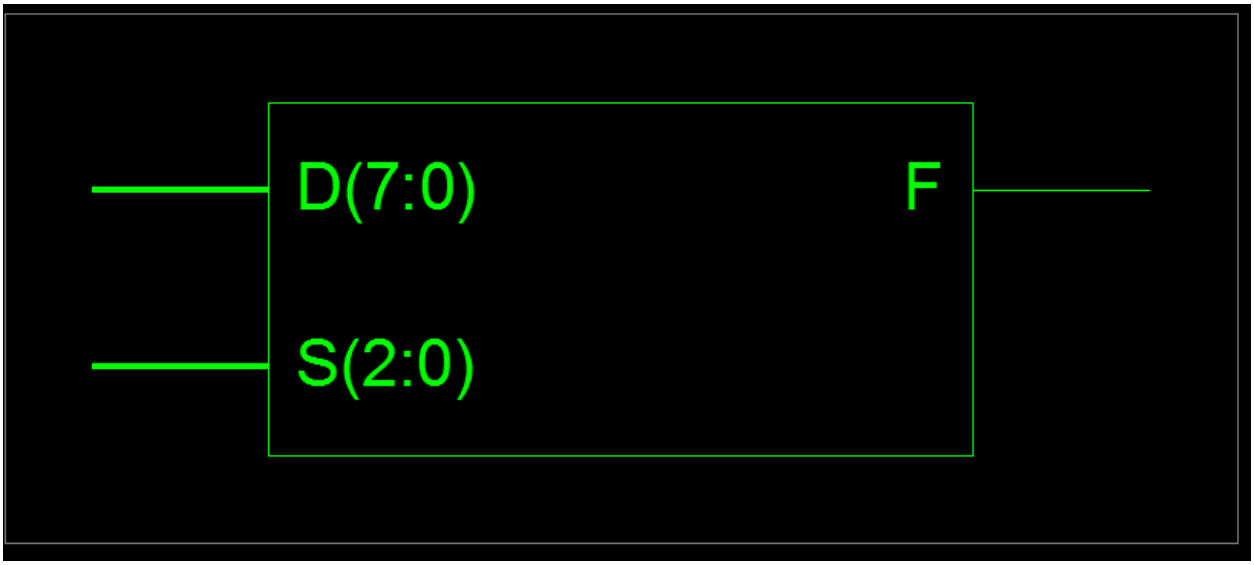

Current Simulation Time: 1000 ns
200.0
0
100
200
300
400
F
D[3:0]
D[3]
D[2]
D[1]
D[0]
S[1:0]
S[1]
S[0]
4'h0
4'hF
2'h0
2'h3

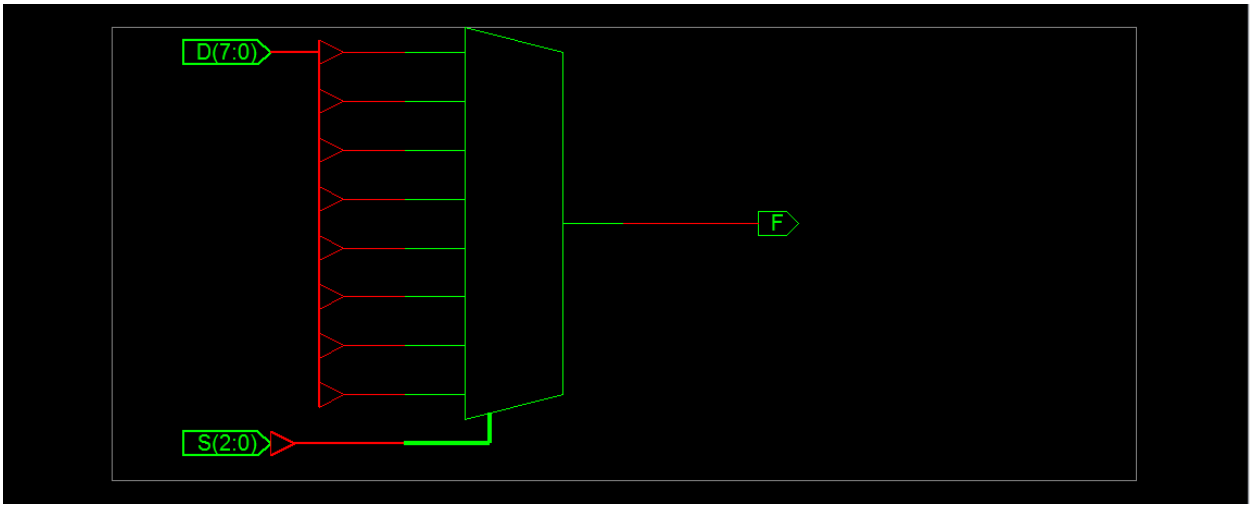
8:1 MUX: SOURCE CODE:

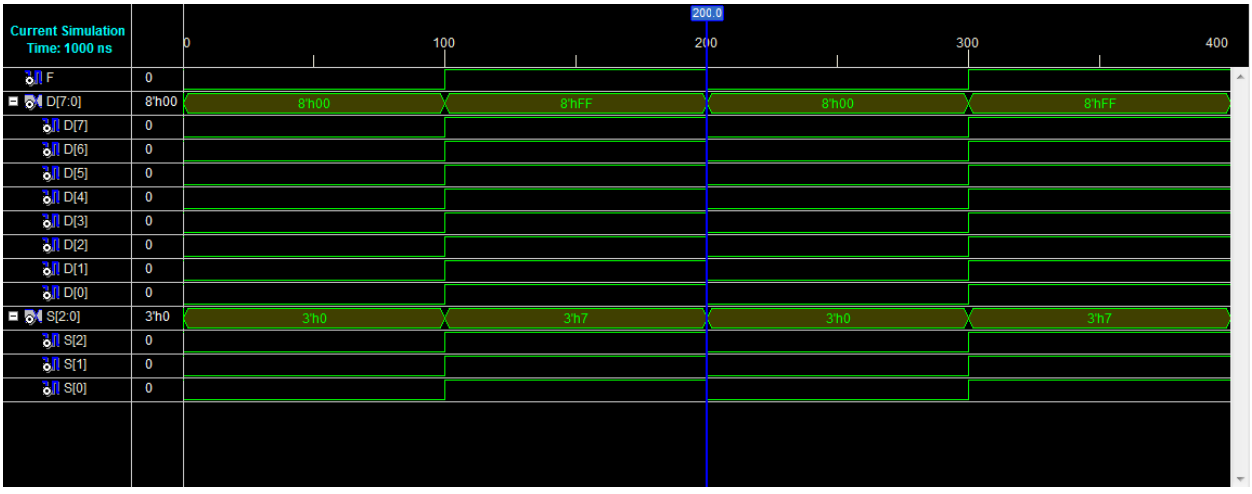
```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    20:44:46 08/20/2011
-- Design Name:
-- Module Name:    MUX22 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
```

```
entity MUX22 is
   Port ( D : in  STD_LOGIC_VECTOR (7 downto 0);
          S : in  STD_LOGIC_VECTOR (2 downto 0);
          F : out  STD_LOGIC);
end MUX22;

architecture Behavioral of MUX22 is
begin
WITH  S SELECT
F<= D(0) WHEN "000",
             D(1) WHEN "001",
              D(2) WHEN "010",
              D(3) WHEN "011",
              D(4) WHEN "100",
              D(5) WHEN "101",
              D(6) WHEN "110",
              D(7) WHEN OTHERS;

end Behavioral;
```

OUTPUT:


D(7:0)
F
S(2:0)


D(7:0)
F
S(2:0)


Current Simulation Time: 1000 ns
200.0
0
100
200
300
400
F
D[7:0]
8'h00
8'hFF
8'h00
8'hFF
D[7]
D[6]
D[5]
D[4]
D[3]
D[2]
D[1]
D[0]
S[2:0]
3'h0
3'h7
3'h0
3'h7
S[2]
S[1]
S[0]