--8 Mhz passband frequency response

din\_8Mhz: process

begin

wait for 12.5 ns;

d <= std\_logic\_vector(to\_signed(0,20));

wait for 12.5 ns;

d <= std\_logic\_vector(to\_signed(308168,20));

wait for 12.5 ns;

d <= std\_logic\_vector(to\_signed(498627,20));

wait for 12.5 ns;

d <= std\_logic\_vector(to\_signed(498627,20));

wait for 12.5 ns;

d <= std\_logic\_vector(to\_signed(308168,20));

wait for 12.5 ns;

d <= std\_logic\_vector(to\_signed(0,20));

wait for 12.5 ns;

d <= std\_logic\_vector(to\_signed(-308168,20));

wait for 12.5 ns;

d <= std\_logic\_vector(to\_signed(-498627,20));

wait for 12.5 ns;

d <= std\_logic\_vector(to\_signed(-498627,20));

end process;

-- --16 Mhz passband frequency response

-- din\_16Mhz: process

-- begin

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(0,20));

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(498627,20));

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(308168,20));

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(-30816,20));

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(-498627,20));

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(0,20));

-- end process;

-- --24 Mhz passband frequency response

-- din\_24Mhz: process

-- begin

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(0,20));

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(498627,20));

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(308168,20));

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(-30816,20));

-- end process;

process(clk)

begin

if rising\_edge(clk) then

temp<=temp+1;

if (temp="100") then

temp1<=not temp1;

elsif (temp="101") then

temp1<=not temp1;

temp<="001";

end if;

end if;

end process;

ce\_r<=temp1;