CSCE 4114 Embedded Systems
Homework #4
Due October 9th 2024
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You are given a set of requirements for building an SoC system. The requirements include the use of an A/D converter set up for a range of -7V to +7V and a precision of 12 bits. The ADC will be running from the systems 10 Mhz clock (sample period 100nsecs).

1. What is the range of digital values produced by the ADC (Hint: assume the digital values are in two's complement form)?
    a. −2^11 to 2^11−1
2. What is the size of the conversion interval (in volts) ?
    a. ***7V – (-7V) / 4096 = 0.00342V***
3. What is the quantization error (in volts)?
    a. Quantization Error=0.00342V/2 = +-0.00171V
4. You were later told that the quantization error must be less that ±.5 millivolts. Will this A/D with 12 bit precision work ? If not what is the minimum precision you would need ?
    a. Conversion Interval = Total Voltage Range / 2^N
    b. Quantization Error = Conversion Interval / 2
    c. Quantization Error = Total Voltage Range / 2^n+1
    d. 14V/2^N+1 <= 0.0005V
    e. Solve For N
    f. N >= 13.78 Round up
    g. N equivalent to 14
    h. The Minimum resolution needed would be approximately 14 bits, therefore the 12 bit A/C would not work
5. You were then told that in addition to the needed ±.5 millivolt quantization error, the input voltage range would need to be adjusted to -10v to +10 volts. For this new requirement what is the minimum precision you would need?
    a. 20V/2^N+1 <= 0.0005V
    b. Solve For N
    c. N >= 14.29
    d. N equivalent to 15
    e. Need a 15 bit A/D converter

As per usual the specs you were given didn't stipulate the type of ADC converter to use, so you are free to pick either a flash or successive approximation ADC (money is no object).

6. How many clock cycles does the flash take to convert the analog signal?
    a. 1 Clock Cycle

7. According to the Nyquist rate, what is the maximum highest signal frequency the flash can convert?
    a. Fmax = Clock Signal/2
8. For the original 12 bit A/D, how many clock cycles would an SA take to convert the analog signal?
    a. 12 clock cycles
9. Remember the SA must use a sample and hold circuit. What is the hold time (in nsecs) for correct operation?
    a. ***Hold = 1/Clock Freq***
    b. ***Hold = 12/f_{clk}***
        i. ***Multiply f_{clk} by 10^9 if it is in HZ form.***
10. Again according to the Nyquist rate, what is the maximum highest signal frequency the SA can convert?
    a. ***(Input Frequency/2)/(Number of Clock Cycles)***
        i. ***Num Clock Cycles = Num Bits of Frequency***