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Homework 4

**You are given a set of requirements for building an SoC system. The requirements include the use of an A/D converter set up for a range of -7V to +7V and a precision of 12 bits. The ADC will be running from the systems 10 Mhz clock (sample period 100nsecs).**

1. What is the range of digital values produced by the ADC (Hint: assume the digital values are in two's complement form)?
   Precision of 12 bits:
   -2^11 to 2^11 - 1

2. What is the size of the conversion interval (in volts)?
   (7V - (-7V))/(2^12) = 0.00342 V

3. What is the quantization error (in volts)?
   (7V - (-7V))/(2^(12+1)) or interval/2 = +/- 0.00171 V

4. You were later told that the quantization error must be less that ±.5 millivolts. Will this A/D with 12 bit precision work ? If not what is the minimum precision you would need?
   0.00171 V = 1.71 millivolts; this will not work!
   If we need .5 then with the same voltage…
   14 V/(2^(n+1)) = 0.0005 V
   14 V/0.0005V = 2^(n+1)
   ceil($\log_2$(28,000)) = n + 1
   15 = n + 1
   N = 14 bits of precision

5. You were then told that in addition to the needed ±.5 millivolt quantization error, the input voltage range would need to be adjusted to -10v to +10 volts. For this new requirement what is the minimum precision you would need?
   If we need .5 then with the new voltage…
   20 V/(2^(n+1)) = 0.0005 V
   20 V/0.0005V = 2^(n+1)
   ceil($\log_2$(40,000)) = n + 1
   16 = n + 1
   N = 15 bits of precision

**As per usual the specs you were given didn't stipulate the type of ADC converter to use, so you are free to pick either a flash or successive approximation ADC (money is no object).**

6. How many clock cycles does the flash take to convert the analog signal?
   1 clock cycle

7. According to the Nyquist rate, what is the maximum highest signal frequency the flash can convert?
   clock frequency/2

8. For the original 10 bit A/D, how many clock cycles would an SA take to convert the analog signal?
   10 clock cycles (1 for each bit)

9. Remember the SA must use a sample and hold circuit. What is the hold time (in nsecs) for correct operation?
   Hold time = # bits * 1/clock frequency = $10/f_{clk}$ or $10^9 * 10/f_{clk}$ if frequency is given in Hz

10. Again according to the Nyquist rate, what is the maximum highest signal frequency the SA can convert?
    (Input frequency/2)/(# of clock cycles) where # of clock cycles = # of bits of frequency