COMP4300 Spring 2023
Homework 2

Suppose you are designing a cache for a machine with 20-bit addresses. The cache is 32K in size. Cache blocks are 64 bytes. (15points each part)

a. How many blocks can be held in the cache.
32K / 2^10 = 32768/1024 =31.25 bytes
32768 bytes /64 bytes = 512

b. How many bits of the address are devoted to the offset?
512 block/cache
2^9 => 9 bit offset

c. If the cache is direct-mapped, how many bits are devoted to the tag and index?
512 blocks/cache
2^9 => 9 bit index
11 bit tag

d. If the cache is 2-way set associative, how many bits are devoted to the tag and index? How many sets are there?
2 way set associative
2 block/set
64/2= 32 sets => 2^5 sets => 5 bit index
7 bit tag

e. If the cache is fully associative, how many bits are devoted to the tag and index?

No index
20 bit tag

2. (25points) Suppose you have a machine with separate I- and D-caches. The miss rate **per memory access** on the I-cache is 2%, and on the D-cache 3%. On an I-cache hit, the value can be read in the same cycle the data is requested. On a D-cache hit, one additional cycle is required to read the value. The miss penalty is 100 cycles for either cache. 35% of the instructions on this RISC machine are LW or SW instructions, the only access data memory. A cycle is 2ns. What is the average memory access time per instruction (in nanoseconds)?

I-cache
Hit = 2 cycle
Miss rate = 2%
Miss penalty = 100 cycles
Average = 0.02/2 = 0.01

D-cache
Hit = 3 cycle
Miss rate = 3%
Miss pentalty = 100 cycles
35% load/store
Average = 0.03/0.35 = 0.0857

((1/1.35) *(2+0.02(100)) + (0.035/1.35)(3 + 0.03(100)) = 3.1185 cycles * 2ns/cycles = 6.237 ns