COMP4300

Lab Exercise Four

Objective

This lab implements the control of the Aubie processor and simulates executing entire instructions.

Instructions

Fill in the VHDL for the states of the controller entity so that the processor interprets and executes instructions consistent with the documents "AUBIE CPU SPECIFICATION v2" and "SEMANTICS OF AUBIE PROCESSOR INSTRUCTIONS." Your project will contain six files: dlx_types.vhd, bva.vhd, bva_b.vhd, interconnect_aubie.vhd, datapath_aubie_v1.vhd, and control_aubie_v1.vhd. The diagram aubie_datapath.jpg is a visualization of the datapath. (if corrections are needed to the provided files, the version numbers will be incremented and new versions uploaded to Canvas, and an announcement will be made on Canvas).

The VHDL code for the memory already has two instructions stored in addresses zero, one, and two. If you can simulate the correct functioning of these two instructions you will get full points for the lab. If you wish to implement further instructions, there is extra credit for them

JMP and JZ implemented and tested: 50 points

LDR and STOR implemented and tested: 50 points

STO implemented: 25 points

Deliverables

Please turn in the following things for this lab:

- All your VHDL code.
- Your simulation test file. Do not exhaustively test these designs since they take lots of input bits, but do test a reasonable number of things. For example, for the ALU, be sure to test every function, and for those that generate error codes, test the error conditions.
- Transcripts/screenshots of tests running your simulations. You cannot test exhaustively, but you should demonstrate that all your modules work.
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Please turn in all files on Canvas as a single zip file. If I have questions, I may ask you to schedule a time to demo your code, if I can't figure out how something works by reading the code.