COMP4300

Lab Exercise One, FA23

Objective

This lab is aimed at getting you familiar with using the ModelSim simulator. This lab requires you to implement a single combinational logic gate with 3 inputs and one output.

Instructions

Write a VHDL program consisting of a single entity whose architecture is a single process that implements a 3-input even parity gate. That is, a circuit which behaves as specified in the following truth table. You should implement your architecture as a single process.

inputs			outputs
a_in	b_in	c_in	result
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Use exactly the names given above for the signals. All your signals should be of type `bit` (NOT integer).

Deliverables

Please turn in the following things for this lab:

- The file with your VHDL code.
- A screen shot of your exhaustive simulation (8 cases)
- A screen shot of a successful compilation of your code.