COMP4300 Spring 2023
Homework 2

1. Suppose you are designing a cache for a machine with 20-bit addresses. The cache is 32K in size. Cache blocks are 64 bytes. (15 points each part)
    a. How many blocks can be held in the cache

    b. How many bits of the address are devoted to the offset?

    c. If the cache is direct-mapped, how many bits are devoted to the tag and index?

    d. If the cache is 2-way set associative, how many bits are devoted to the tag and index? How many sets are there?

    e. If the cache is fully associative, how many bits are devoted to the tag and index?

2. (25 points) Suppose you have a machine with separate I- and D- caches. The miss rate **per memory access** on the I-cache is 2%, and on the D-cache 3%. On an I-cache hit, the value can be read in the same cycle the data is requested. On a D-cache hit, one additional cycle is required to read the value. The miss penalty is 100 cycles for either cache. 35% of the instructions on this RISC machine are LW or SW instructions, the only instructions that access data memory. A cycle is 2ns. What is the average memory access time per instruction (in nanoseconds) ?