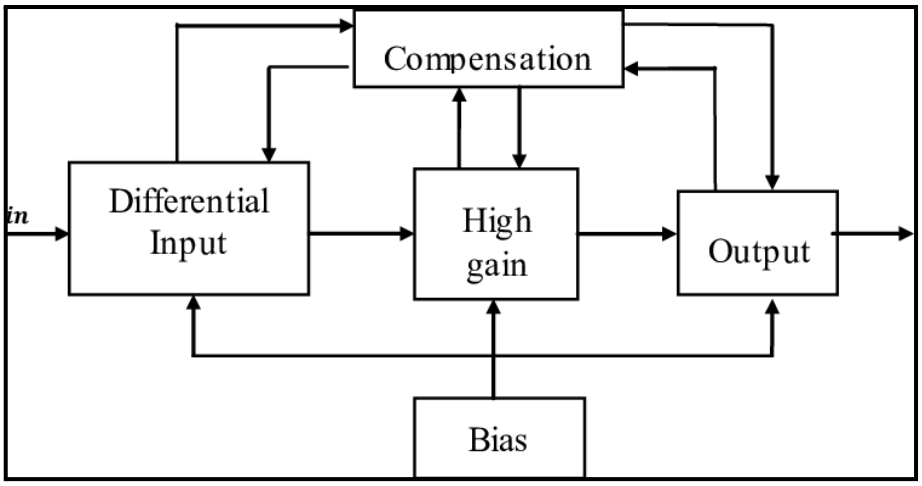
TWO STAGE OPERATIONAL AMPLIFIER

AIM: Following are the specifications for designing the amplifier

i. Process = 0.18 µm
ii. Leff = 0.5 µm
iii. VDD = 1.8 V
iv. VSS = 0 V
v. Slew Rate = 20 V/µsec
vi. Product of gain and bandwidth (GBW) = 30 MHz
vii. Load capacitance = 2 pF
viii. $ICMR^{+}$ = 1.6 V
ix. $ICMR^{-}$ = 0.8 V
x. Max Power Dissipation: 300uW
xi. Phase Margin ≥ 60°

THEORY:

The operational amplifier (Op-amp) is one of the most beneficial gadgets in electronic industry. Op-amps are used extensively for signal conditioning, filtering and for execution of mathematical operations. Op-amp is basically a differential amplifier and the output signal is nothing but the difference of the two input signals implemented at the excessive impedance terminals magnified by using a steady benefit. The design of Op-amps basically considers supply voltage and channel lengths of transistor in the era of CMOS technology with trade-off among velocity, energy, gain and some other parameters which signifies the performance. Nowadays, high gain in Op-amp is used for various applications and also optimizing various parameters has become mandatory, which results in increase in slew rate for increase in current.



Block Diagram for a practical Operational Amplifier

Op-amps are the spine for the design of analog circuits, and performance relies on data transmission and DC gain. The symbolic representation of a 2 stage Op-amp is shown in the above Figure.

The principal part of an Op-amp is the differential amplifier which has two inputs i.e. inverting and non-inverting voltages which results in yielding of differential voltage or current.

The next block is used to change the differential sign produced by the main square into a solitary finished adaptation. Much of the time the increase given by the information stages isn't adequate and extra enhancement is required which is produced by the intermediate stage.

A. Two Stage amp For MOSFET we have **several basic technology parameters** including

$$i_D = \frac{1}{2}k_n(\frac{W}{L})(V_{GS} - V_{TN})^2$$

$$g_m = \sqrt{2k_n(\frac{W}{L})} \cdot \sqrt{I_D}$$

kn = 350μA/V² and kp = 70μA/V² for our case using TSMC 180nm

B. Gain, Poles and zeros.

We define the input Vin, the output voltage of the first stage
i.e. the input voltage of the second stage V1, and the output voltage of the whole circuit Vout, so we can get that for two stage operational amplifier we have

$$\frac{V_{out}}{V_n} = \frac{V_{out}}{V_1} \times \frac{V_1}{V_{in}}$$

so, we can calculate the voltage gain of two stage separately and then combine together. We set the output resistance of the first stage Ro2 || Ro4 as R1 and the output resistance of the second stage Ro6 || Ro7 as R2. We also se the output capacitance of the first stage as C1 ,output capacitance C2 ≈ CL for the second stage and Miller capacitance C_c. So we finallyget that

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}R_1 \times g_{m2}R_2 \times (1 - \frac{sC_c}{g_{m2}})}{as^2 + bs + 1}$$

$a=R_1R_2(C_1C_2+C_1C_L+C_2C_L)$

$$b = R_2(C_c + C_2) + R_1(C_c + C_1) + C_c g_{m2} R_1 R_2$$

$$g_{m1} = \sqrt{2K_p(\frac{W}{L})_1 I_{D1}}$$

$$g_{m2} = \sqrt{2K_n(\frac{W}{L})_6 I_{D6}}$$

to find the poles and zeros, we must transform the equation into form like

$$A_{dc} = g_{m1}R_1 \times g_{m2}R_2$$

the zero point of the circuit

$$z_1 = \frac{g_{m2}}{C_c}$$

When it comes to the poles of the circiut, approximately we have

$$p_1 \approx \frac{1}{b}$$

we can simply it to

$$p_1 \approx \frac{1}{C_c g_{m2} R_1 R_2}$$

for another pole p2 we have

$$p_2 \approx \frac{g_{m2}C_c}{C_1C_2 + C_1C_L + C_2C_L}$$

C1 is very small so we can simply it into

$$p_2 \approx \frac{g_{m2}}{C_1 + C_2}$$

C. **Gain bandwidth,** GBW is equal to DCgain × p1 = gm1/Cc

D. Phase Margin:

Phase at GBW is

$$\angle\frac{V_{out}}{V_{in}} = -\arctan(\frac{\omega}{z}) - \arctan(\frac{\omega}{p_1}) - \arctan(\frac{\omega}{p_2})$$

and we have

$$z = 10 \times GBW$$

$$\angle\frac{V_{out}}{V_{in}} = -\arctan(\frac{GBW}{z})-\arctan(\frac{GBW}{p_1})-\arctan(\frac{GBW}{p_2})$$

so

$$\angle\frac{V_{out}}{V_{in}} = -\arctan(\frac{1}{10}) - \arctan(A_{DC}) - \arctan(\frac{GBW}{p_2})$$

then we need p2 > 2.2GBW and finally Cc > 0.22CL to get more than 60^0 phase margin. Thus we also have

$$Z=10 \text{ X } GBW$$

$$\text{so, } gm_2 / C_c = 10(gm_1 / C_c)$$

$$\text{so, } gm_2 = 10gm_1$$

$$p2 > 2.2GBW$$

$$\text{so, } gm_2 / C_2 > 2.2 \text{ X } (gm_1 / C_c)$$

$$\text{so, } C_c > 0.22\ C_2$$

E. **Slew Rate** In our design, the slew rate is just equal to

$$SR = I_0/C_c$$

we already have I_0 = 20μA so Cc must be > 440fF, which is certain to full-fill. Herewe need to obtain 20V /us slew rate.

Circuit Diagram:

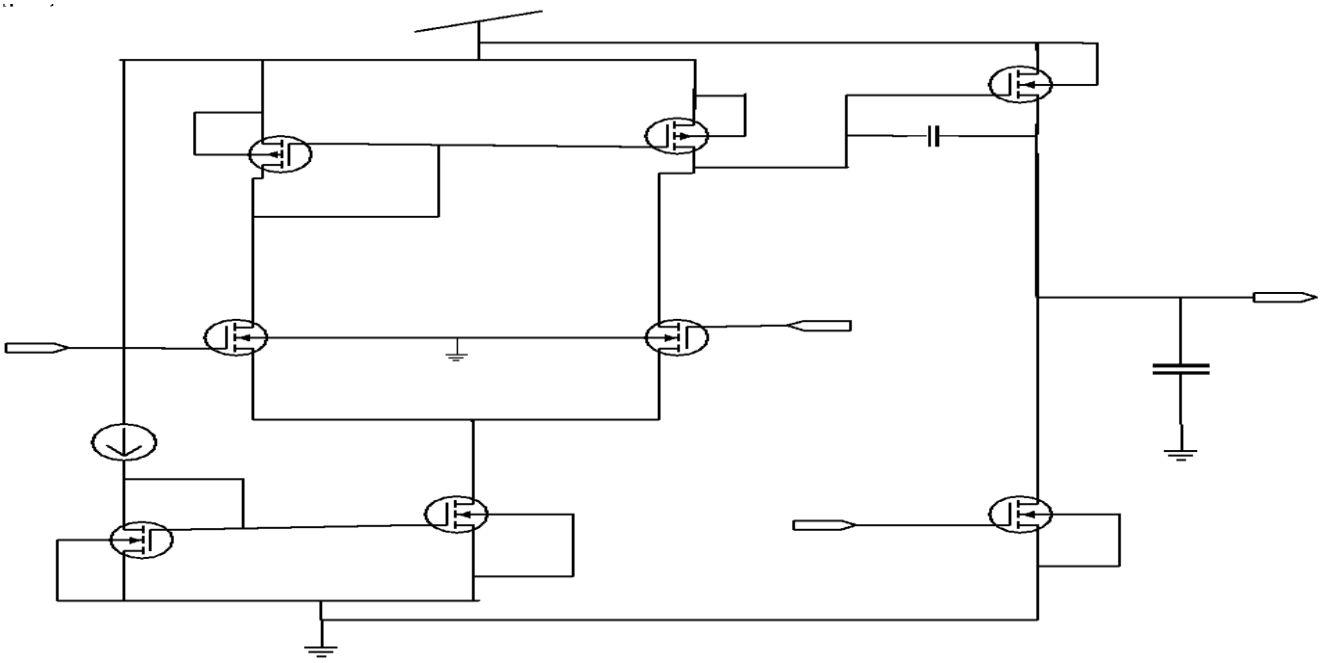


Fig. 4 *Circuit for a practical Operational Amplifier*

Fig. 4 is equivalent to a typical CMOS Op-amp, includes three subsections: differential gain stage with next gain stage and bias stage. The primary phase of Op-amp, the differential amplifier, is made up with transistors M1, M2, M3, and M4. This is basically a current mirror (CM) with active type of load utilized here. The second stage used to deliver high gain to the amplifier and made up with of transistors M6 and M7. The biasing circuit stage of amplifier is accomplished with transistors M5, M6,M7,M8.

Design Procedure:

The following equations are drawn up to design the Op-amp :-

$$\text{Slew Rate , } SR = \frac{I0}{C_c} \qquad \ldots\ldots\ldots\ldots\ldots(1)$$

$$\text{Gain for 1st stage, } Av_1 = \frac{gm_2}{gds_2 + gds_3} \qquad \ldots\ldots\ldots\ldots\ldots(2)$$

$$\text{Gain for 2nd stage, } Av_2 = \frac{gm_5}{gds_5 + gds_7} \qquad \ldots\ldots\ldots\ldots\ldots(3)$$

$$\text{Gain Bandwidth, GBW} = \frac{gm_1}{C_c \times 2\pi} \qquad \ldots\ldots\ldots\ldots\ldots(4)$$

Designing of M1,M2:

From equation (1) we get , I_0 = 20uA (Where C_c= 500fF & $C_c \geq 0.22C_L$)
From equation (4) we get, gm_1= 160uA (Where C_c= 800fF & $C_c \geq 0.22C_L$)

Now we know, $(W/L)_{1,2} = \frac{gm^2}{2I_D\mu_n C_{ox}}$

Putting the values we get ***$(W/L)_{1,2} = 5$***

Designing of M3,M4:

From dc analysis calculations we get, $Vth_{1(min)}$ = 0.56 V $Vth_{1(max)}$ = 0.74 V $Vth_{3(max)}$ = 0.525V

By analyzing the differential amplifier we get,

$$ICMR^+ \leq Vds_{1(min)} + Vth_{1(min)} \ldots\ldots\ldots\ldots\ldots (1)$$

$$\text{Where } Vds_1 = V_{DD} - \sqrt{\frac{2I_3}{\beta_3}} - Vth_{3(max)}$$

From these values,

$$(W/L)_{3,4} = \frac{2I_3}{\mu_p C_{ox}[V_{DD} - ICMR^+ - Vth_{3(max)} + Vth_{1(min)}]^2}$$

Hence, ***$(W/L)_{3,4} = 6$***

By analyzing M1 and M0 we get,

$$ICMR^- = Vgs_{1(max)} + Vdsat_5$$

$$\text{Where } Vgs_{1(max)} = \left[\sqrt{\frac{2I_1}{\beta_1}}\right] + Vth_{1(max)}$$

$$\text{From these we get, } Vdsat_5 = ICMR^- - \left[\sqrt{\frac{2I_1}{\beta_1}}\right] - Vth_{1(max)}$$

Now we know, $(W/L)_{5,8} = \frac{2I_{D5}}{\mu_n C_{ox} V_{dsat5}}$

Putting the values we get ***$(W/L)_{5,8} = 5$***

Designing of M6:

$$(W/L)_6 / (W/L)_4 = gm_6 / gm_4$$

$$gm_4 = 91.65u,\ gm_6 = 10 * gm_1 = 1600u$$

Putting the values we get ***$(W/L)_6 = 105$***

Designing of M7:

$$(W/L)_6 / (W/L)_4 = I_6 / I_4$$

$$I_6 = 175uA$$

$$(W/L)_7 / (W/L)_5 = I_6 / I_5$$

Putting the values we get ***$(W/L)_7 = 44$***

Power Requirement Exceeding 300uW, So tweaking few parameters to get power <300uW

Few changes Done: $(W/L)_{3,4} = 8$, $I_6 = 125uA$, $(W/L)_7 = 30$

<u>Final Design :</u>

$(W/L)_{1,2} = 5$, $(W/L)_{3,4} = 8$, : $(W/L)_{5,8} = 5$, : $(W/L)_6 = 104$, : $(W/L)_6 = 30$

Circuit diagram:

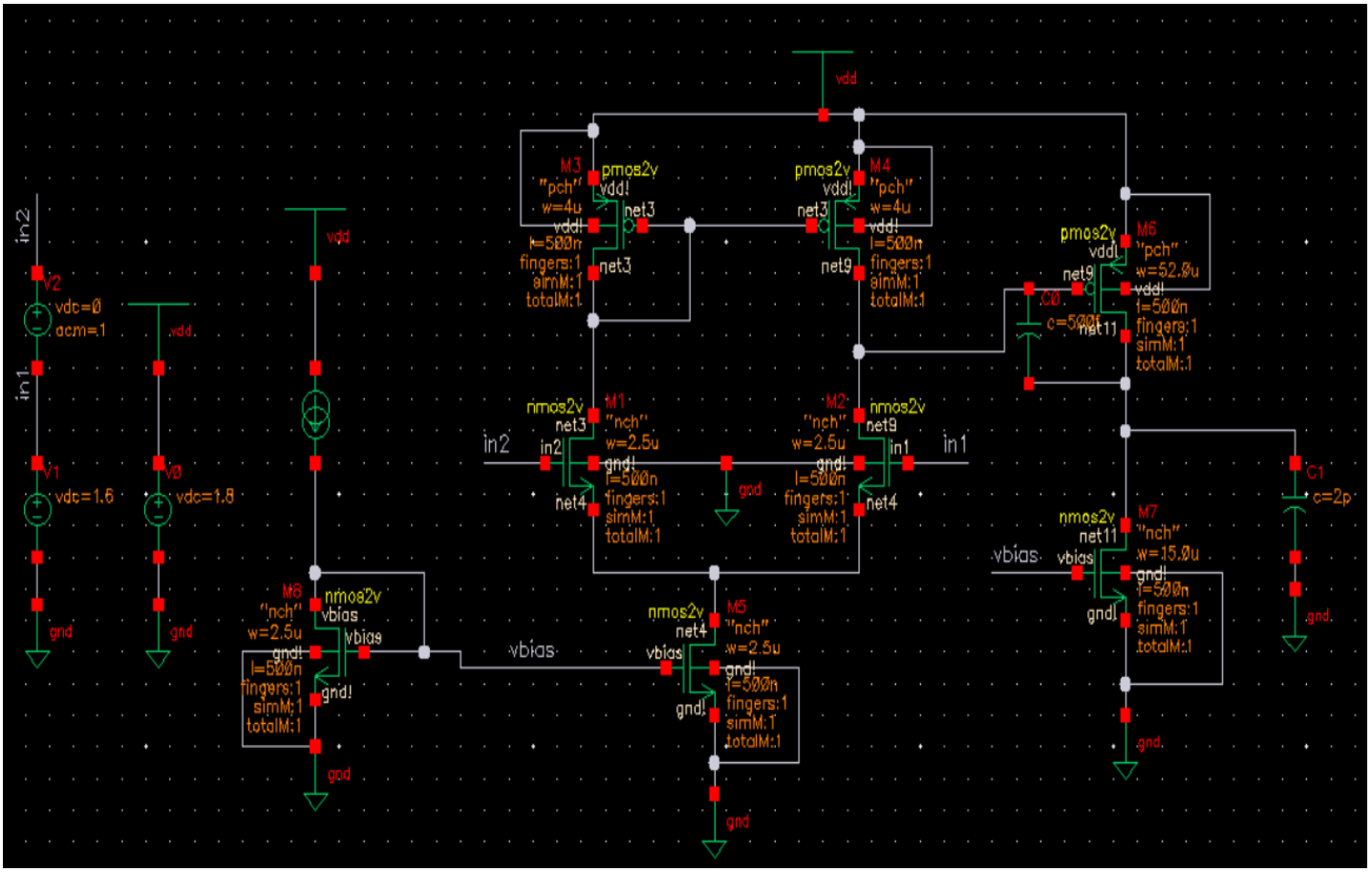


Fig. circuit diagram with aspect ratios

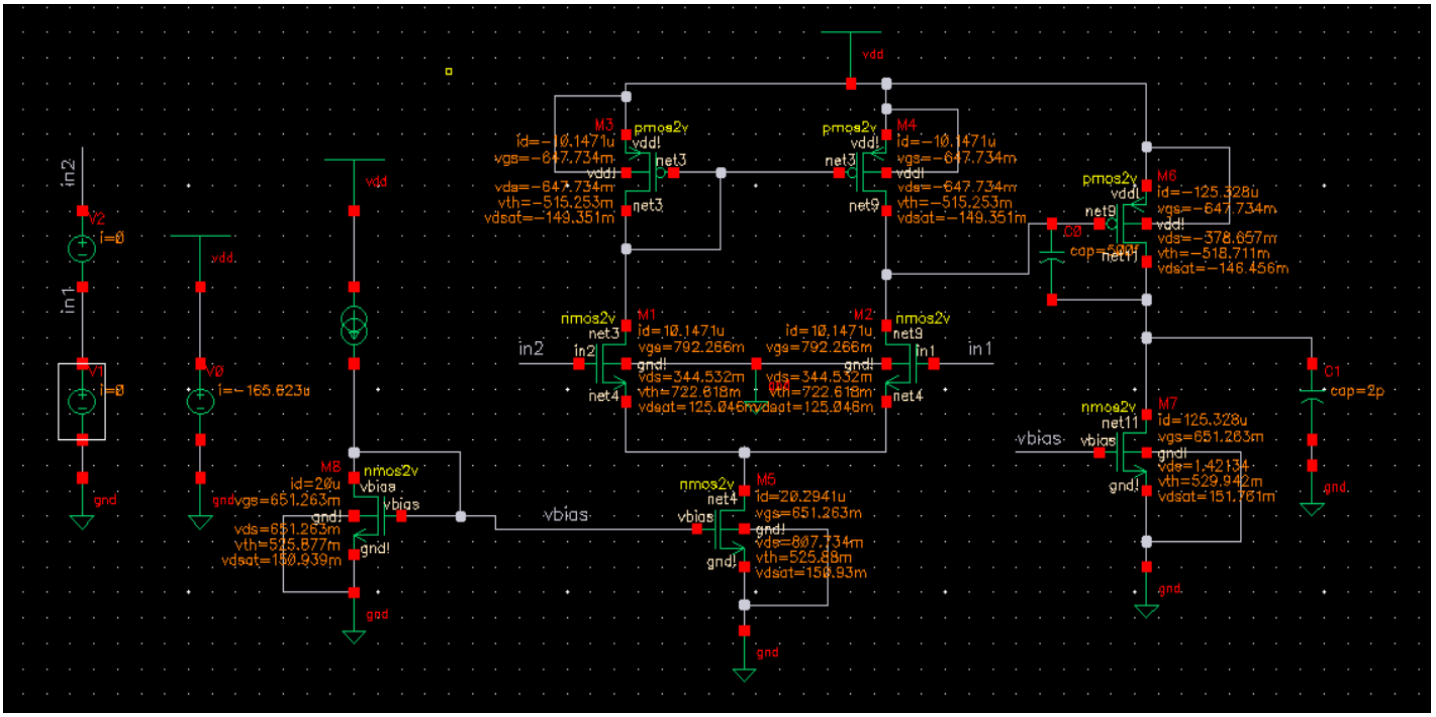


Fig. Circuit Diagram with DC operating point(VCM=1.6v)

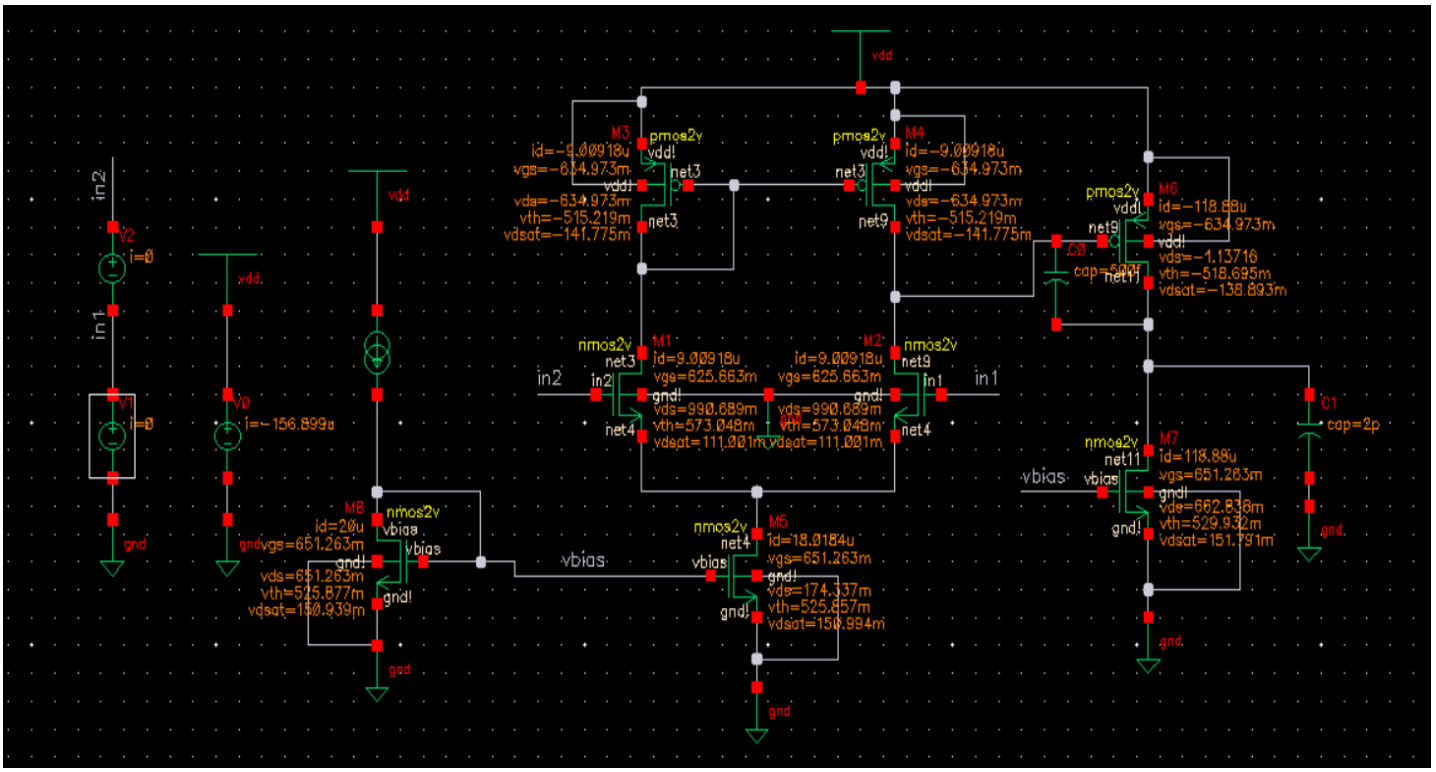
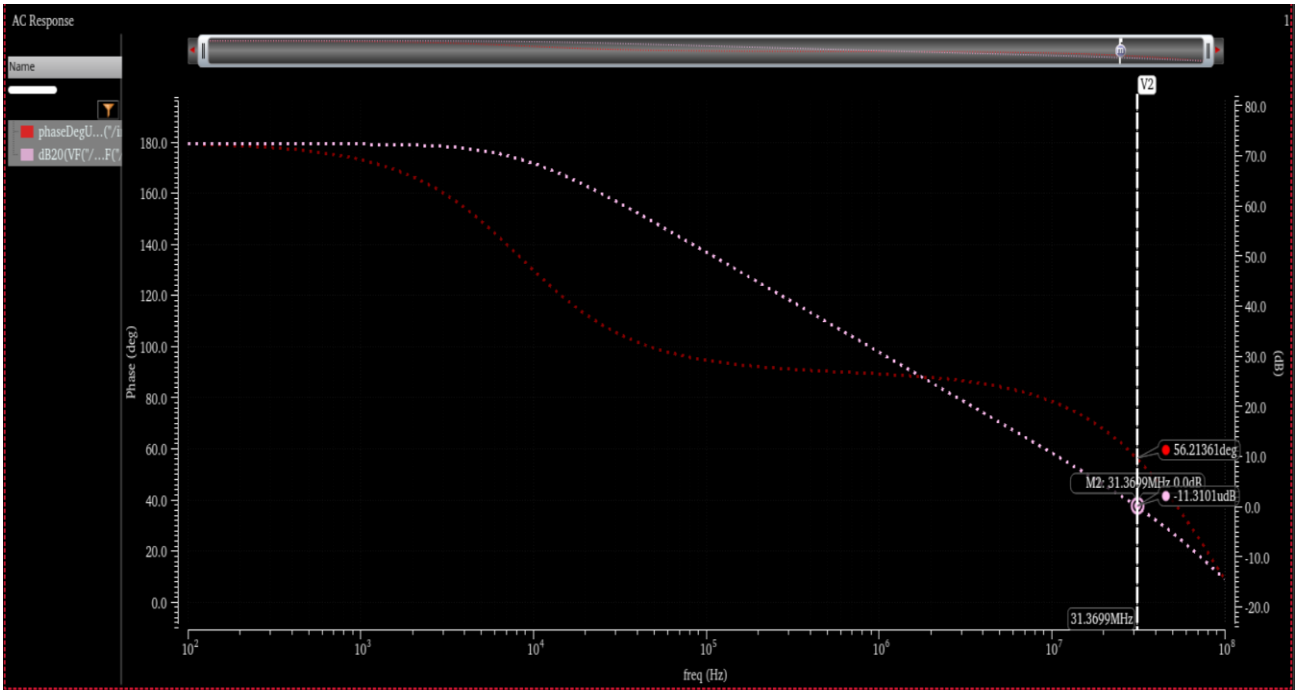
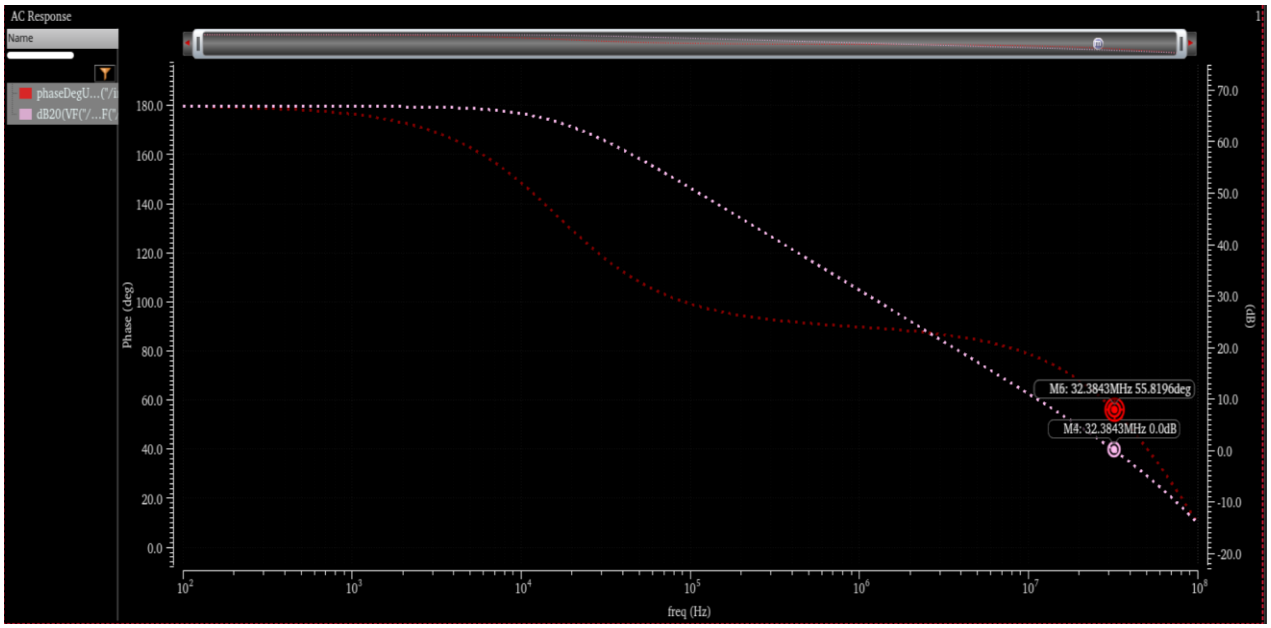


Fig. Circuit Diagram with DC operating point(VCM=0.8v)

AC Analysis (Magnitude & Phase Plot) of the designed Op-amp:



VCM=0.8V, Gain=72dB, GBW=31.36MHz, PM=56.21degree



VCM=1.6v Gain=66.81dB, GBW=32.384MHz, PM=55.8degree

Conclusion:-

1. We have successfully designed a Two stage Op-amp and achieved a Gain ofabove 60 dB, GBW of around 32 MHz and a Phase Margin of around 56°.
2. For a stable system Phase Margin should be closer to 60^0, otherwise there might be oscillations and the system will need some time to settle; we have considered this fact while calculating the (W/L) ratios of all the Transistors.
3. We have compensated the Op-amp by Miller Compensation technique so that below UGF the system can behave like an one pole system and we have compensated/minimized the effect of one pole by adding Rz so that our overall Phase Margin improves.
4. We have considered a current of 20uA as our reference current and Cc = 0.5 pF so our Slew Rate = 40 V/us (which is greater than the given specification 20V/us). We have considered a higher Slew Rate so our (W/L) ratios become significantly higher.
5. Power Requirement Exceeding 300uW. So, tweaking few parameters to get power <300uW. We have kept L = 0.5um throughout our design to avoid the second order effects coming due to short-channel.