Automotive Low Power Technology for IoT Society

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Abstract

This paper addresses automotive low power technologies in Internet of Things (IoT) societies, where the interaction among cloud information, real-time recognition and vehicle control is a key. High reliability and high performance with low power under the harsh operating conditions are strongly demanded for automotive microcontroller units (MCUs). Our developed embedded Flash (eFlash) and SRAM achieved those required performance at up to Tj=170°C mainly for the vehicle control solution. To perform the highly robust computation in car information applications, the power management involving adaptive voltage scaling and real time power saving are adopted. Moreover other low-power schemes such as multi core CPU system with the easier parallelism and the digitally assisted ADC are introduced.

Keywords: *High reliable embedded memory, Power management, Multi core CPU, Digitally assisted ADC.*

Introduction

In the upcoming IoT era, a huge number of devices are connected with each other. Mobile devices such as smartphones and tablets which prevail all over the world are leading the recent progress of IoT in the consumer products. Nowadays IoT technologies are being widely adopted by industrial and automotive products to establish the energy efficient society because energy consumption in emerging countries is predicted to be doubled in the next two decades. Smart meter for the electric power management and Ethernet for the industrial automation are the representative solutions.

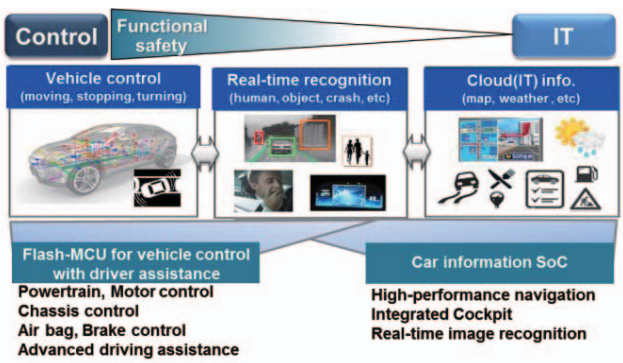

Fig. 1: Convergence of IT and control in automotive IoT.

Advanced automotive systems will interact technologies among cloud information, real-time recognition and vehicle control to pursue the higher energy efficiency, safety and comfort, as shown in Fig. 1. A single automotive has already contained lots of electrical parts, as around 100 Flash MCUs are being used for the vehicle control such as moving, stopping, and turning. High reliability, low power and intensive computation capability under the harsh operating condition are required for Flash MCUs which can execute the dedicated real-time control applications with offering the excellent on-chip programmability.

On the other hand, the driving experience that is safe, pleasant and comfortable is becoming a key for all of drivers. Navigation system, surround monitoring, real-time recognition and IT information will be integrated into the cockpit in the near future. High performance car information SoC would play an important role of IT connection and processing various applications with high-level human interface accommodating 3D graphics. Furthermore IoT society would evolve the advanced driver assistance system (ADAS) by interacting with outside world. Functional safety in vehicle control is being deployed to ADAS leading up to self-driving cars. Low power technology is essential to cope with the gate count increase caused by that safety, such as dependable CPU core and ECC.

Embedded memories for vehicle control solutions

Flash-MCUs which hold embedded Flash and SRAM are key components for vehicle control such as powertrain, chassis, brake controls and so on. Especially the powertrain applications aggressively require the large memory capacity with high reliability, high speed and low power at high temperature, up to 170°C, because regulations of CO_2 emission are continuously tightened by the governments.

Split-gate MONOS (SG-MONOS) [1], which is a split-gate memory cell with charge-trapping storage, could be one possible convergence in the automotive eFlash, as shown in Fig. 2. Split-gate cells enable fast and low power read due to the low voltage swing of word-line. Charge-trapping structure contributes to the intrinsic high data reliability because of its robustness against the point defect. Moreover its low cell profile assures the better compatibility with fine CMOS logic process, compared with the floating gate type.

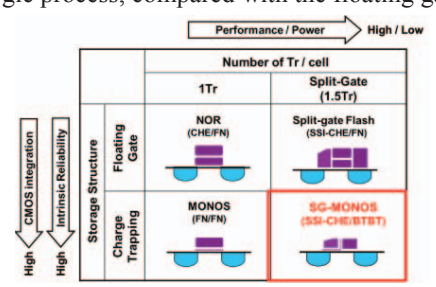

Fig. 2: Superiority of SG-MONOS among eFlash candidates.

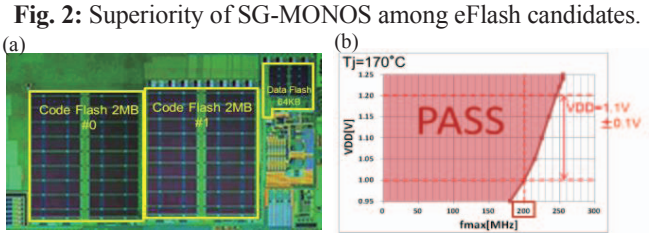

Fig. 3: 28nm SG-MONOS [2] (a) Photo (b) Read shmoo plot.

In fact, the world's first 28nm eFlash macro by using SG-MONOS has been successfully demonstrated for the high-end automotive applications [2]. In this work, the fastest random read of 200MHz for code Flash and over 1M program and erase cycles for data Flash are achieved. Figs. 3 (a) and (b) show the microphotograph of 28nm eFlash macro and its read shmoo plot, respectively.

Developed embedded SRAM for the vehicle control ensured sufficient static-noise-margin (SNM) and lower leakage power at Tj=170°C by optimizing the bitcell design within 10% area overhead. SNM was improved by 40% and the leakage power was reduced by 90%. Moreover about 80% smaller sleep current at Tj=170°C is achieved by employing the floating bit-line and the raised VSS schemes with the lowered VDD of memory cell. For the robust operation, the weak retention bit can be effectively screened by the dedicated test circuits in which bit line pairs discharged to VSS could flip the weak bit cell [3].

Low power technology for car information SoC

The car information system needs much higher performance

for real-time image recognition at higher temperature than mobile system. Fig. 4 shows the trend of high-end car information system and a die photo of the 2nd generation R-Car (H2) in 28nm. H2 is the world-wide first commercial octal-core processor for automotive applications. An adaptive voltage scaling (AVS) and a power gating are introduced to reduce the leakage power [4, 5]. Fig. 5 (a) shows two types of AVS system in H2. The open-loop AVS sets the optimum voltage in accordance with the process variation monitored by the probing test. The closed-loop AVS dynamically controls the voltage level of PMIC output power supply with thermal and delay sensors near/in the CPU region. Power gating with IO NMOS footer switch contributes to high reliability as well as low standby power, ensuring higher HCI, BTI, and electro-migration (EM) immunity [5]. Fig. 5 (b) shows leakage current of the octal-core CPU at 125°C. By shutting off high performance cores and all cores, the leakage current of CPU cores is reduced by 95.7% and 99.8%, respectively.

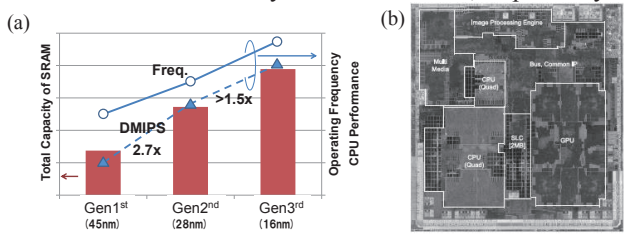

Fig. 4: Trends of infotainment system and a die photo of the 2nd generation R-Car (H2) in 28nm.

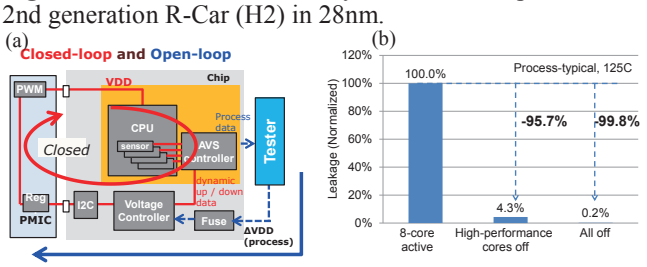

Fig. 5: Proposed AVS system and leakage reduction in CPU.

The next generation for smart-car system (Gen 3rd), is facing a limitation of the thermal headroom. The advanced FinFET technology has been adopted to overcome the limits of the planar MOSFET devices. To enhance the operating voltage range for extended AVS, SRAM V_{min} should be improved. Fig. 6 shows a 16nm FinFET SRAM with wordline over-driven read/write assist and its measured data [6]. We confirmed 0.7 V low-voltage operation and 648 ps high-speed read access, resulting in 40% power reduction.

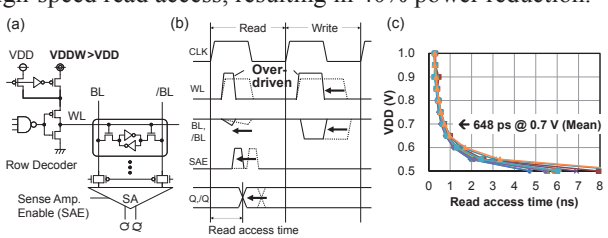

Fig. 6: 16 nm FinFET SRAM with read/write assist and measured read access time of 256-kbit SRAM at 25°C [6].

Integration of automotive technology with IT

ADAS will be aggressively evolved by integrating vehicle control and IT. For the present, automotive companies plan to add the pedestrian detection and auto-braking. Safety-relevant cognitive processing on various information through multiple vehicle-mounted sensors requires intensive computation and excellent real-time capability. In consumer applications, low power multi core CPU systems are useful to improve performance, because the task-level parallelism can be easily found. To the contrary, it's difficult to find task-level parallelism in the vehicle control application and satisfy the strict real-time requirement in the path from sensor input to processing results. Model based design is suggested that real-time processing parts should be described in special-purpose languages to analyze and extract their parallelism effectively, as shown in Fig. 7. Previous study [7] incorporating with the dedicated OS for multi core CPU can provide the easier parallelism, with achieving 5.5× higher computation performance in 8-core CPU system for engine control, compared with the single core. Thus the higher parallelism increases the computation efficiency, resulting in the low power dissipation.

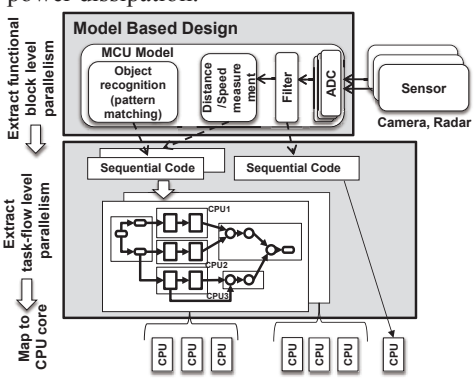

Fig. 7: Flow of extracting parallelism in cognitive system.

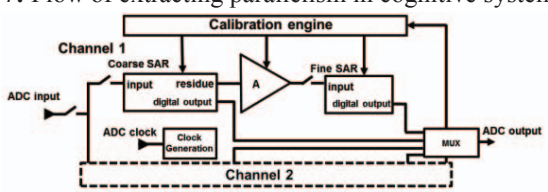

Fig. 8: Block diagram of digitally assisted ADC [8].

Digitally assisted ADC is effective for low power and fast data conversion of analog inputs from the vehicle-mounted sensors. One of the examples shown in Fig. 8 implements the calibration logic for both coarse and fine SAR ADCs and the residue amplifier [8]. The excellent area efficiency with low power can be achieved in the narrower process node, because its digital rich functions can reinforce the higher accuracy instead of analog parts.

As another aspect of IT, the real-time program updates over the air is deployed to automotive Flash-MCUs for easier maintenance. The spread spectrum phase shifted clock generation for eFlash charge pump reduces EMI noise by 19dB, resulting in the reliable in-field programming through the wireless communications [2].

Conclusion

Automotive IoT interacting between vehicle control and IT requires low power technologies to attain high speed and reliable operation under the harsh operating condition. Our 28nm SG-MONOS with the fastest 200MHz random read at 170°C is firstly demonstrated for the advanced vehicle control. Other technologies such as the extensive power management and multi core CPU with the easier parallelism also contribute to the robust computation with low power.

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