Lab 8: Up/Down Counters

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Objective:

In this lab, our objective is to write three Verilog codes that implant a up/down counter for binary, grey code, and one hot using finite state machines. In addition, will be using the FPGA board to test our counters.

Introduction:

Binary Counter: The Binary counter will be using in this lab will a 3-bit counter that goes from "000" to "111" which is 0 to 7.

Gary code: Gray Code is a binary encoding system that groups a sequence of bits so that just one bit in each group differs from the number before and after it. Will be using a 3-bit grey code counter in this lab so that we start "000" until we get "100".

One-Hot: A one-hot is a set of bits in which the only permissible value combinations are those with a single high (1) bit and all others low (0). We will be using a 8-bit one hot counter that will start "00000001" to "10000000".
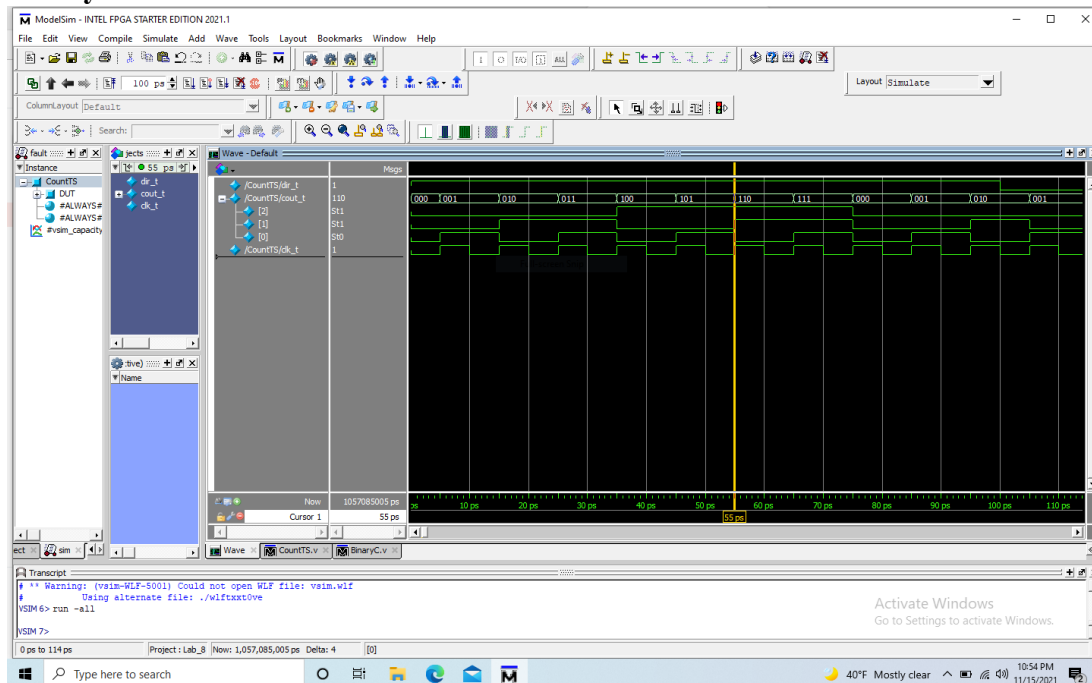
Finite state machine:

State Diagram:

State Name	Binary	Gray Code	One-Hot
S0	000	000	00000001
S1	001	001	00000010
S2	010	011	00000100
S3	011	010	00001000
S4	100	110	00010000
S5	101	111	00100000
S6	110	101	01000000
S7	111	100	10000000
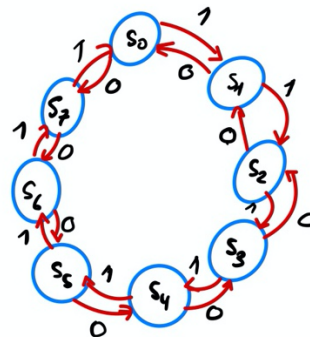
ModelSim:

Binary:

As shown in the waveform we have the binary "000" to "111" (0 to 7) and then back to zero.

Gray Code:

As shown in the waveform we have gray code that for each present bit we get a district bit from the number before and after it.

One Hot:

As shown in the waveform we have implemented a one hot counter that's starting at "00000001" to "10000000".
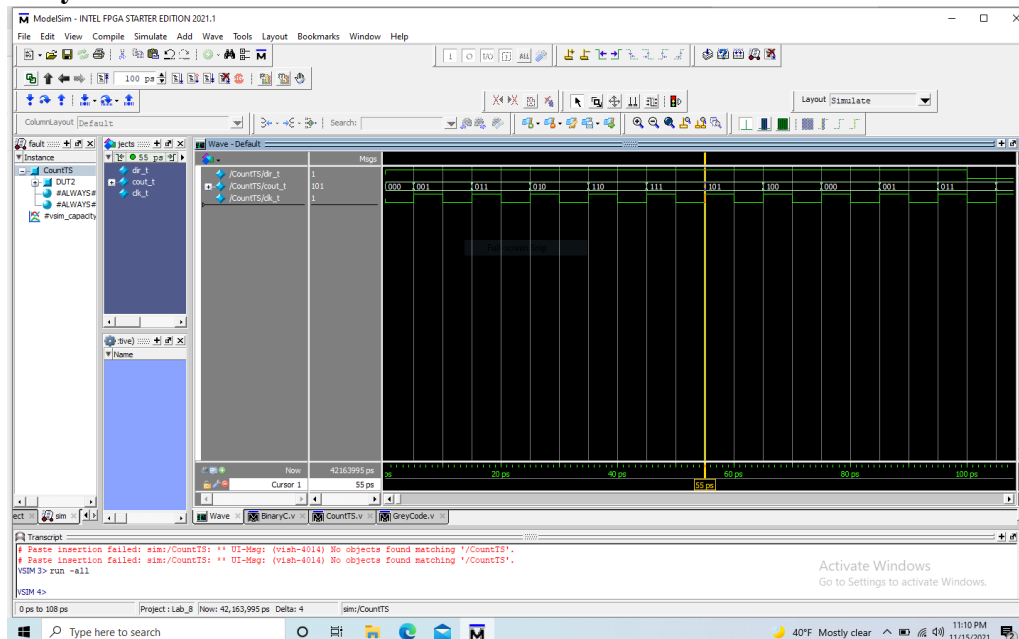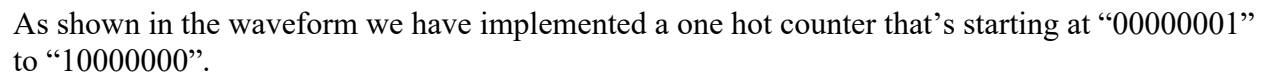
FPGA Board:

The FPGA board is running three counters at the same time, with the first eight LED lights indicating the one-hot counter. Then there is a one-LED break, and the next three LEDs indicate the gery code. Again, we have a one-LED gap, and the following LED represents the binary counter. Furthermore, when direction is 0, the 7-sigment display counts from 7 to 0, and when direction is 1 count from 0 to 7 and cycles back.

Click on the link:https://youtu.be/TfW35ZmhvgY