1. Description

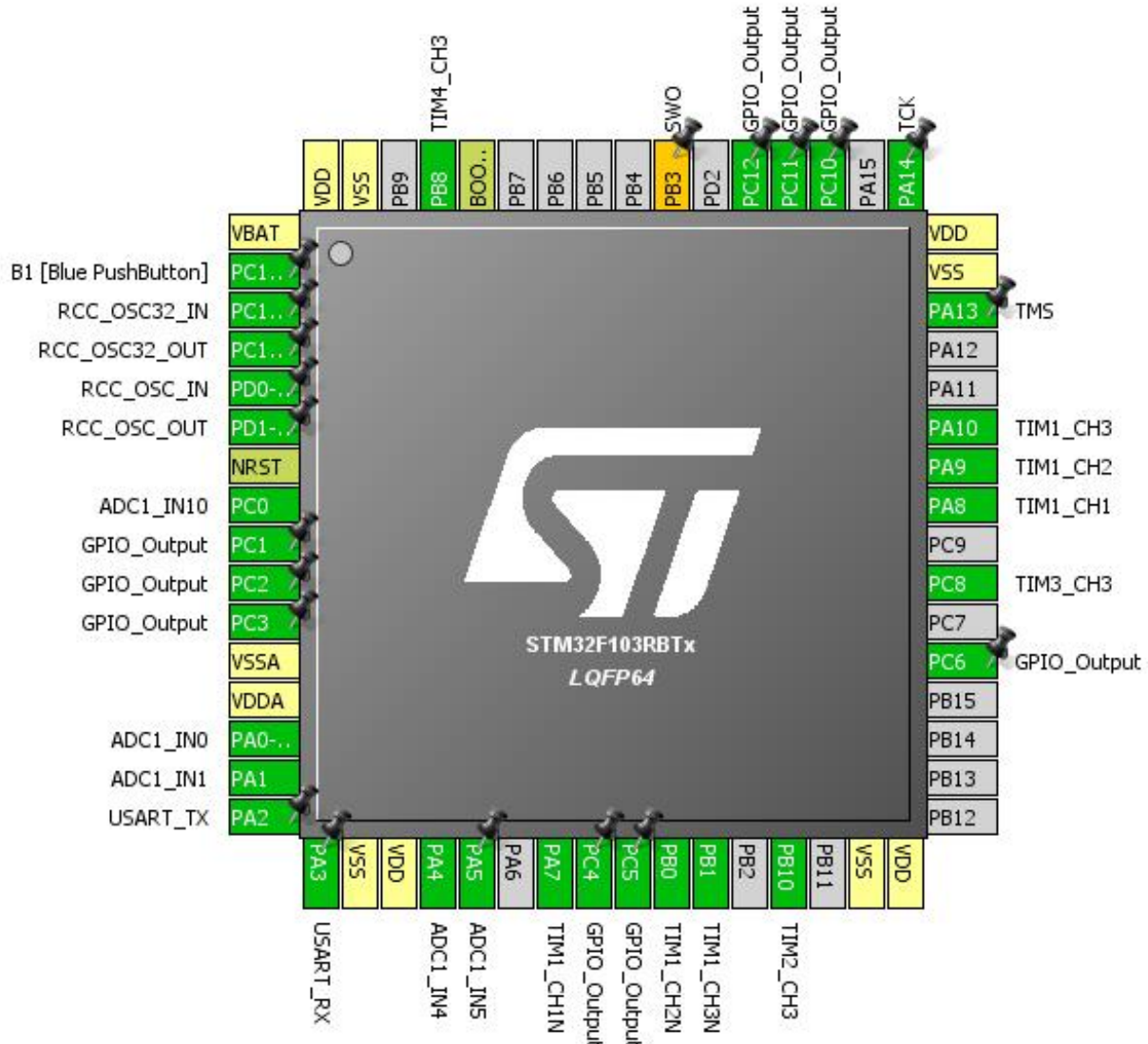
1.1. Project

Project Name	voiture-elec
Board Name	NUCLEO-F103RB
Generated with:	STM32CubeMX 4.21.0
Date	09/19/2017

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103RBTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



3. Pins Configuration

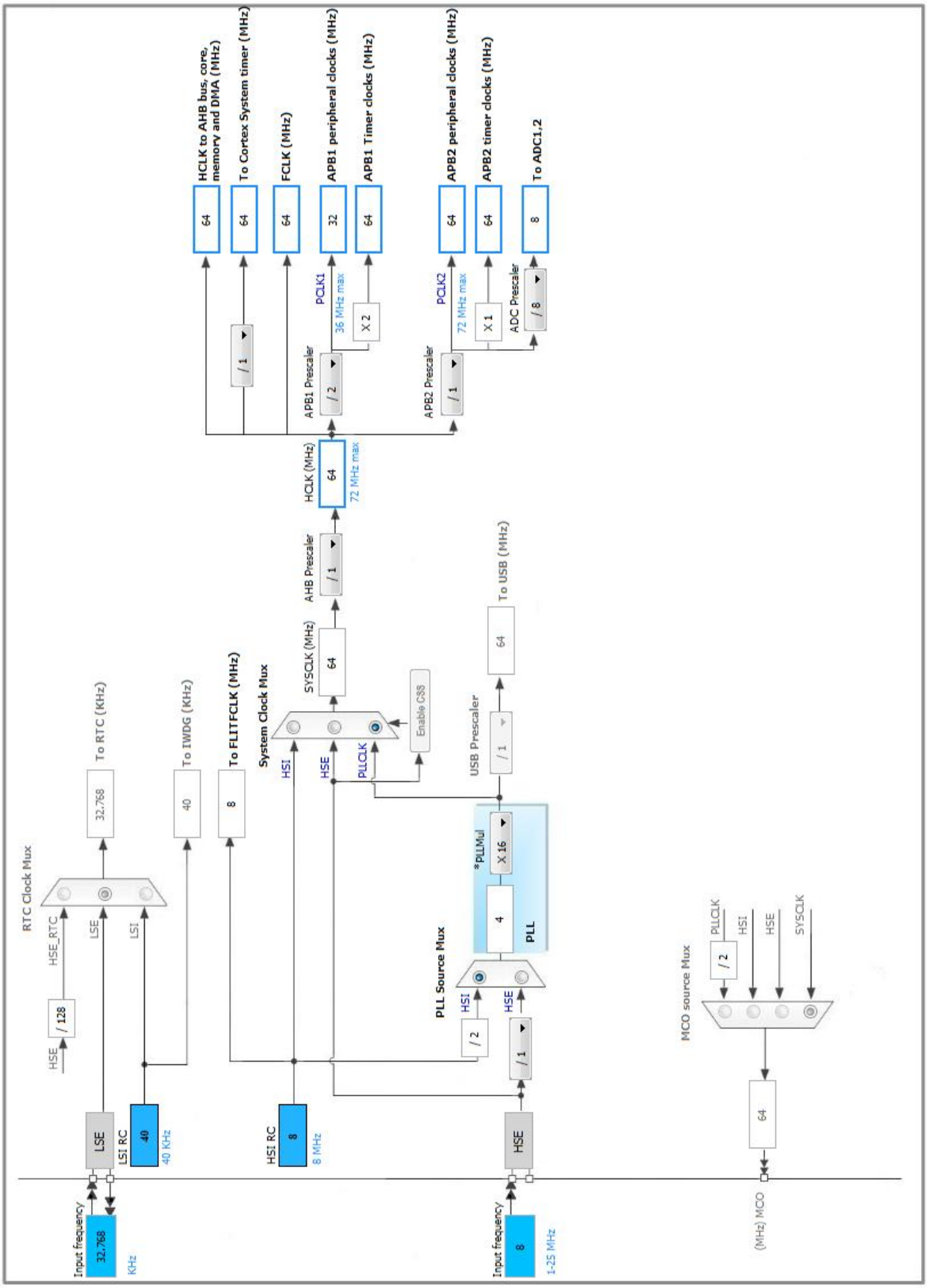
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-TAMPER-RTC	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC1_IN10	
9	PC1 *	I/O	GPIO_Output	
10	PC2 *	I/O	GPIO_Output	
11	PC3 *	I/O	GPIO_Output	
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	ADC1_IN0	
15	PA1	I/O	ADC1_IN1	
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN4	
21	PA5	I/O	ADC1_IN5	
23	PA7	I/O	TIM1_CH1N	
24	PC4 *	I/O	GPIO_Output	
25	PC5 *	I/O	GPIO_Output	
26	PB0	I/O	TIM1_CH2N	
27	PB1	I/O	TIM1_CH3N	
29	PB10	I/O	TIM2_CH3	
31	VSS	Power		
32	VDD	Power		
37	PC6 *	I/O	GPIO_Output	
39	PC8	I/O	TIM3_CH3	
41	PA8	I/O	TIM1_CH1	
42	PA9	I/O	TIM1_CH2	
43	PA10	I/O	TIM1_CH3	
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
51	PC10 *	I/O	GPIO_Output	
52	PC11 *	I/O	GPIO_Output	
53	PC12 *	I/O	GPIO_Output	
55	PB3 **	I/O	SYS_JTDO-TRACESWO	SWO
60	BOOT0	Boot		
61	PB8	I/O	TIM4_CH3	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0

mode: IN1

mode: IN4

mode: IN5

mode: IN10

5.1.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
ADC_Regular_ConversionMode:	
Enable Regular Conversions	Enable
Number Of Conversion	**5 ***
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	1.5 Cycles
Rank	**3 ***
Channel	**Channel 4 ***
Sampling Time	1.5 Cycles
Rank	**4 ***
Channel	**Channel 5 ***
Sampling Time	1.5 Cycles
Rank	**5 ***
Channel	**Channel 10 ***
Sampling Time	1.5 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.4. TIM1

Channel1: PWM Generation CH1 CH1N

Channel2: PWM Generation CH2 CH2N

Channel3: PWM Generation CH3 CH3N

5.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**3200 ***

Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	0

PWM Generation Channel 1 and 1N:

Mode	PWM mode 1
Pulse (16 bits value)	**320 ***
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 2 and 2N:

Mode	PWM mode 1
Pulse (16 bits value)	**1600 ***
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 3 and 3N:

Mode	PWM mode 1
Pulse (16 bits value)	**1600 ***
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

5.5. TIM2

Clock Source : Internal Clock

Channel3: Input Capture direct mode

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**6399 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.6. TIM3

Clock Source : Internal Clock

Channel3: Input Capture direct mode

Channel4: Input Capture indirect mode

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**63 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 3:

Polarity Selection	Rising Edge

IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**15 ***

Input Capture Channel 4:

Polarity Selection	**Falling Edge ***
IC Selection	Indirect
Prescaler Division Ratio	No division

5.7. TIM4

mode: Clock Source
Channel3: Input Capture direct mode

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**6399 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.8. USART2

Mode: Asynchronous

5.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)

Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	n/a	n/a	
	PA0-WKUP	ADC1_IN0	Analog mode	n/a	n/a	
	PA1	ADC1_IN1	Analog mode	n/a	n/a	
	PA4	ADC1_IN4	Analog mode	n/a	n/a	
	PA5	ADC1_IN5	Analog mode	n/a	n/a	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM1	PA7	TIM1_CH1N	Alternate Function Push Pull	n/a	Low	
	PB0	TIM1_CH2N	Alternate Function Push Pull	n/a	Low	
	PB1	TIM1_CH3N	Alternate Function Push Pull	n/a	Low	
	PA8	TIM1_CH1	Alternate Function Push Pull	n/a	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	n/a	Low	
	PA10	TIM1_CH3	Alternate Function Push Pull	n/a	Low	
TIM2	PB10	TIM2_CH3	Input mode	No pull-up and no pull-down	n/a	
TIM3	PC8	TIM3_CH3	Input mode	No pull-up and no pull-down	n/a	
TIM4	PB8	TIM4_CH3	Input mode	No pull-up and no pull-down	n/a	
USART2	PA2	USART2_TX	Alternate Function Push Pull	n/a	Low	USART_TX
	PA3	USART2_RX	*	No pull-up and no pull-down	n/a	USART_RX
Single Mapped Signals	PB3	SYS_JTDO-TRACESWO	n/a	n/a	n/a	SWO
GPIO	PC13-TAMPER-RTC	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PC1	GPIO_Output	Output Push Pull	n/a	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC2	GPIO_Output	Output Push Pull	n/a	Low	
	PC3	GPIO_Output	Output Push Pull	n/a	Low	
	PC4	GPIO_Output	Output Push Pull	n/a	Low	
	PC5	GPIO_Output	Output Push Pull	n/a	Low	
	PC6	GPIO_Output	Output Push Pull	n/a	Low	
	PC10	GPIO_Output	Output Push Pull	n/a	Low	
	PC11	GPIO_Output	Output Push Pull	n/a	Low	
	PC12	GPIO_Output	Output Push Pull	n/a	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
TIM2 global interrupt	true	0	0
TIM3 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
USART2 global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103RBTx
Datasheet	13587_Rev17

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	voiture-elec
Project Folder	U:\Projets Cube\voiture-elec
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F1 V1.4.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No