

STM32MPU embedded software architecture

Content

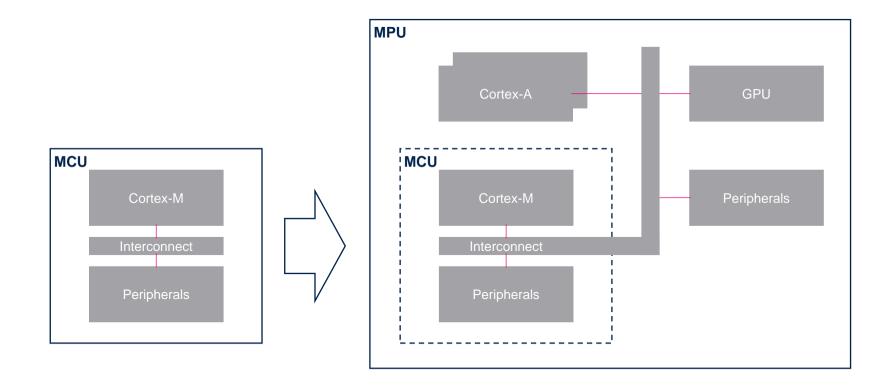
- Peripherals overview and sharing
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Peripherals overview and sharing



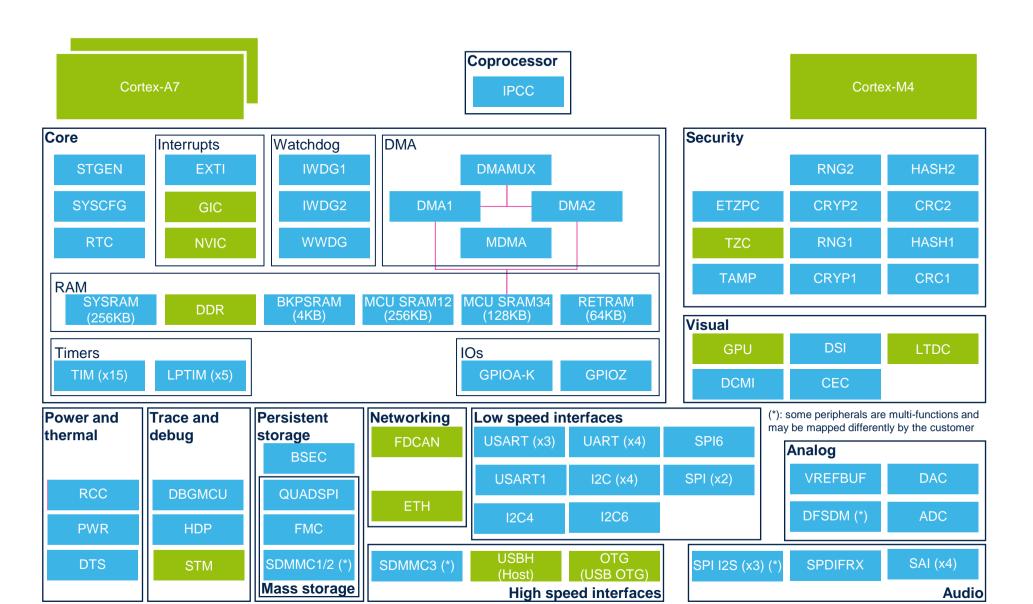
From MCU to MPU







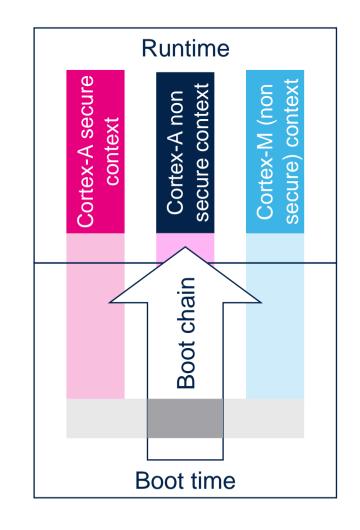
Hardware blocks sourcing





Multiple-core architecture concepts

- Hardware execution context
 - « a core and a security mode »
- Firmwares executed runtime contexts
 - Arm Cortex-A secure (Trustzone) executes OP-TEE
 - Arm Cortex-A non secure executes Linux
 - Arm Cortex-M (non secure) executes STM32Cube
- Peripheral assignment to the runtime contexts
 - Assigned or shared

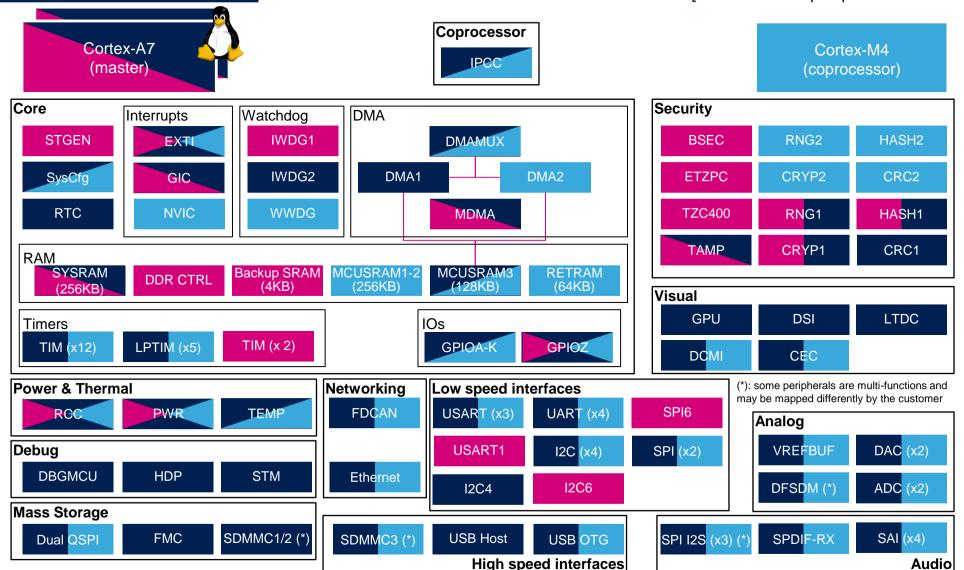




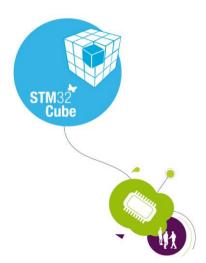
Assigned to Assigned A7S or A7NS to A7NS or M4 Assigned to A7 Assigned to A7 Assigned to Legend Assigned IP Secure (TZ) Non Secure М4 Shared IP Shared by Shared by A7S & A7NS A7NS & M4 Shared by A7S & A7NS & M4

Peripherals sharing

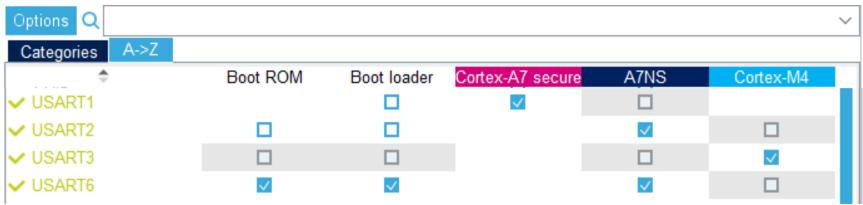
Source: ST Wiki article [STM32MP15 peripherals overview]







Peripherals assignment via stm32cubemx

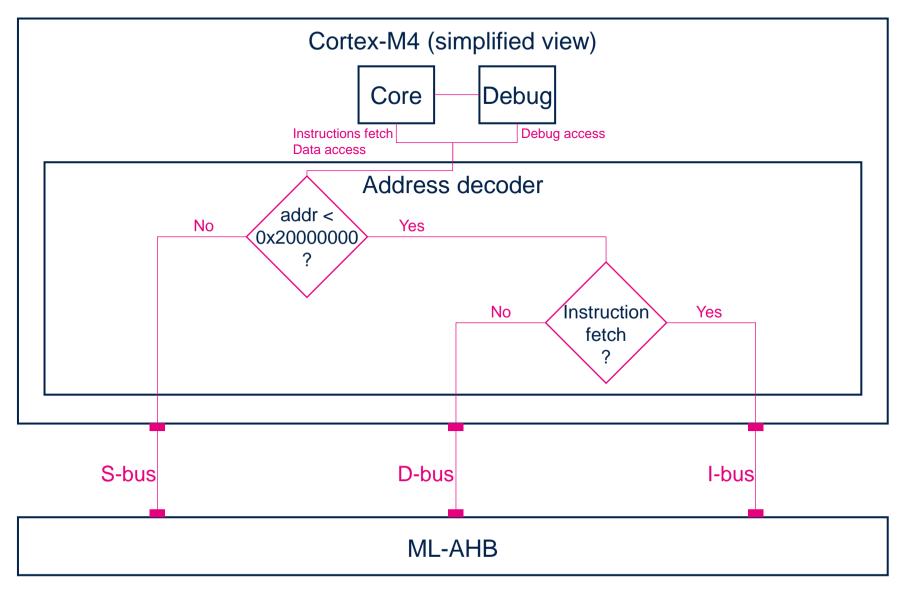




Software memory mapping



Cortex-m4 ports





Software memory mapping

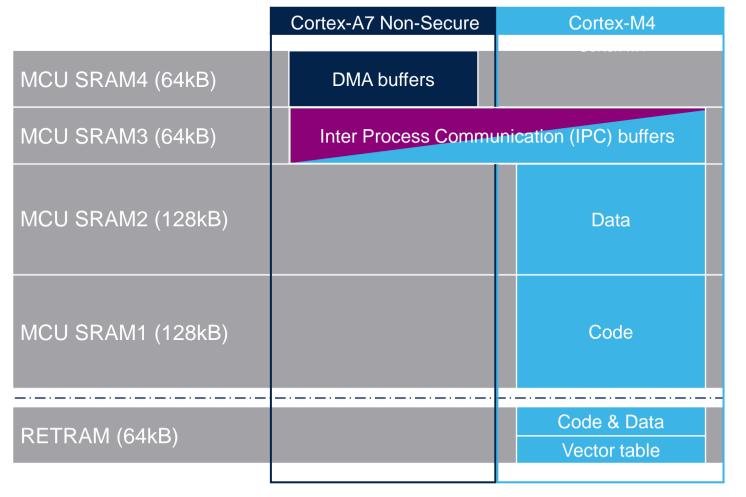
The memory mapping below is a subset of all regions that are really exposed at hardware level.





Shared RAM memory mapping

Notice that each core may not see the same regions at the same address, as already explained on previous slide



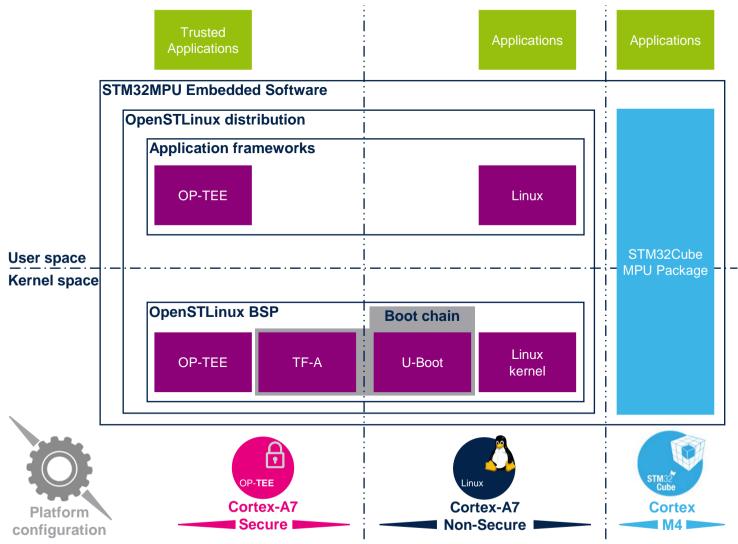


STM32MPU embedded software



STM32MPU embedded software

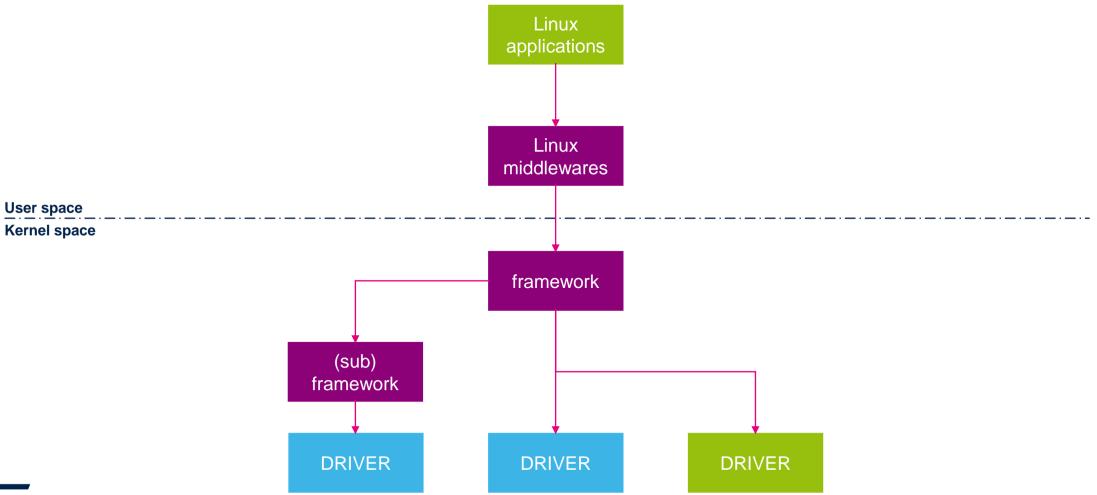






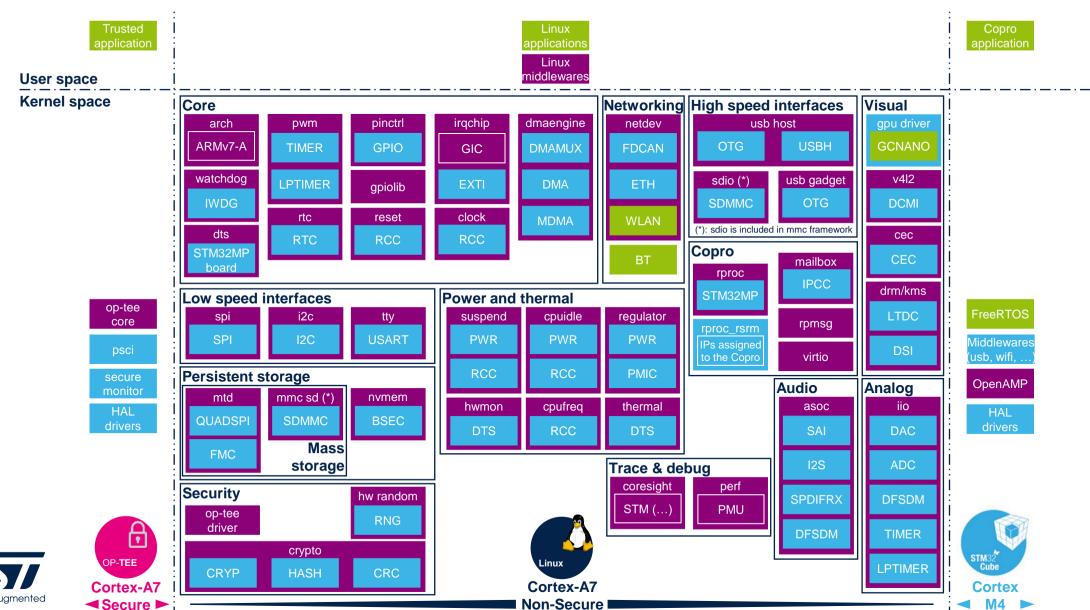
ST Community • lowercase = community framework • UPPERCASE = peripheral driver

Linux framework & driver



3rd Party ST Community • lowercase = community framework • UPPERCASE = peripheral driver

Openstlinux + stm32cube





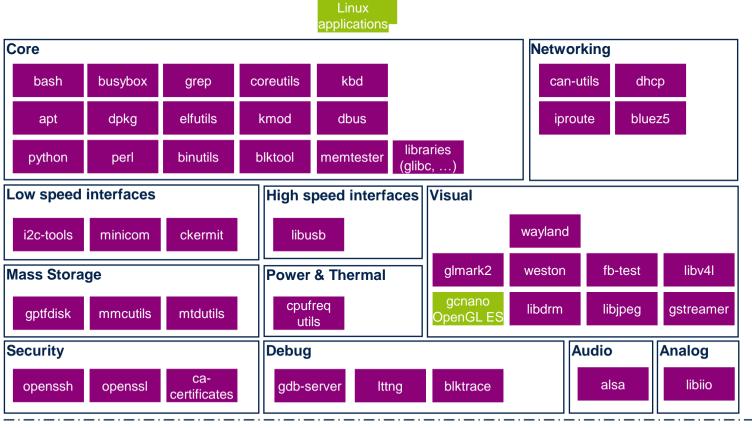


COMPATIBLE

User space

Open-embedded user space

• The components list shown here is not exhaustive and can be tuned by the customer to fit with applications needs.







openembedded