



STM32MP1 training

Overall view





Planning





Training planning

- Day 1 : (9:00am to 5:00pm):
 - STM32MP1 overall presentation
 - MP1 HW presentation (architecture, external memories Flash & DDR)
 - SW architecture
 - Boot mechanism
 - Lunch break
 - Starter package: presentation and hands on with usage of STM32CubeProgrammer
 - Developer package : presentation and demo





Training planning

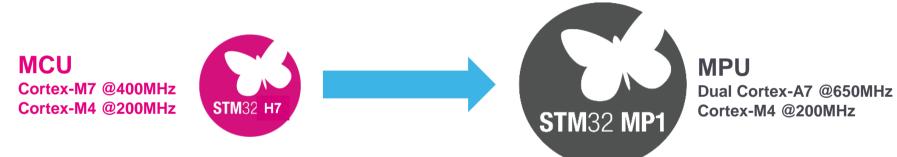
- Day 2 (9:00am to 3:30pm)
 - Distribution package: introduction and demo
 - CubeMx: device tree generation and integration
 - DDR tools : presentation and hand on
 - Lunch break
 - M4 firmware generation and debug





STM32MP1 introduction

- First General Purpose STM32 MPU
 - Roadmap extension of STM32H7, new microprocessor based on Cortex-A7
 - Sub-gigahertz product, targeting low to mid end MPU applications
 - Add to STM32 ecosystem the support for Linux & Android
 - Embed an additional Cortex-M4 core and common STM32 MCU IP / peripherals to address real time constraints and low power processing
 - Keeps fully compatible with existing STM32 MCU software ecosystem & tools
 - Industrial qualification -40°C/125°C Tj on all packages
 - 40nm product with 10year lifetime guarantee









First STM32 performance line MPU

Microprocessors



Microcontrollers





Cortex-M4 @180MHz (225DMIPS)



Cortex-M3 @120MHz (150DMIPS)

STM32 Performance Line



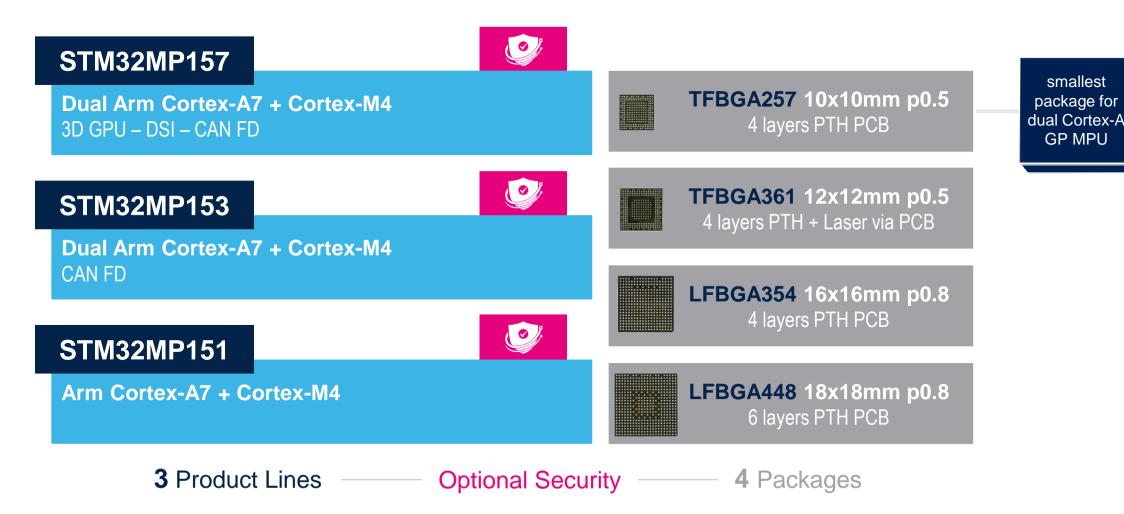


STM32MP1 product lines 24 sales type in production now

smallest

package for

GP MPU





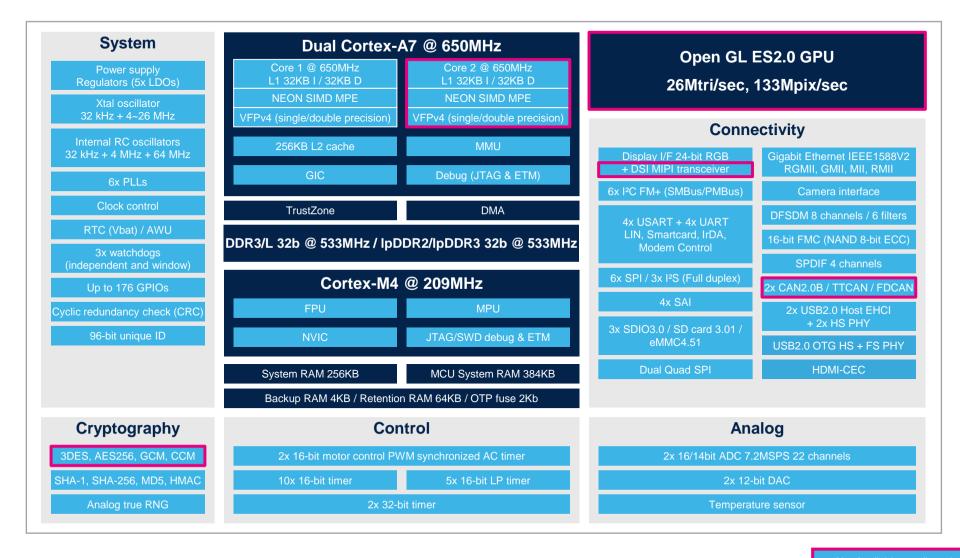


STM32MP157





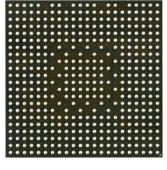
STM32MP157 block diagram





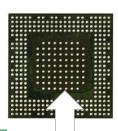


Packages



0.8mm - DDR3

0.5mm - LPDDR2/3 & DDR3



Full features

LFBGA448 18x18mm pitch 0.8
32-bit DDR3I/F
176 GPIOs
6 layers PTH PCB

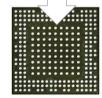
TFBGA361 12x12mm pitch 0.5 32-bit LPDDR2/LPDDR3/DDR3I/F 148 GPIOs 4 layers PCB

> Pitch 0.65 on inner ball matrix to ease PCB supply routing

Low cost



LFBGA354 16x16mm pitch 0.8 16-bit DDR3I/F 98 GPIOs 4 layers PTH PCB TFBGA257 10x10mm pitch 0.5 16-bit LPDDR2/LPDDR3/DDR3I/F 98 GPIOs 4 layers PCB



Industrial qualification: -40°C / 125°C Tj



STM32MP1 product lines

	• MDMA + DMA • LPDDR2/LPDDR3 16/32**-bits 533MHz • DDR3/DDR3L 16/32**-bits 533MHz CONNECTIVITY • 2 x USB2.0 HS Host • USB2.0 OTG FS/HS • 3 x SDMMC/SDIO	Product RPN	f _{CPU} (MHz)	Cortex®-A7 cores	f _{MCU} (MHz)	Cortex®-M4 cores	f _{GPU} (MHz)	Cortex [®] -A7 L1 cache (I/D) L2 cache	RAM (Kbytes)	HW Crypto	3D GPU	FDCAN	MIPI®-DSI
		STM32MP151A	- 650	1	209	1	-	32K+32K + 256K	640K + 64K retention + 4K backup	·		_	_
Arm [®] Cortex [®] -A7 – 650 MHz		STM32MP151C								•			
		STM32MP153A	650	2	209	1	-	2x (32K+32K) + 256K	640K + 64K retention + 4K backup	i	_	2	_
		STM32MP153C		_						•		_	
	AUDIO • I ² S + audio PLL • 4 x SAI + 8 x DFSDM + SPDIF-RX • 2 x 12-bit DAC	STM32MP157A	650	2	209	1	533	2x (32K+32K)	640K + 64K retention	i		2	
	OTHER 16- and 32-bit timers 2 x 16-bit ADC (7.2 MSPS)	STM32MP157C			200	·		+ 256K	+ 4K backup	•		_	-



Notes:

* not available in all product lines

^{** 16/32-}bits for LFBGA448 and TFBGA361 packages, 16-bits only for LFBGA354 and TFBGA257 packages

^{*** 10/100}M Ethernet only for LFBGA354 and TFBGA257 packages



Power management IC





STPMIC1

- Power management companion IC for STM32MP1
 - Large input range (2.8~5.5V) compatible with 3.7V battery
 - No Battery charger integrated, external battery charging device to be added if needed
 - Provides all the supply for STM32MP1, DRAM and few external components
 - Combination of 4 switching regulators + 6 linear regulators
 - Integrated 5V boost regulator for USB Vbus with 2 ports power switching capability
 - Control via through I2C interface and digital I/O
 - Power control, reset, interrupt, wake up, ...
 - Programmable configuration with NVM
 - Straighforward NVM (re)programming via I2C
 - Default output voltage, soft start
 - Start sequence
 - Protections, ...





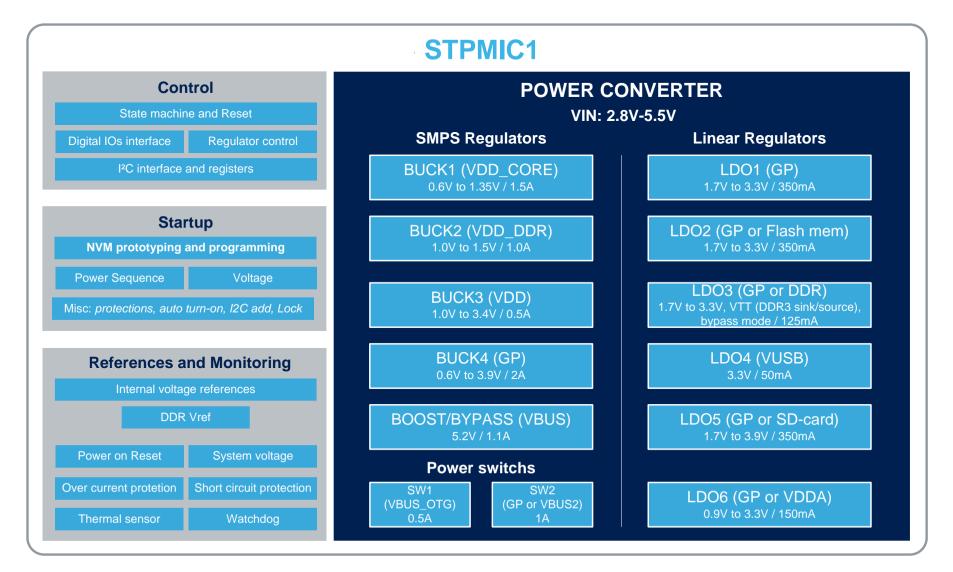
STPMIC1

- Power management companion IC for STM32MP1
 - Packaging
 - QFN44 5x6x0.4mm
 - Industrial and consumer temperature range





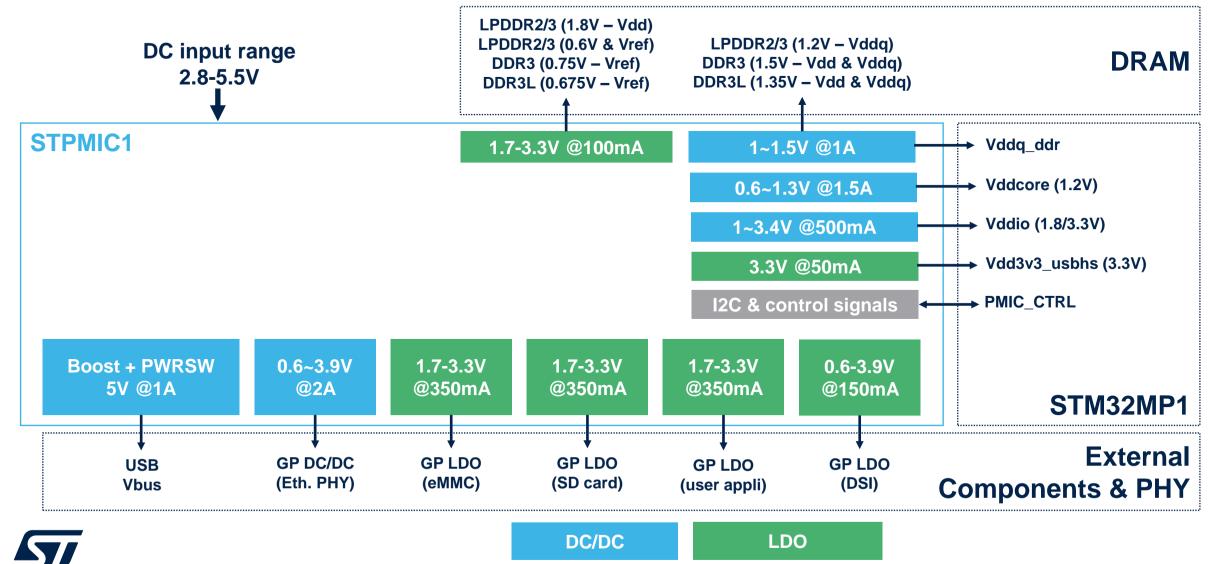
STPMIC1 functional block diagram







PMIC





Hardware ecosystem



STM32MP1 hardware solutions

Speed-up evaluation, prototyping and design

Available at \$399









Evaluation Board

Full feature STM32MP1 evaluation

- STM32MP157A-EV1
- STM32MP157C-EV1



Discovery Board

Flexible prototyping & demo

2 Versions

- STM32MP157A-DK1
- STM32MP157C-DK2
 - + MIPI DSI WVGA display
 - + Wi-Fi/BT combo module

Boards & SoM*s

3rd Parties Boards for prototyping and production

- Board Specification from Linaro (96boards.org)
- Commercial SoM w/ different forms



EV1



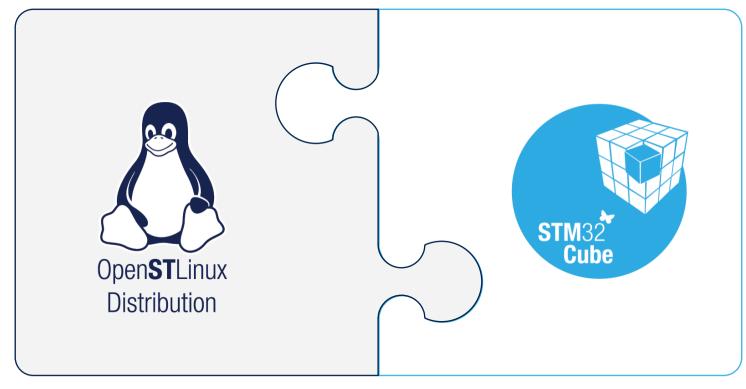
Software ecosystem





A fully integrated design suite leveraging the stm32cube environment







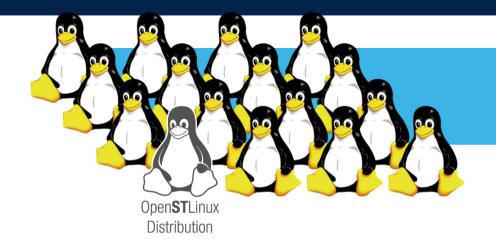
STM32MPU Embedded Software Distribution





Simplify your linux development

Fully mainlined open source Linux distribution for Arm Cortex-A7



STM32MP1 SoC drivers already adopted by the Linux community

STM32MP1 supported in Linux 4.19 LTS

Fully compliant with open-source standards





Pre-integrated Secure OS







STM32CUBEMP1 package

Full re-use of STM32 MCU Cube firmware on Arm Cortex-M





Several APIs to access peripherals



Collection of Middleware components for Cortex-M



Hundreds of Examples



Production-ready Quality



Business-friendly license terms

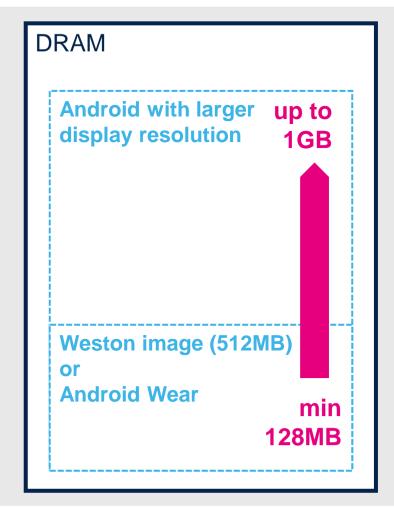


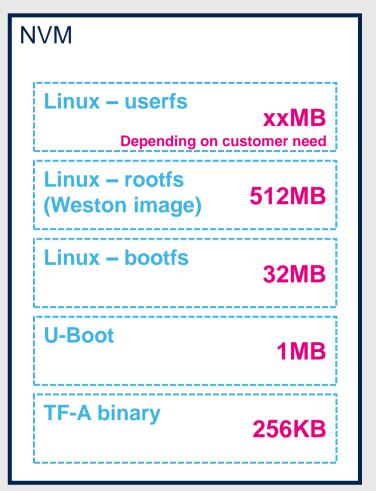


Memory footprints

ST software footprints (footprints can be reduced depending)

(footprints can be reduced depending on the implemented application)









Power modes





Power modes

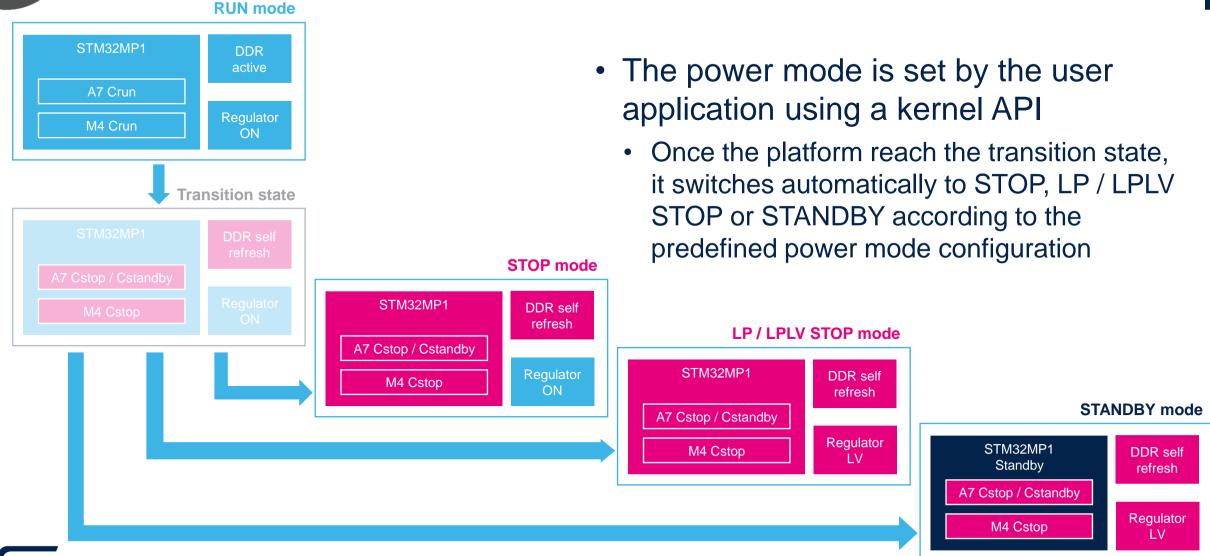
- Power management at platform and cluster level
 - STM32MP1 has 4 power states
 - Run
 - Stop
 - LP / LPLV-Stop => Same as Stop with low voltage supply (Vcore = 0.9V)
 - Standby => Only Vdd remains (Vcore = OFF) and wakeup only with a reset
 - Each cluster has its own power management
 - A7 cluster has 4 power modes
 - Crun
 - Csleep (core clock stopped)
 - Cstop (core + IP clock stopped)
 - Cstandby (core + IP clock stopped and wakeup only with a reset)
 - M4 cluster has 3 power modes
 - Crun
 - Csleep (core clock stopped)
 - Cstop (core + IP clock stopped)





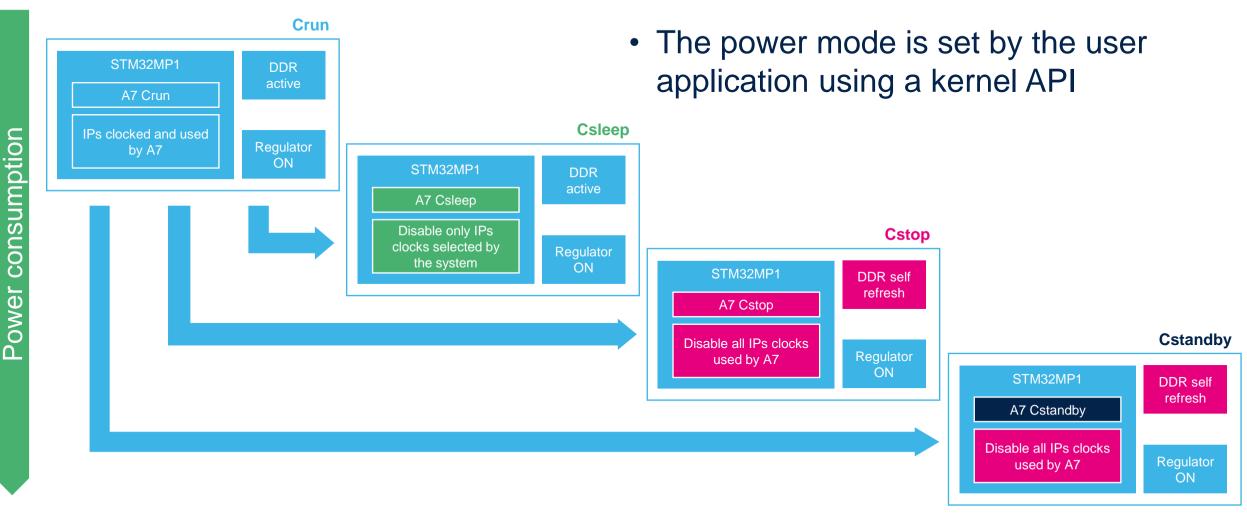
Power consumption

Platform power mode





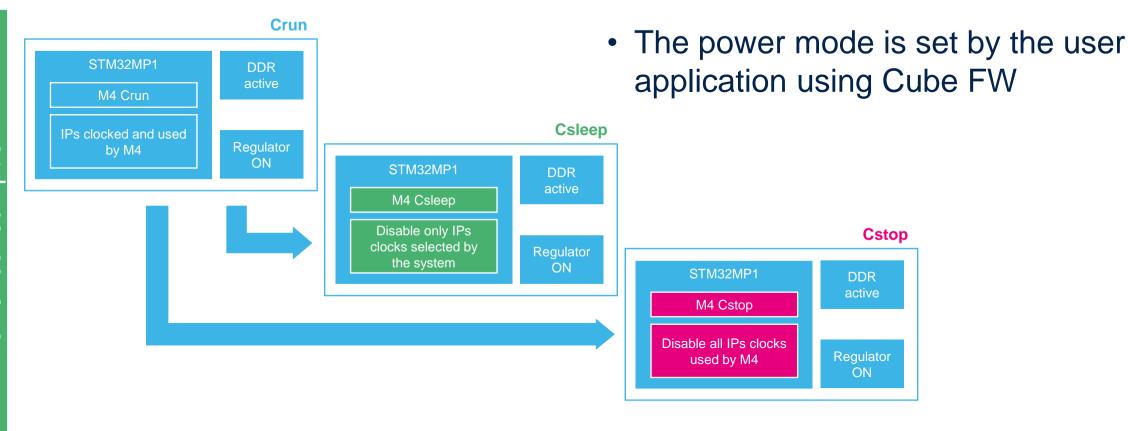
A7 cluster power mode







M4 cluster power mode

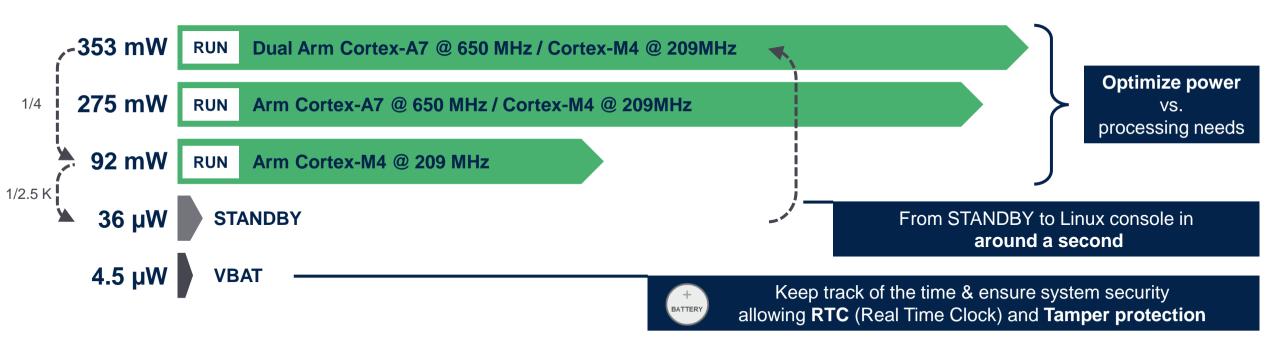






Flexible architecture for power efficiency

Power figures



Typ @ VDDCORE = 1.2V, VDD = 3.3V @ 25 °C, Peripherals OFF





Software distribution

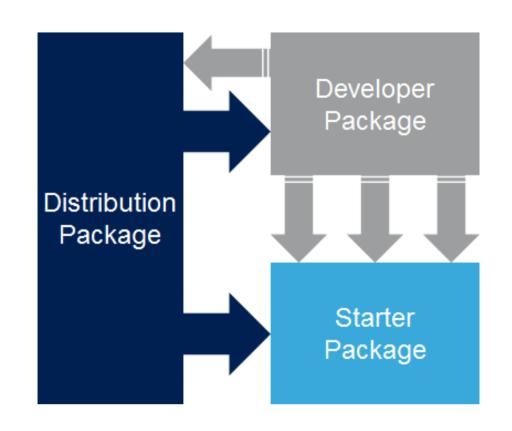






One distribution, three packages

- Open STLinux
- Starter Package
 - To quickly and easily start with any STM32MP1
- Developer Package
 - To add your own developments on top of the STM32MP1 Embedded Software distribution
- Distribution Package
 - To create your own Linux® distribution, your own Starter Package and your own Developer Package







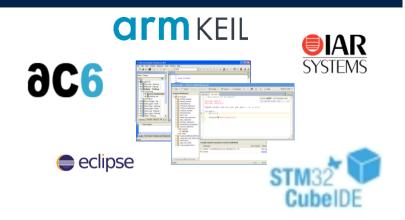
STM32MP1 tools



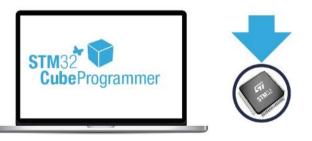
STM32MP1 software tools

Complete support of Arm Cortex-A + Cortex-M architecture





All-in-one STM32 programming tool Multi-mode, user-friendly



STM32CubeMX

STM32CubeMX enhanced for MPU

- Configure and generate Code
- · DRAM interface tuning tool
- Device Tree generation

IDEsCompile and Debug

Multi-Core Solutions

- Partners IDE
- Free IDE based on Eclipse
- Multi-core debugging

STM32 Programming Tool

STM32CubeProgrammer

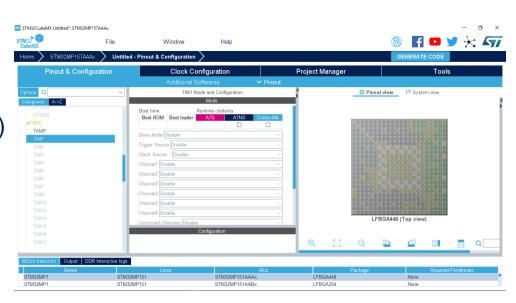
- Flash, DRAM and/or system memory
- OTP programming
- Signing tool & Keys generation





STM32CubeMX

- For STM32MP1
 - Manages the GPIOs multiplexing & the clock setup (like for STM32 MCU)
 - Manages the interactive peripherals assignment to Cortex-A & Cortex-M cores
- For the Cortex-A side
 - Handles the DRAM configuration & tuning
 - Generates the configuration => device tree (for TF-A, U-Boot & Linux)
 - GPIOs multiplexing, clock setup, peripherals assignment
- For the Cortex-M side
 - Generates the code & configuration (like for STM32 MCU)
 - GPIOs multiplexing, clock setup, peripherals assignment

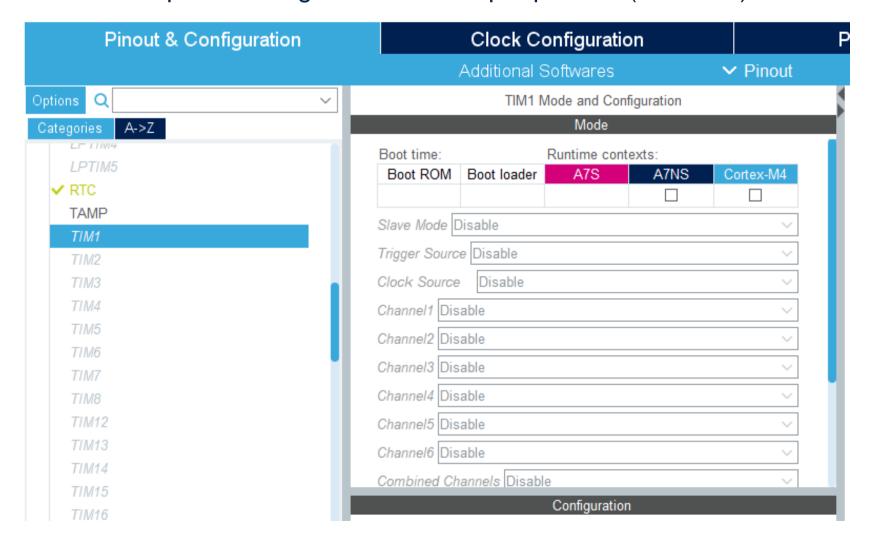






STM32CubeMX – peripheral assignment

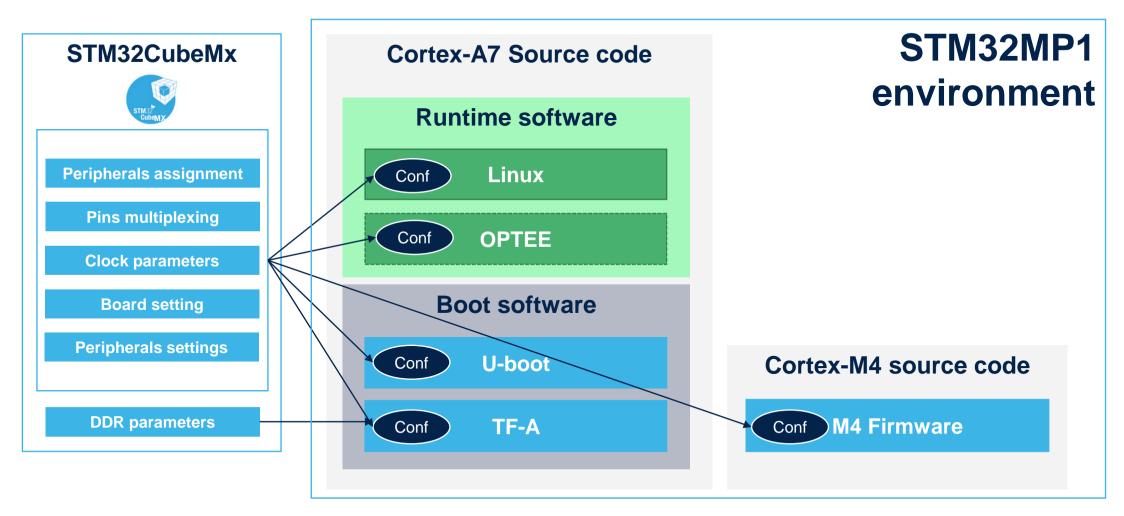
Allows user to make specific assignment core peripherals (ex. TIM1)







STM32CubeMX – device tree

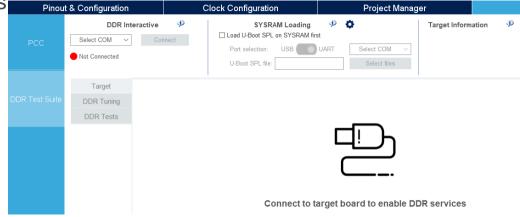






STM32CubeMX – DDR plugin

- The DDR plugin handles the configuration, test and tuning of the DRAM controller
 - Configuration
 - Basic / advanced wizard to generate the memory controller configuration based on the DRAM datasheet
 - Test the DRAM configuration on board
 - Generates a configuration report
 - Test
 - Set of default tests provided to check hardware reliability
 - Generates a test report
 - Tuning
 - Run tuning, collect back the results and adjust parameters
 - Adjust the default configuration with tuned parameters







IDE - STM32CubeIDE

STM32CubeIDE

Latest version 1.4.2

- Description
 - Support STM32MP1 now.
 - Does everything same as system workbench.
- IDE
 - Eclipse
- Compiler

Available via command line

- GCC C/C++
- Debugger
 - OpenOCD/GDB-based
- Debug probe
 - ST-Link





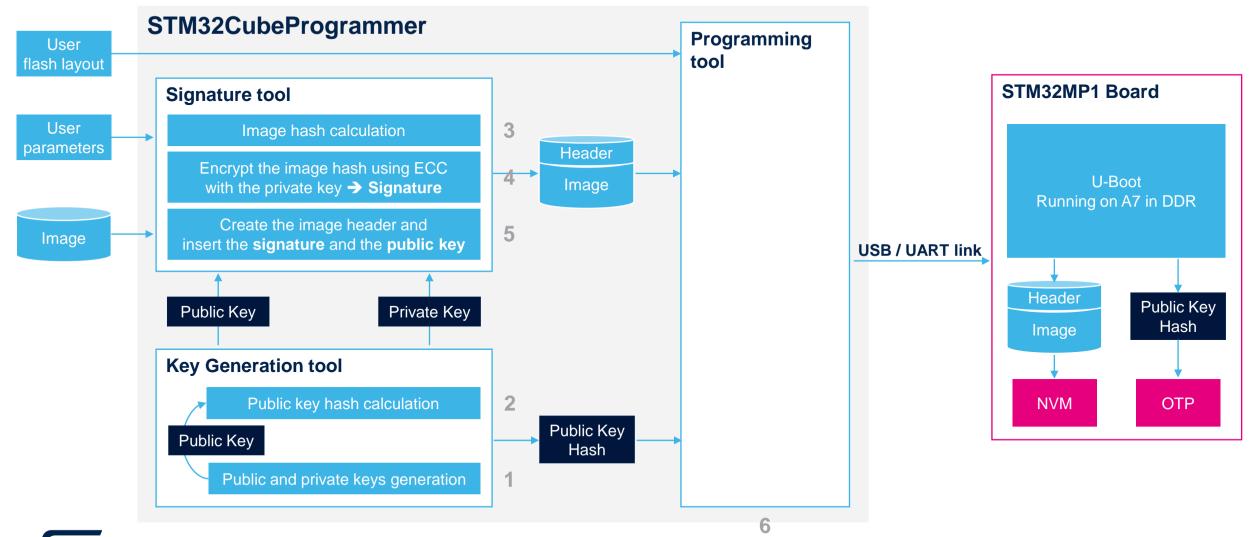
Stm32cubeprogrammer

- The STM32CubeProgammer tool set is made of three software
 - Key generation tool
 - ECC key generation (private & public keys)
 - Public hash key generation
 - Signature tool
 - Create binary header with
 - User information (image entry point, load address, image version, ECC algorithm and option parameter)
 - ECC signature
 - ECC public key
 - Concatenate the header with the image
 - Programming tool
 - Utility to program STM32MPU1 NVMs/OTP through UART and USB
 - Flashing services & OTP programming via U-Boot
 - Support NOR, NAND, SDCARD, eMMC
 - PMIC NVM programming via U-Boot (I2C)
 - Secure secret programming





Stm32cubeprogrammer





Releasing your creativity with the STM32



Famous video here

www.st.com/stm32

