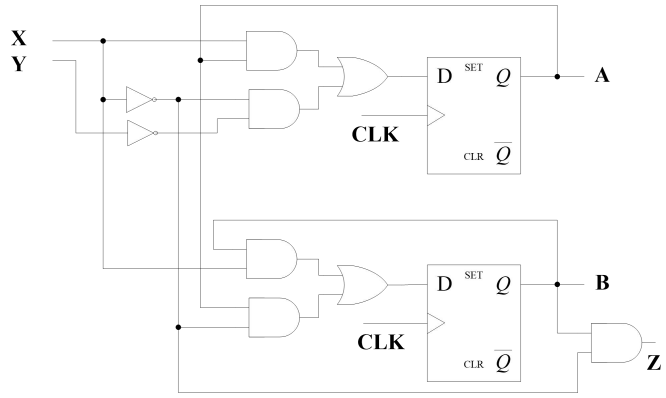
第四章布置习题参考解

4-6

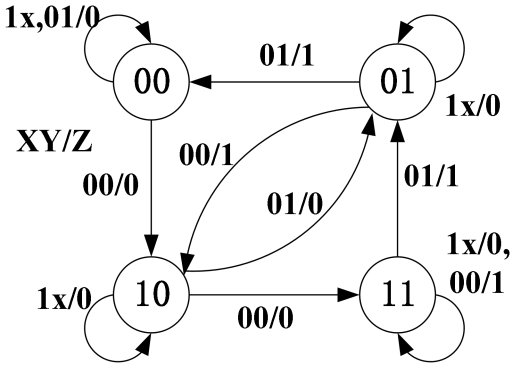
Solution:

a）According to the input equations and output equation, the logic diagram is:



b) According to the input equations and output equation, the state table is:

Present state		Inputs		Next state		Output
A	B	X	Y	A	B	Z
0	0	0	0	1	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	1	0	1
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	1	1	0
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	1	1	1
1	1	0	1	0	1	1
1	1	1	0	1	1	0
1	1	1	1	1	1	0

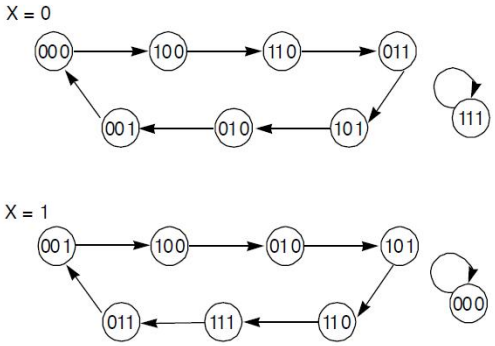


c) According to the state table, the state diagram is:

4-7

Solution：

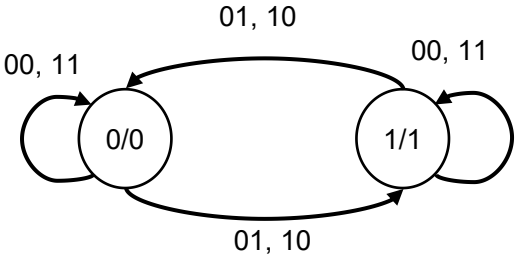
Present state			Input	Next state		
A	B	C	X	A	B	C
0	0	0	0	1	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	0	0	1
1	0	0	0	1	1	0
1	0	0	1	0	1	0
1	0	1	0	0	1	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	0	1	1



State diagram is the combination of the above two diagrams.

4-8

Present state	Inputs		Next state	Output
Q	X	Y	Q	S
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



4-9

Present State	**00**	**01**	**00**	**00**	**01**	**11**	**00**	**01**	**11**	**10**	**10**
Input	**1**	**0**	**0**	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**0**
Output	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**
Next State	**01**	**00**	**00**	**01**	**11**	**00**	**01**	**11**	**10**	**10**	**00**

4-11

① **State equations：**

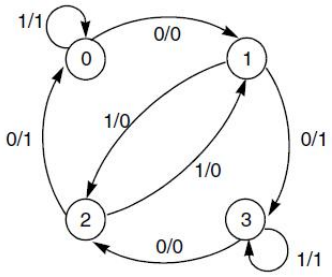
$S_A = B$，$S_B = \overline{X \oplus A}$

$Y = X \oplus A \oplus B$

② **State table：**

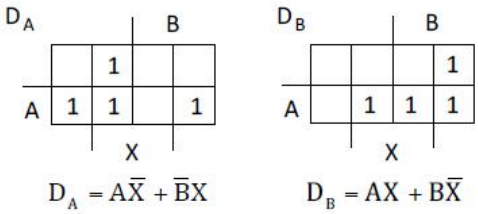
Present state		Input	Next state		Output
A	*B*	*X*	*A*	*B*	*Y*
0	0	0	0	1	0
0	0	1	0	0	1
0	1	0	1	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	0	1	0
1	1	0	1	0	0
1	1	1	1	1	1

③ **State diagram：**



4-13

Present state		Input	Next state	
A	*B*	*X*	*A*	*B*
0	0	0	0	0
0	0	1	1	0
0	1	0	0	1
0	1	1	0	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	1

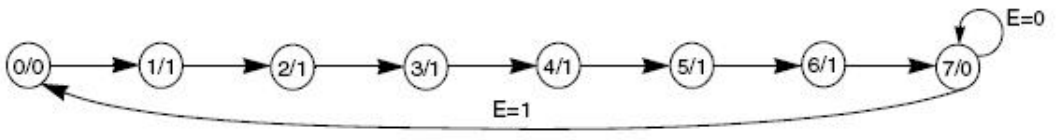


$D_A = A\overline{X} + \overline{B}X$ $D_B = AX + B\overline{X}$

Logic diagram not given.

4-21

Moore state diagram is:



Assumes for E = 0, the output remains

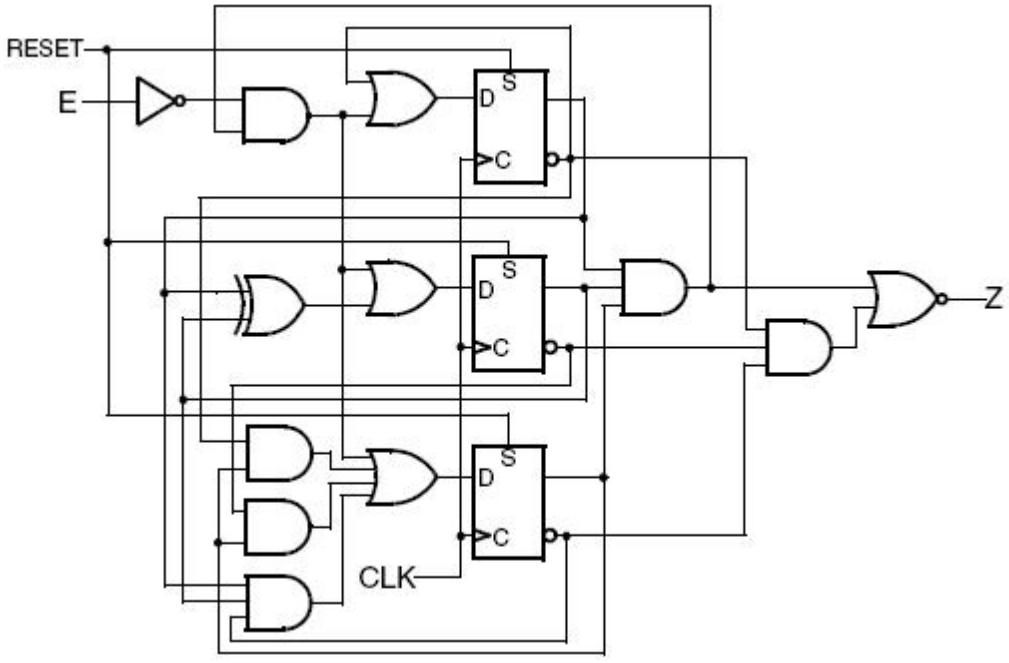
state table:

Present state	Next State For Input		Output
$D_2D_1D_0$	E=0	E=1	Z
000	001	001	0
001	010	010	1
010	011	011	1
011	100	100	1
100	101	101	1
101	110	110	1
110	111	111	1
111	111	000	0

next state functions and output function:

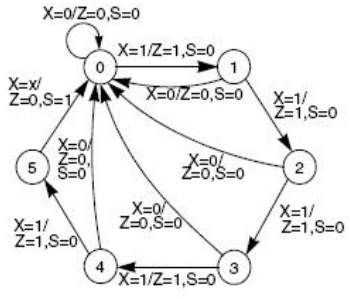
$$D_2(t+1) = D_2\overline{D_1} + D_2\overline{D_0} + \overline{D_2}D_1D_0 + D_2\overline{E} \quad (D_2D_1D_0\overline{E})$$
$$D_1(t+1) = D_1\overline{D_0} + \overline{D_1}D_0 + D_2D_0\overline{E} \quad (D_2D_1\overline{E},\quad D_2D_1D_0\overline{E})$$
$$D_0(t+1) = \overline{D_0} + D_2D_1\overline{E} \quad (D_2D_1D_0\overline{E})$$
$$Z = \overline{D_2D_1D_0 + \overline{D_2}\,\overline{D_1}\,\overline{D_0}} = D_1\overline{D_0} + D_2\overline{D_1} + \overline{D_2}D_0 = \overline{D_1}D_0 + \overline{D_2}D_1 + D_2\overline{D_0}$$

When reset, the initial state should be '111', so the signal RESET is connected to the direct Set input of all flip-flops.
Circuit diagram:



4-22

The input of the circuit is the Sequence on X with stalls. After a fifth 1 in sequence appears on X, next input should be skipped, and Z = 0, S = 1. So the state diagram is:



Present state			Input	Next state			Output	
A	*B*	*C*	*X*	*A*	*B*	*C*	*Z*	*S*
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1	0
0	0	1	0	0	0	0	0	0
0	0	1	1	0	1	0	1	0
0	1	0	0	0	0	0	0	0
0	1	0	1	0	1	1	1	0
0	1	1	0	0	0	0	0	0
0	1	1	1	1	0	0	1	0
1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	1	0
1	0	1	0	0	0	0	0	1
1	0	1	1	0	0	0	0	1

$$D_A = A\overline{C}X + BCX$$

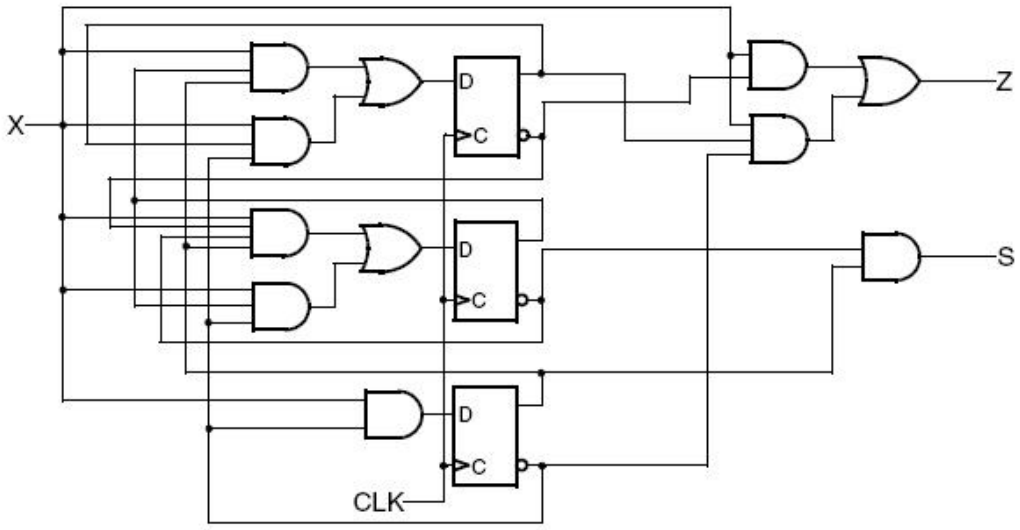
$$D_B = B\overline{C}X + \overline{A}\overline{B}CX$$

$$D_C = \overline{C}X$$

$$Z = \overline{A}X + \overline{C}X = (\overline{A} + \overline{C})X$$

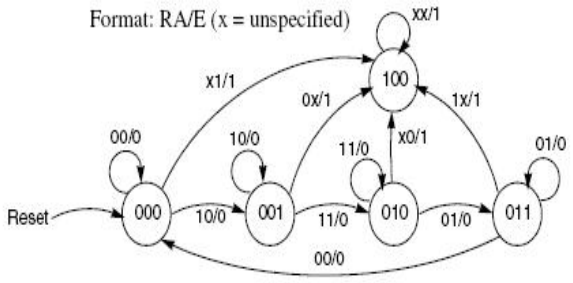
$$S = AC$$

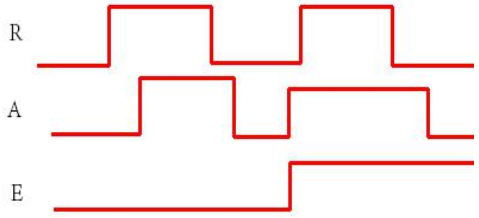
电路图为：



4-25

4 working cycle states are setup when input RA = 00, 10, 11, 01. An error state is setup when an error input occurred. So the state diagram is:





State diagram:

Present state			Inputs		Next state			Output
B	*C*	*D*	*R*	*A*	*B*	*C*	*D*	*E*
0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0	1
0	0	0	1	0	0	0	1	0
0	0	0	1	1	1	0	0	1
0	0	1	0	0	1	0	0	1
0	0	1	0	1	1	0	0	1
0	0	1	1	0	0	0	1	0
0	0	1	1	1	0	1	0	0
0	1	0	0	0	1	0	0	1
0	1	0	0	1	0	1	1	0
0	1	0	1	0	1	0	0	1
0	1	0	1	1	0	1	0	0

Present state			Inputs		Next state			Output
B	*C*	*D*	*R*	*A*	*B*	*C*	*D*	*E*
0	1	1	0	0	0	0	0	0
0	1	1	0	1	0	1	1	0
0	1	1	1	0	1	0	0	1
0	1	1	1	1	1	0	0	1
1	0	0	0	0	1	0	0	1
1	0	0	0	1	1	0	0	1
1	0	0	1	0	1	0	0	1
1	0	0	1	1	1	0	0	1

4-29

If the invalid next states are don't care, the state diagram is:

Current State			Next State			Output		
A	B	C	A	B	C	X	Y	Z
0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	x	x	x	0	1	0
0	1	1	0	0	1	0	1	1
1	0	0	1	1	0	1	0	0
1	0	1	x	x	x	1	0	1
1	1	0	1	1	1	1	1	0
1	1	1	0	1	1	1	1	1

a) Next state functions and output functions:

$D_A = \overline{C}$

$D_B = A$

$D_C = B$

$X = A$

$Y = B$

$Z = C$

Circuit diagram (omitted)

b) Connect $\overline{\text{Reset}}$ to the direct Reset of all flip-flops.

c)~f) The circuit is suitable for child's toy, but not for life critical applications. In the case of the child's toy, it is the cheapest implementation. If an error occurs the child just needs to reset it. In life critical applications, the immediate detection of errors is critical. The circuit above enters invalid states for some errors. For a life critical application, additional circuitry is needed for immediate detection of the error ($E = A\overline{B}C + \overline{A}B\overline{C}$). This circuit using the design in a), does return from the invalid states to a valid state automatically after one or two clock periods.

4-58

a) nearby 28ns, signal D1 violate setup time restriction.

b) nearby 16ns, signal D2 violate hold time restriction. Nearby 24ns, signal D2 violate setup time restriction.

4-59

a) The longest direct path delay is from input X through the two XOR gates to the output Y.

$t_{delay} = t_{pdXOR} + t_{pdXOR} = 0.04 + 0.04 = 0.08$ ns

b) The longest path from an external input to a positive clock edge is from input X through the XOR gate and the inverter to the B Flip-flop.

$t_{delay} = t_{pdXOR} + t_{pdINV} + t_{sFF} = 0.04 + 0.01 + 0.02 = 0.07$ ns

c) The longest path delay from the positive clock edge is from Flip-flop A through the two XOR gates to the output Y.

$t_{delay} = t_{pdFF} + 2\ t_{pdXOR} = 0.08 + 2(0.04) = 0.16$ ns

d) The longest path delay from positive clock edge to positive clock edge is from clock on Flip-flop A through the XOR gate and inverter to clock on Flip-flop B.

$t_{delay\text{-}clock\ edge\ to\ clock\ edge} = t_{pdFF} + t_{pdXOR} + t_{pdINV} + t_{sFF} = 0.08 + 0.04 + 0.01 + 0.02 = 0.15$ ns

e) The maximum frequency is $1/t_{delay\text{-}\ clock\ edge\ to\ clock\ edge}$. For this circuit, $t_{delay\text{-}clock\ edge\ to\ clock\ edge}$ is 0.15 ns, so the maximum frequency is 1/0.15 ns = 6.67 GHz.

Comment: The clock frequency may need to be lower due to other delay paths that pass outside of the circuit into its environment. Calculation of this frequency cannot be performed in this case since data for paths through the environment is not provided.