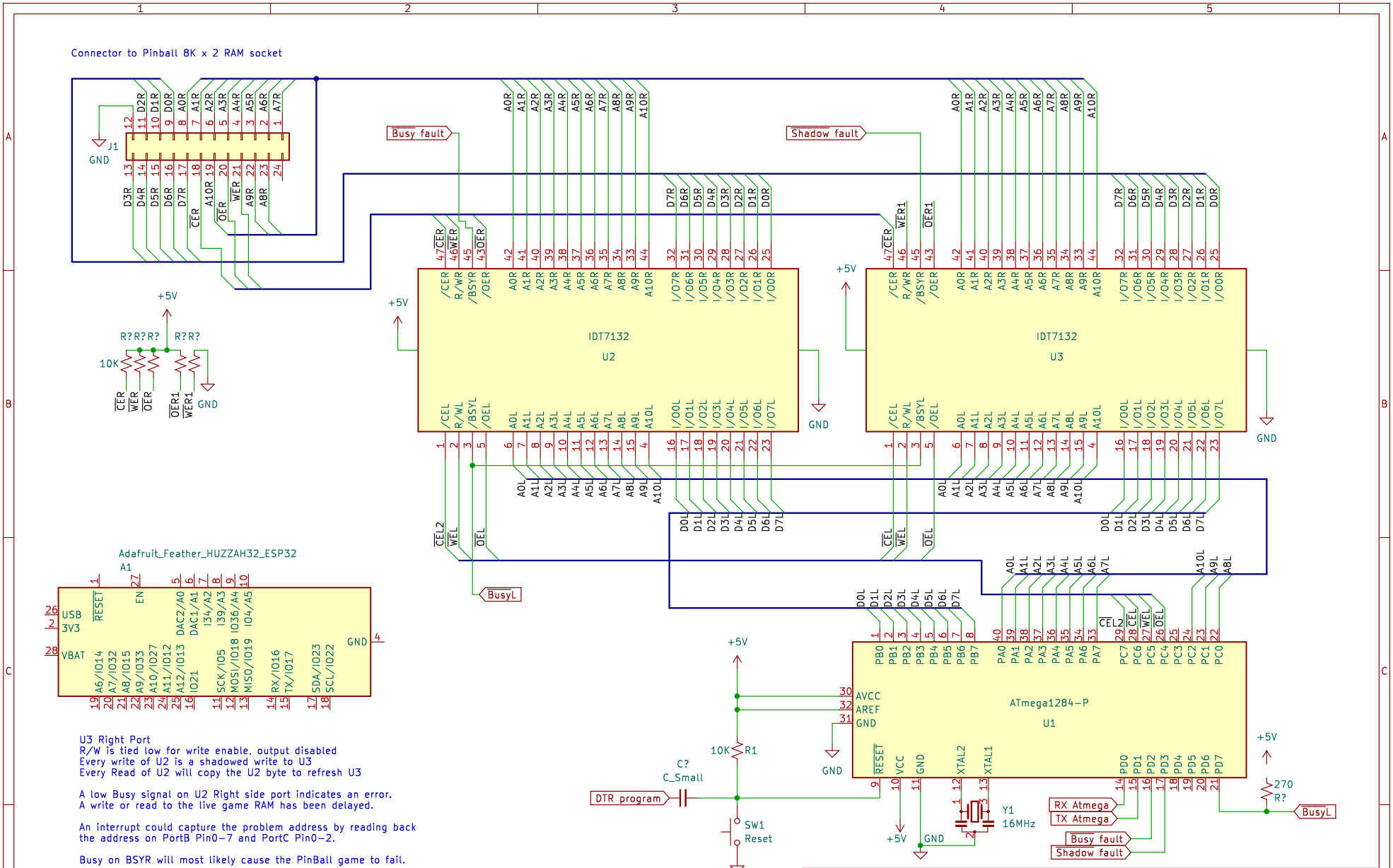

U3 Right Port
R/W is tied low for write enable, output disabled
Every write of U2 is a shadowed write to U3
Every Read of U2 will copy the U2 byte to refresh U3

A low Busy signal on U2 Right side port indicates an error.
A write or read to the live game RAM has been delayed.

An interrupt could capture the problem address by reading back
the address on PortB Pin0-7 and PortC Pin0-2.

Busy on BSYR will most likely cause the PinBall game to fail.

The ATmega 1284 will have a near realtime copy of the Game RAM by reading
the shadow RAM U3 using the Left interface of the dual Port

Writes to U3 RAM are not copied back to the live game RAM U2.

Careful timing and knowlege of which address in U2 are vulnerable will allow
some writes to the U2 RAM through the Left Dual Port

CEL2 controls the Left Port of U2

https://pdf1.alldatasheet.com/datasheet-pdf/view/65970/IDT/IDT7132.html

https://www.alldatasheet.com/datasheet-pdf/pdf/392244/ATMEL/ATMEGA1284.html

Tim Gopaul

Sheet: /
File: Pinball Memory Tap.kicad_sch

Title: Pinball Memory Tap

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