2.6.4 GD32E230Gx QFN28 pin definitions

Table 2-7. GD32E230Gx QFN28 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
BOOT0	1	I		Default: BOOT0
PF0-OSCIN	2	I/O	5VT	Default: PF0

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: I2C0_SDA Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Alternate: I2C0_SCL Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), CMP_OUT, I2C1_SCL(5) Additional: ADC_IN0, CMP_IM6, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), I2C1_SDA(5), EVENTOUT, TIMER14_CH0_ON(5) Additional: ADC_IN1, CMP_IP
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER14_CH0(5) Additional: ADC_IN2, CMP_IM7
PA3	9	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER14_CH1(5) Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4, CMP_IM4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK Additional: ADC_IN5, CMP_IM5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT, CMP_OUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT Additional: ADC_IN8
PB1	15	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
V_{SS}	16	P		Default: V_{SS}
V_{DD}	17	P		Default: V_{DD}
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(4), EVENTOUT
PA9(6)	19	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN(5), I2C0_SCL, CK_OUT
PA10(6)	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA13	21	I/O	5VT	Default: PA13/SWDIO Alternate: SWDIO, IFRP_OUT, SPI1_MISO(5)
PA14	22	I/O	5VT	Default: PA14/SWCLK Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	23	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART0_RX(3), USART1_RX(4), SPI1_NSS(5), EVENTOUT
PB3	24	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, I2S0_CK, EVENTOUT
PB4	25	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, EVENTOUT, I2C0_TXFRAME, TIMER16_BRKIN
PB5	26	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI,I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1 Additional: WKUP5
PB6	27	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	28	I/O	5VT	Default: PB7 Alternate:I2C0_SDA,USART0_RX,TIMER16_CH0_ON

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32E230G4 devices only.

(4) Functions are available on GD32E230G8/6 devices.

(5) Functions are available on GD32E230G8 devices only.

(6) Pin pair PA11/PA12 can be remapped instead of pin pair PA9/PA10 using SYSCFG_CFG0 register. ***Table 2-10. Port A alternate functions summary*** shows PA11/PA12 remap.