

		LOW NIBBLE																															
		X0	X1	X2	X3	X4	X5	X6	X7	X8	X9	XA	XB	XC	XD	XE	XF																
HIGH NIBBLE	0X	BRK s 7 6	ORA (zp,x) 5 5	CLE 2 1	SEE 2 1	TSB zp 4 4	ORA zp 3 3	ASL zp 4 4	RMB0 zp 4 4	PHP s 3 2	ORA # 2 2	ASL A 1 1	TSY 1 1	TSB a 5 5	ORA a 4 4	ASL a 5 5	BBR0 r 4 3	0X															
	1X	BPL/BNC r 2 2	ORA (zp),y 5 5	ORA (zp),z 5 5	BPL/BNC rr 3 3	TRB zp 4 4	ORA zp,x 3 3	ASL zp,x 4 4	RMB1 zp 4 4	CLC 1 1	ORA a,y 4 4	INC A 1 1	INZ 1 1	TRB a 5 5	ORA a,x 4 4	ASL/SFL a,x 5 5	BBR1 r 4 3	1X															
	2X	JSR a 5 5	AND (zp,x) 5 5	JSR (a) 7 7	JSR (a,x) 7 7	BIT zp 4 3	AND zp 3 3	ROL zp 4 4	RMB2 zp 4 4	PLP s 3 2	AND # 2 2	ROL A 1 1	TSY 1 1	BIT a 5 4	AND a 4 4	ROL a 5 5	BBR2 r 4 3	2X															
	3X	BMI/BNS r 2 2	AND (zp),y 5 5	AND (zp),z 5 5	BMI/BNS rr 3 3	BIT zp,x 4 3	AND zp,x 3 3	ROL zp,x 4 4	RMB3 zp 4 4	SEC 1 1	AND a,y 4 4	DEC A 1 1	DEZ 1 1	BIT a,x 5 4	AND a,x 4 4	ROL a,x 5 5	BBR3 r 4 3	3X															
	4X	RTI s 5 4	XOR (zp,x) 5 5	NEG A 2 1	ASR A 2 1	ASR zp 4 4	XOR zp 3 3	LSR zp 4 4	RMB4 zp 4 4	PHA s 3 2	XOR # 2 2	LSR A 1 1	TAZ 1 1	JMP a 3 3	XOR a 4 4	LSR a 5 5	BBR4 r 4 3	4X															
	5X	BVC r 2 2	XOR (zp),y 5 5	XOR (zp),z 5 5	BVC rr 3 3	ASR zp,x 4 4	XOR zp,x 3 3	LSR zp,x 4 4	RMB5 zp 4 4	CLI 1 1	XOR a,y 4 4	PHY s 3 2	TAB 1 1	AUG 4 1	XOR a,x 4 4	LSR/SFR a,x 5 5	BBR5 r 4 3	5X															
	6X	RTS s 4 3	ADC (zp,x) 5 5	RTN # 7 4	BSR rr 5 5	STZ zp 3 3	ADC zp 3 3	ROR zp 4 4	RMB6 zp 4 4	PLA s 3 2	ADC # 2 2	ROR A 1 1	TZA 1 1	JMP (a) 5 5	ADC a 4 4	ROR a 5 5	BBR6 r 4 3	6X															
	7X	BVS r 2 2	ADC (zp),y 5 5	ADC (zp),z 5 5	BVS rr 3 3	STZ zp,x 3 3	ADC zp,x 3 3	ROR zp,x 4 4	RMB7 zp 4 4	SEI 2 1	ADC a,y 4 4	PLY s 3 2	TBA 1 1	JMP (a,x) 5 5	ADC a,x 4 4	ROR a,x 5 5	BBR7 r 4 3	7X															
	8X	BRA r 2 2	STA (zp,x) 5 5	STA (d.SP),Y 6 5	BRA rr 3 3	STY zp 3 3	STA zp 3 3	STX zp 3 3	SMB0 zp 4 4	DEY 1 1	BIT # 2 2	TXA 1 1	STY a,x 4 4	STY a 4 4	STA a 4 4	STX a 4 4	BBS0 r 4 3	8X															
	9X	BCC r 2 2	STA (zp),y 5 5	STA (zp),z 5 5	BCC rr 3 3	STY zp,x 3 3	STA zp,x 3 3	STX zp,y 3 3	SMB1 zp 4 4	TYA 1 1	STA a,y 4 4	TXS 1 1	STX a,y 4 4	STZ a 4 4	STA a,x 4 4	STZ a,x 4 4	BBS1 r 4 3	9X															
	AX	LDY # 2 2	LDA (zp,x) 5 5	LDX # 2 2	LDZ # 2 2	LDY zp 3 3	LDA zp 3 3	LDX zp 3 3	SMB2 zp 4 4	TAY 1 1	LDA # 2 2	TAX 1 1	LDZ a 4 4	LDY a 4 4	LDA a 4 4	LDX a 4 4	BBS2 r 4 3	AX															
	BX	BCS r 2 2	LDA (zp),y 5 5	LDA (zp),z 5 5	BCS rr 3 3	LDY zp,x 3 3	LDA zp,x 3 3	LDX zp,y 3 3	SMB3 zp 4 4	CLV 1 1	LDA a,y 4 4	TSX 1 1	LDZ a,x 4 4	LDY a,x 4 4	LDA a,x 4 4	LDX a,y 4 4	BBS3 r 4 3	BX															
	CX	CPY # 2 2	CMP (zp,x) 5 5	CPZ # 2 2	DEW zp 6 6	CPY zp 3 3	CMP zp 3 3	DEC zp 4 4	SMB4 zp 4 4	INY 1 1	CMP # 2 2	DEX 1 1	ASW a 7 7	CPY a 4 4	CMP a 4 4	DEC a 5 5	BBS4 r 4 3	CX															
	DX	BNE/BZC r 2 2	CMP (zp),y 5 5	CMP (zp),z 5 5	BNE/BZC rr 3 3	CPZ zp 3 3	CMP zp,x 3 3	DEC zp,x 4 4	SMB5 zp 4 4	CLD 1 1	CMP a,y 4 4	PHX s 3 2	PHZ s 3 2	CPZ a 4 4	CMP a,x 4 4	DEC a,x 5 5	BBS5 r 4 3	DX															
	EX	CPX # 2 2	SBC (zp,x) 5 5	LDA (d.SP),Y 6 5	INW zp 6 6	CPX zp 3 3	SBC zp 3 3	INC zp 4 4	SMB6 zp 4 4	INX 1 1	SBC # 2 2	NOP 1 1	ROW a 7 7	CPX a 4 4	SBC a 4 4	INC a 5 5	BBS6 r 4 3	EX															
	FX	BEQ/BZS r 2 2	SBC (zp),y 5 5	SBC (zp),z 5 5	BEQ/BZS rr 3 3	PHW ##/s 5 5	SBC zp,x 3 3	INC zp,x 4 4	SMB7 zp 4 4	SED 1 1	SBC a,y 4 4	PLX s 3 2	PLZ s 3 2	PHW a/s 7 7	SBC a,x 4 4	INC a,x 5 5	BBS7 r 4 3	FX															
		X0	X1	X2	X3	X4	X5	X6	X7	X8	X9	XA	XB	XC	XD	XE	XF																
CE02	CE02V	45	42	80	80	74	67	57	55	56	54	48	48	60	60	64	64	25	20	48	48	24	20	51	44	72	67	64	64	72	76	64	48

OPCode	
Cycles on Original	Cycles on V-Version

Cyan Numbers indicate potential additional cycles, like for branches

Darker Gray = 6502

Gray = added by 65C02

Lighter Gray = added by 65CE02

Average CPI	Average MIPS (1MHz)
65CE02: 3.531	65CE02: 0.283
65CE02 Core: 3.348	65CE02V: 0.299