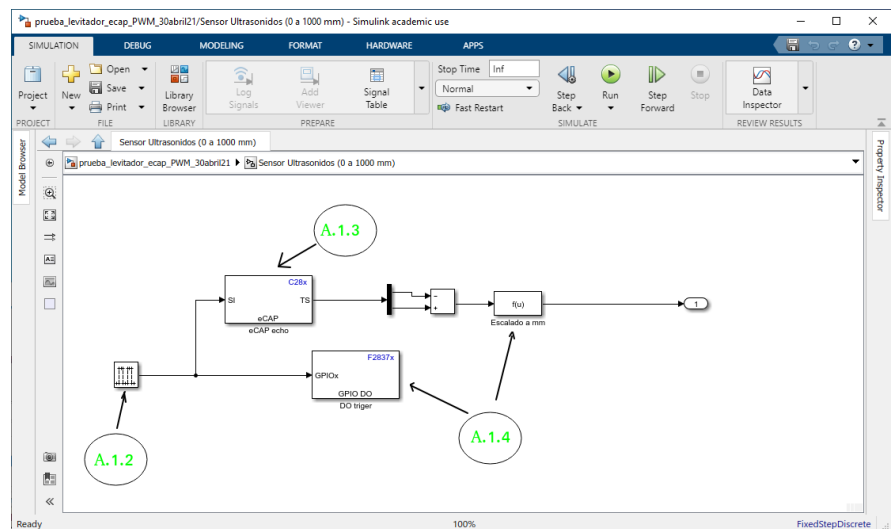


ANEXO A:

A. Configuración de los Bloques:

A.1 Bloque sensor de Ultrasonidos:



A.1.2 Generador de pulsos:

Block Parameters: Pulse Generator

else  
Y(t) = 0  
end

Pulse type determines the computational technique used.

Time-based is recommended for use with a variable step solver, while Sample-based is recommended for use with a fixed step solver or within a discrete portion of a model using a variable step solver.

Parameters

Pulse type: Sample based

Time (t): Use simulation time

Amplitude: 1

Period (number of samples): 100

Pulse width (number of samples): 1

Phase delay (number of samples): 0

Sample time: 0.001

☒ Interpret vector parameters as 1-D

OK Cancel Help Apply

A.1.3 Bloque ecap echo:

Block Parameters: eCAP echo

C28x eCAP (mask) (link)

Configure the settings of the F280x/F2833x/C2834x/F2802x/F2803x/F2805x/F2806x/F2807x/F28M3x/F2837x/F28004x processor for eCAP (Enhanced Capture)

General eCAP APWM Interrupt

Operating mode: eCAP

eCAPx pin: eCAP1

Counter phase offset value (0 ~ 4294967295): 0

☒ Enable counter Sync-In mode

☒ Enable software-forced counter synchronizing input

Sync output selection: CTR=PRD

Sample time: -1

OK Cancel Help Apply

Block Parameters: eCAP echo

C28x eCAP (mask) (link)

Configure the settings of the F280x/F2833x/C2834x/F2802x/F2803x/F2805x/F2806x/F2807x/F28M3x/F2837x/F28004x processor for eCAP (Enhanced Capture)

General eCAP APWM Interrupt

Event prescaler (integer from 0 to 31): 0

Select mode control: Continuous

Stop value after: Capture Event 2

☐ Enable reset counter after capture event 1 time-stamp

Select capture event 1 polarity: Rising Edge

☒ Enable reset counter after capture event 2 time-stamp

Select capture event 2 polarity: Falling Edge

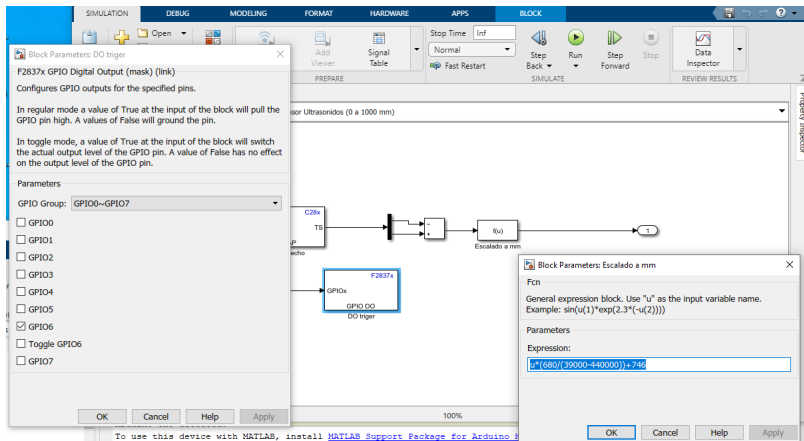
Time-Stamp counter data type: uint32

☐ Enable capture event status flag output

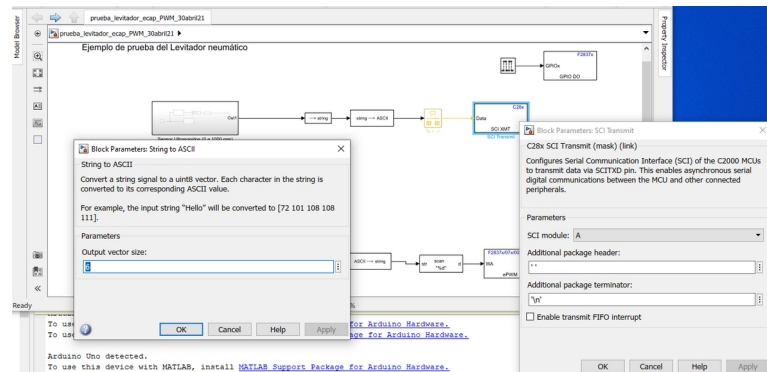
☐ Enable overflow status flag output

OK Cancel Help Apply

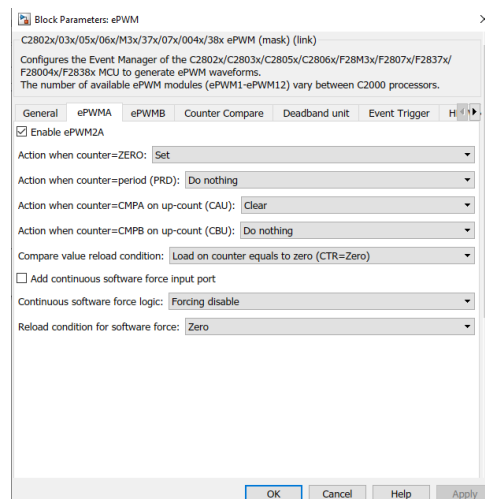
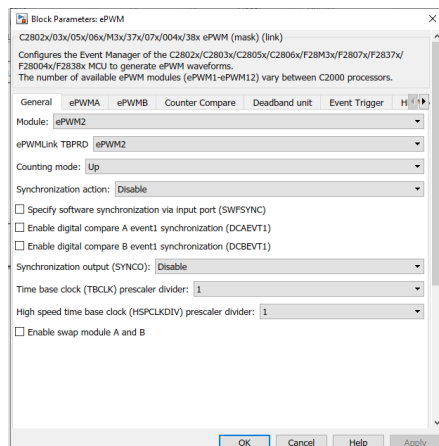
## A.1.4 Bloques Trigger y Escalado a milímetros:



## A.2 Bloques String to ASCII y Sci Transmit:



## A.3 Bloque PWM:



Block Parameters: ePWM

C2802x/03x/05x/06x/M3x/37x/07x/004x/38x ePWM (mask) (link)

Configures the Event Manager of the C2802x/C2803x/C2805x/C2806x/F28M3x/F2807x/F2837x/F28004x/F2838x MCU to generate ePWM waveforms.  
The number of available ePWM modules (ePWM1-ePWM12) vary between C2000 processors.

General ePWMA ePWB Counter Compare Deadband unit Event Trigger H11

ePWMLink CMPA Not Linked

CMPA units: Percentages

Specify CMPA via: Input port

CMPA initial value: 0

Reload for compare A Register (SHDWAMODE): Counter equals to zero

ePWMLink CMPB Not Linked

CMPB units: Clock cycles

Specify CMPB via: Specify via dialog

CMPB value: 32000

Reload for compare B Register (SHDWBMODE): Counter equals to zero

ePWMLink CMPC Not Linked

CMPC units: Clock cycles

Specify CMPC via: Specify via dialog

CMPC value: 32000

Reload for compare C Register (SHDWCMODE): Counter equals to zero

## A.4 Hardware settings:

Configuration Parameters: prueba\_levitador\_ecap\_PWM\_30abniz1/Configuration (Active)

Solver  
Data Import/Export  
Math and Data Types  
Diagnostics  
Hardware Implementation  
Model Referencing  
Simulation Target  
Code Generation

Target hardware resources

Groups  
Build options  
Clocking  
ADC\_A  
ADC\_B  
ADC\_C  
ADC\_D  
DAC  
ePWM  
eCAP  
eQEP  
I2C\_A  
I2C\_B  
SCI\_A  
SCI\_B  
SCI\_C  
SCI\_D  
SPI\_A  
SPI\_B  
SPI\_C  
eCAN\_A  
eCAN\_B  
Watchdog

Desired CPU Clock in Mhz: 100

☐ Use internal oscillator

Oscillator clock (OSCLK) frequency in Mhz: 10

☒ Auto set PLL based on OSCLK and CPU clock

System PLL multiplier (SYSPLLMULT) [1-127.75]: 40

System clock divider (SYSDIVSEL) [1.2, 4.6, ..., 124, 126]: 4

Achievable SYSCLKOUT in Mhz = (OSCLK\*SYSPLLMULT)/SYSDIVSEL: 100

Low-Speed Peripheral Clock Prescaler (LSPCLK): SYSCLKOUT/1

Low-Speed Peripheral Clock (LSPCLK) in Mhz: 100

OK Cancel Help Apply

Configuration Parameters: prueba\_levitador\_ecap\_PWM\_30abniz1/Configuration (Active)

Solver  
Data Import/Export  
Math and Data Types  
Diagnostics  
Hardware Implementation  
Model Referencing  
Simulation Target  
Code Generation

ADC\_A  
ADC\_B  
ADC\_C  
ADC\_D  
DAC  
ePWM  
eCAP  
eQEP  
I2C\_A  
I2C\_B  
SCI\_A  
SCI\_B  
SCI\_C  
SCI\_D  
SPI\_A  
SPI\_B  
SPI\_C  
eCAN\_A  
eCAN\_B  
Watchdog  
GPIO0\_7  
GPIO8\_15  
GPIO16\_23  
GPIO24\_31  
GPIO32\_39

Suspension mode: Free\_run

Number of stop bits: 2

Parity mode: None

Character length bits: 8

Desired baud rate in bits/sec: 115200

Baud rate prescaler (BRR = (SCIHBAUD << 8) | SCILBAUD): 108

Closest achievable baud rate (LSPCLK/(BRR+1)\*8) in bits/sec: 114679

Communication mode: Raw\_data

☐ Blocking mode

Data byte order: Little\_Endian

Pin assignment(Tx): GPIO42

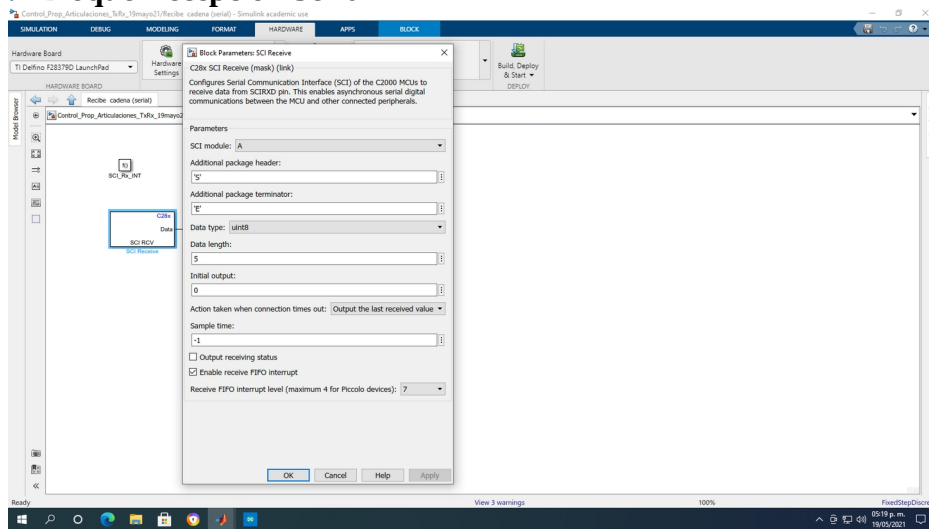
Pin assignment(Rx): GPIO43

OK Cancel Help Apply

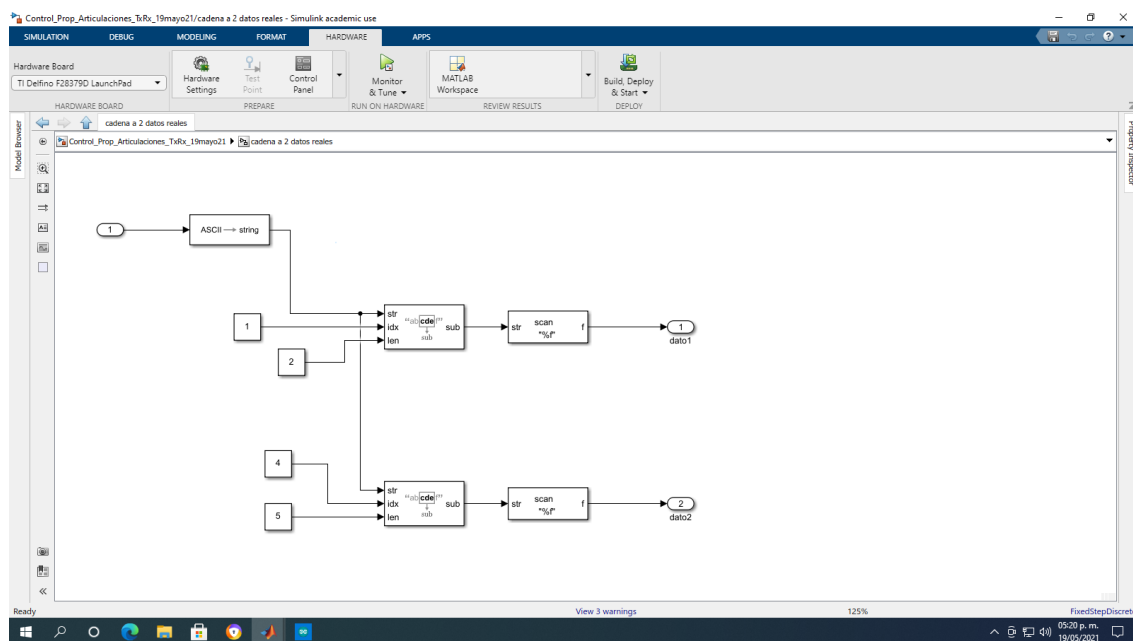
## ANEXO B:

### B. Configuración de los Bloques:

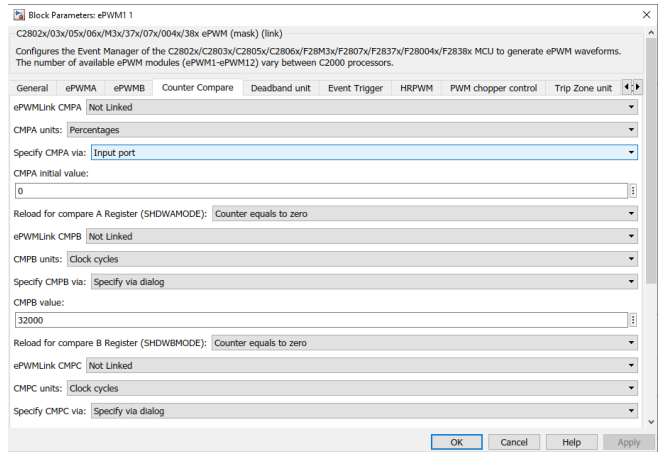
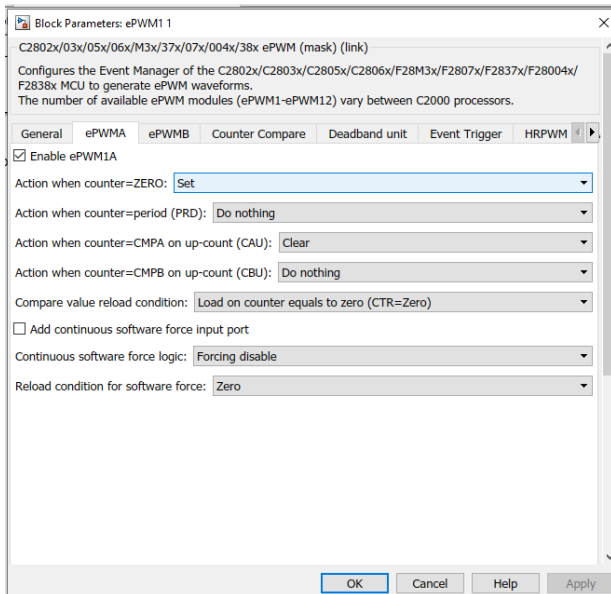
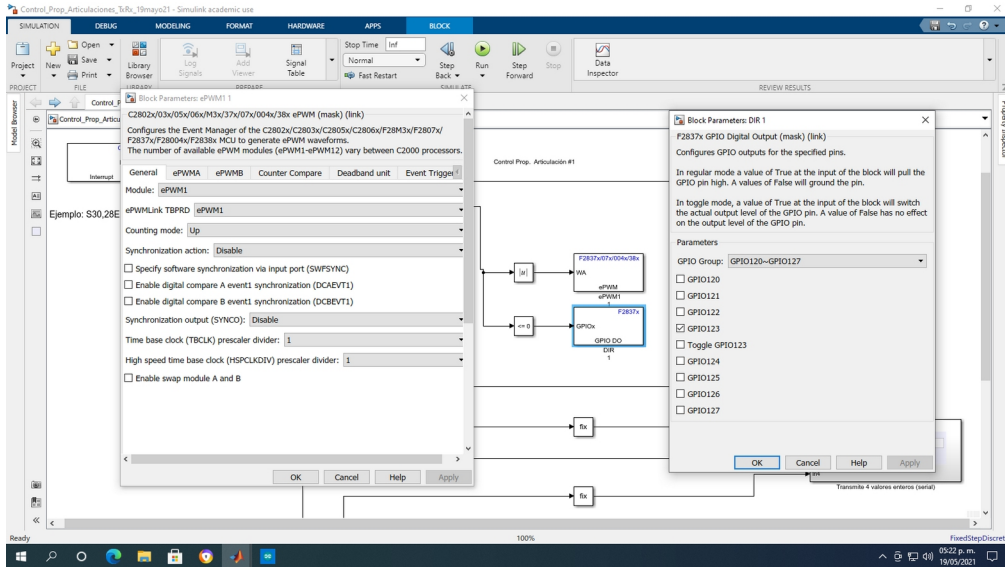
#### B.1 Bloque Recepción Serial



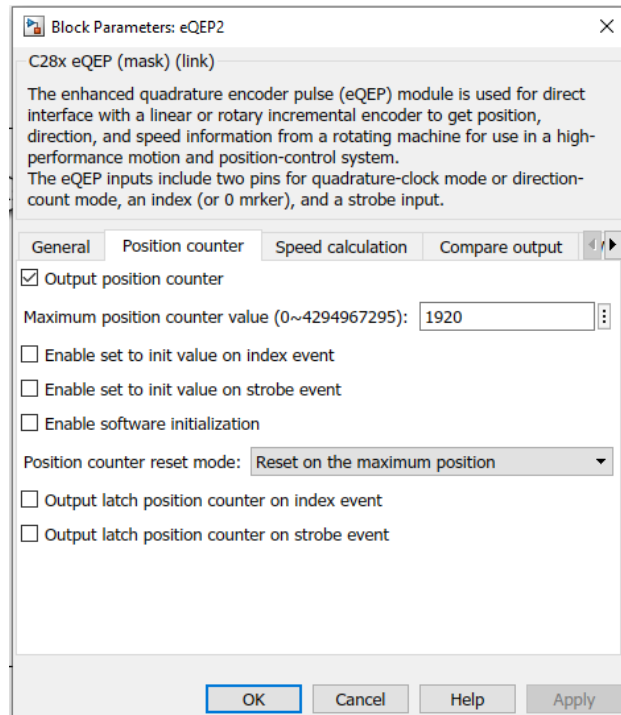
#### B.2 Bloque Cadena a 2 valores reales



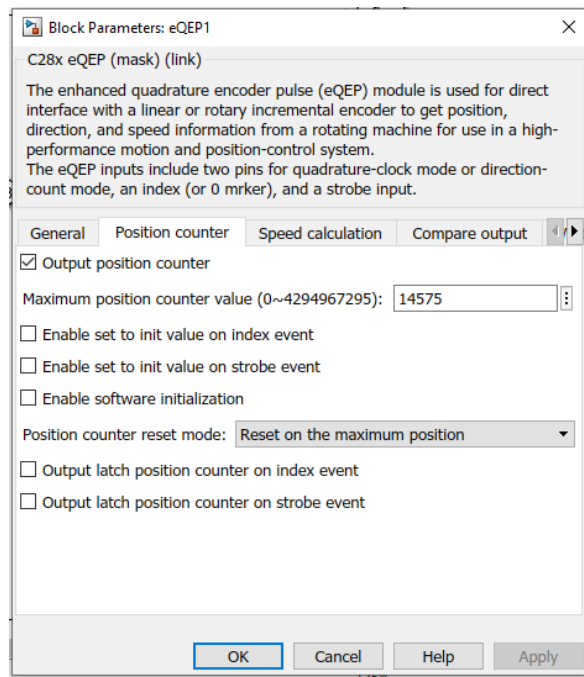
## B.3 Bloques ePWM1 y Dirección de giro (DIR).



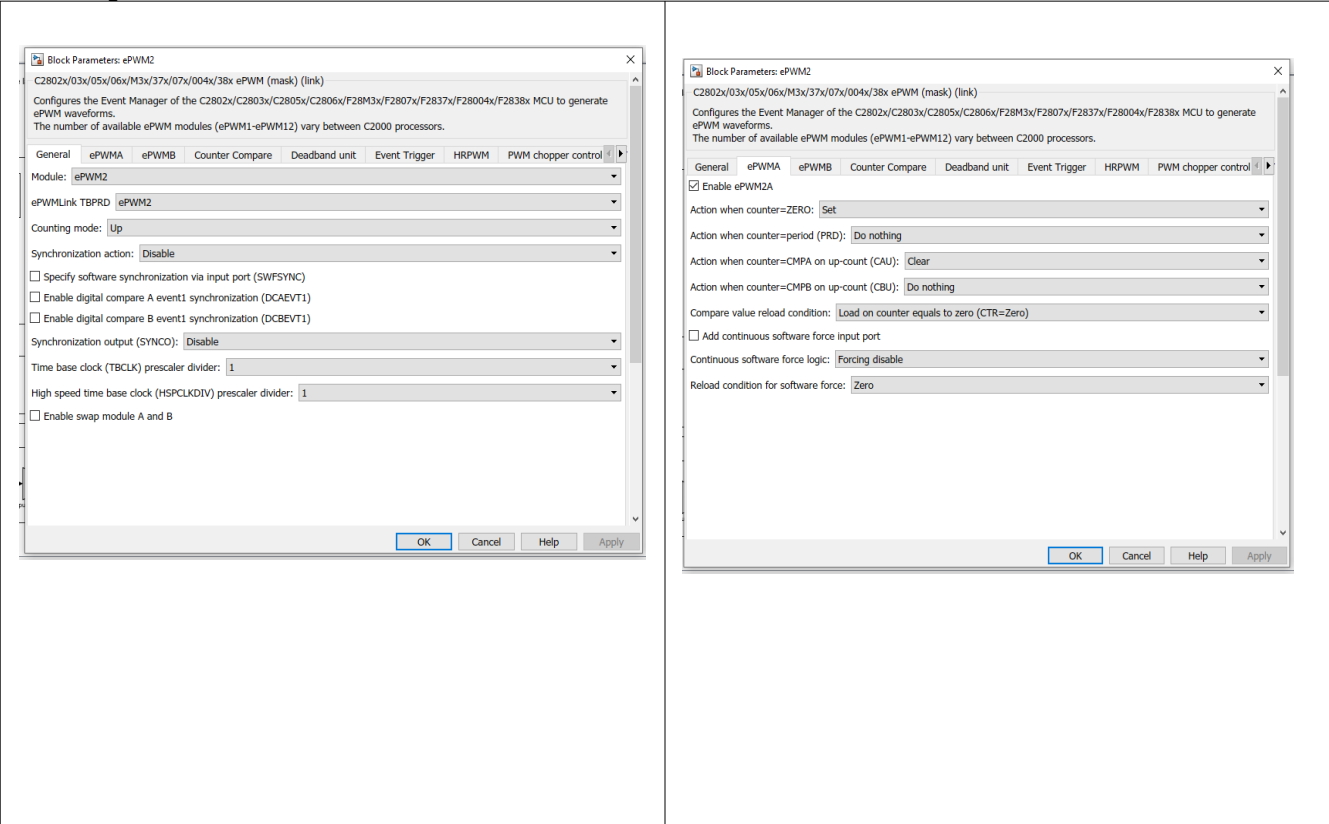
## B.4 Bloque Manejo del Encoder 2 (eQep2) de la articulación 1



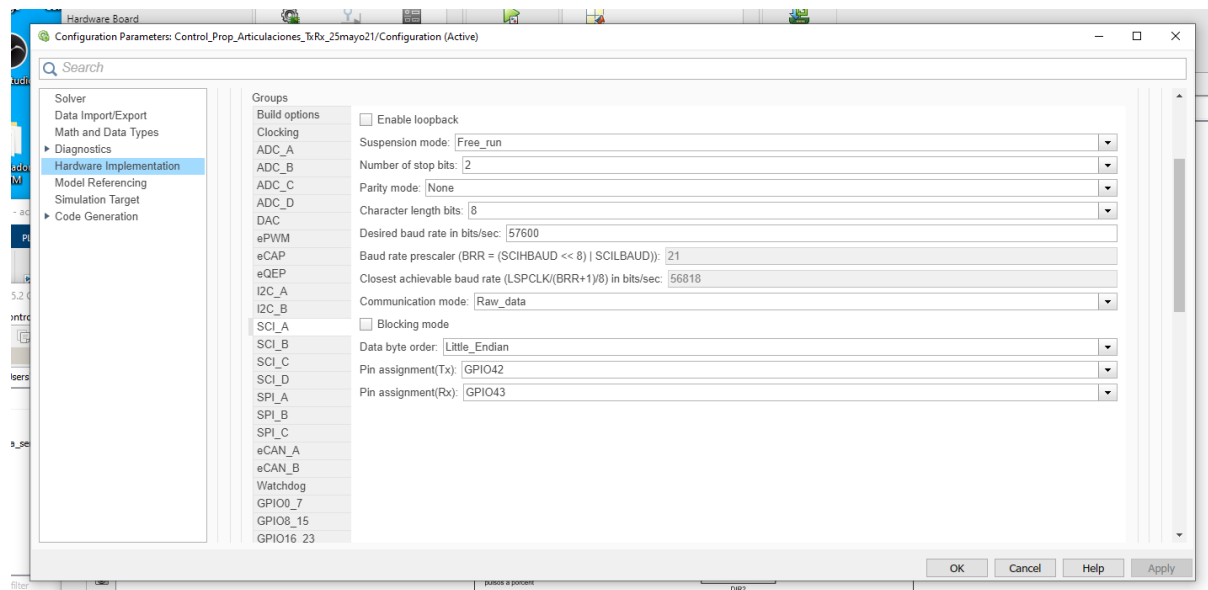
## B.5 Bloque Encoder 1 (eQep1) de la Articulación 2



## B.6 Bloque ePWM2



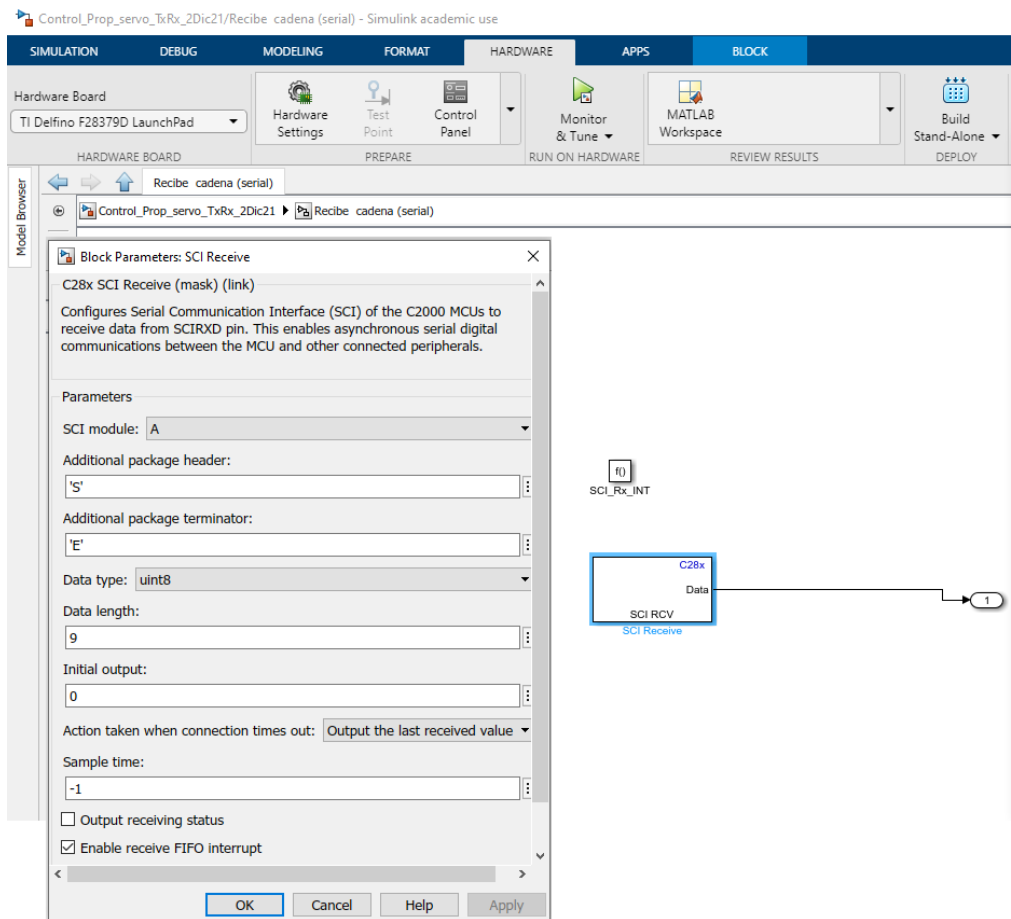
## B.7 Configuración del Puerto Serial SCI\_A:



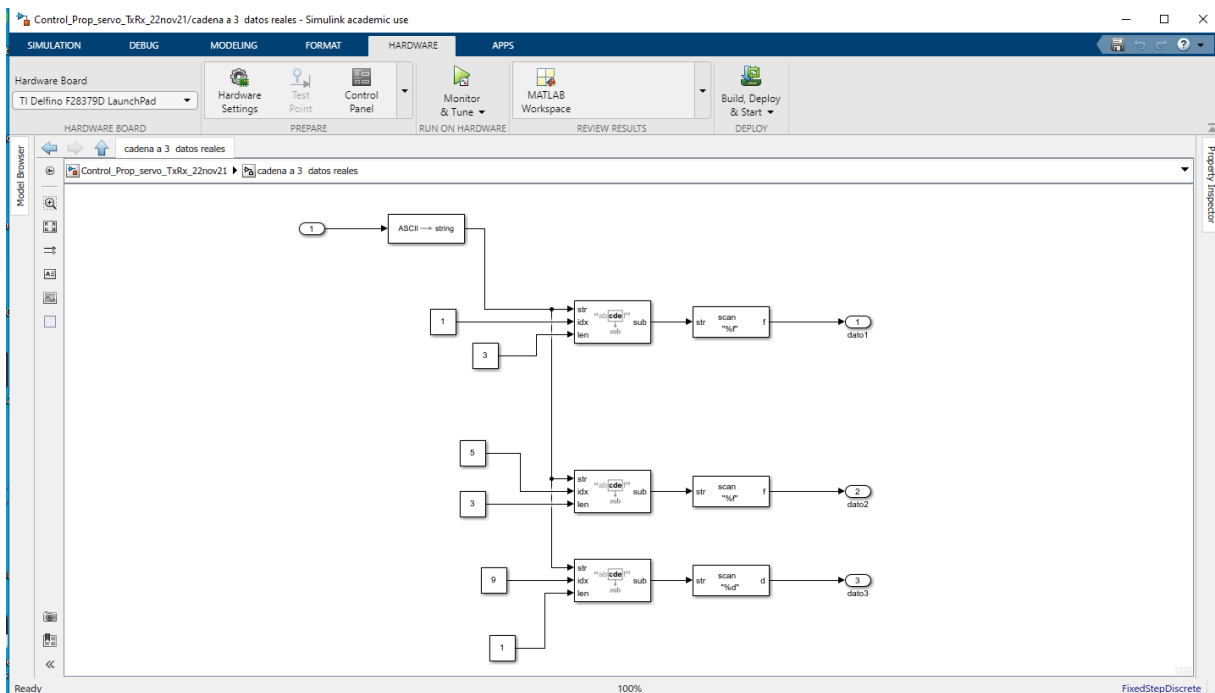
## ANEXO C:

### C. Configuración de los Bloques:

#### C.1 Bloque de Recepción Serial



#### C.2 Bloque Cadena a 2 valores reales





### C.3 Bloques ePWM1 y Dirección de giro (DIR) del motor de la correa.

**Block Parameters: ePWM1**

C2802x/03x/05x/06x/M3x/37x/07x/004x/38x ePWM (mask) (link)

Configures the Event Manager of the C2802x/C2803x/C2805x/C2806x/F28M3x/F2807x/F2837x/F28004x/F2838x MCU to generate ePWM waveforms.  
The number of available ePWM modules (ePWM1-ePWM12) vary between C2000 processors.

General ePWMA ePWMB Counter Compare Deadband unit Event Trigger HRPWM PWM chopper control Trip Zone

☒ Enable ePWM1A

Action when counter=ZERO: Set

Action when counter=period (PRD): Do nothing

Action when counter=CMPA on up-count (CAU): Clear

Action when counter=CMPB on up-count (CBU): Do nothing

Compare value reload condition: Load on counter equals to zero (CTR=Zero)

☐ Add continuous software force input port

Continuous software force logic: Forcing disable

Reload condition for software force: Zero

OK Cancel Help Apply

**Block Parameters: ePWM1**

C2802x/03x/05x/06x/M3x/37x/07x/004x/38x ePWM (mask) (link)

Configures the Event Manager of the C2802x/C2803x/C2805x/C2806x/F28M3x/F2807x/F2837x/F28004x/F2838x MCU to generate ePWM waveforms.  
The number of available ePWM modules (ePWM1-ePWM12) vary between C2000 processors.

General ePWMA ePWMB Counter Compare Deadband unit Event Trigger HRPWM PWM chopper control

ePWMLink CHPA Not Linked

CHPA units: Percentages

Specify CHPA via: Input port

CHPA initial value: 0

Reload for compare A Register (SHDWMODE): Counter equals to zero

ePWMLink CHPB Not Linked

CHPB units: Clock cycles

Specify CHPB via: Specify via dialog

CHPB value: 32000

Reload for compare B Register (SHDWMODE): Counter equals to zero

ePWMLink CHPC Not Linked

CHPC units: Clock cycles

Specify CHPC via: Specify via dialog

CHPC value: 32000

Reload for compare C Register (SHDWMODE): Counter equals to zero

ePWMLink CHPD Not Linked

CHPD units: Clock cycles

OK Cancel Help Apply

**Block Parameters: ePWM1**

C2802x/03x/05x/06x/M3x/37x/07x/004x/38x ePWM (mask) (link)

Configures the Event Manager of the C2802x/C2803x/C2805x/C2806x/F28M3x/F2807x/F2837x/F28004x/F2838x MCU to generate ePWM waveforms.  
The number of available ePWM modules (ePWM1-ePWM12) vary between C2000 processors.

General ePWMA ePWMB Counter Compare Deadband unit Event Trigger HRPWM PWM chopper control

Module: ePWM1

ePWMLink TBPRD ePWM1

Counting mode: Up

Synchronization action: Disable

☐ Specify software synchronization via input port (SWFSYNC)

☐ Enable digital compare A event1 synchronization (DCAEVT1)

☐ Enable digital compare B event1 synchronization (DCBEVT1)

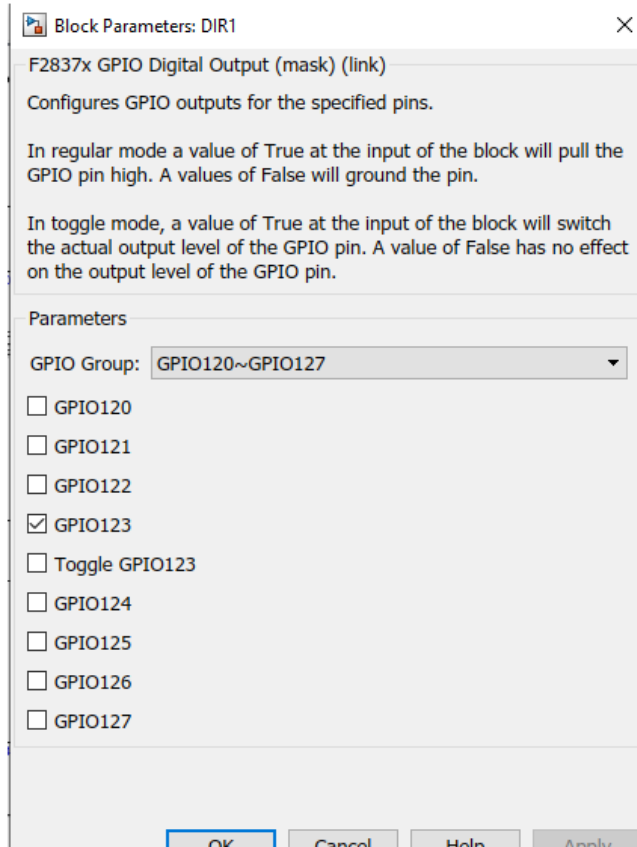
Synchronization output (SYNCO): Disable

Time base clock (TBCLK) prescaler divider: 1

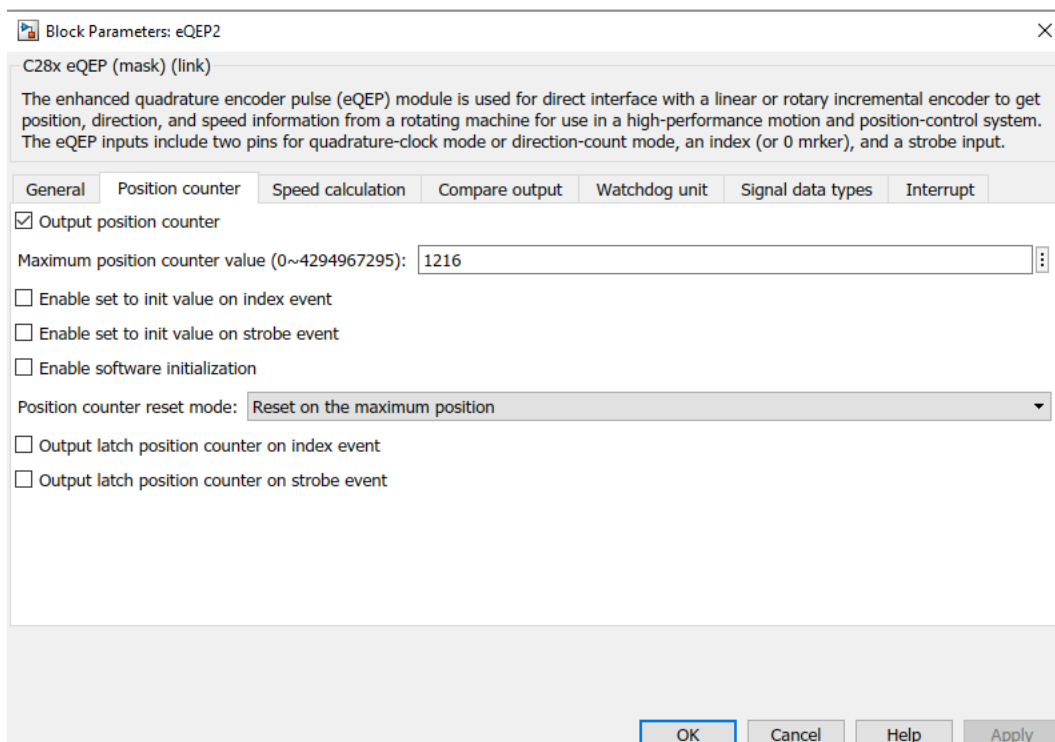
High speed time base clock (HSPCLKDIV) prescaler divider: 1

☐ Enable swap module A and B

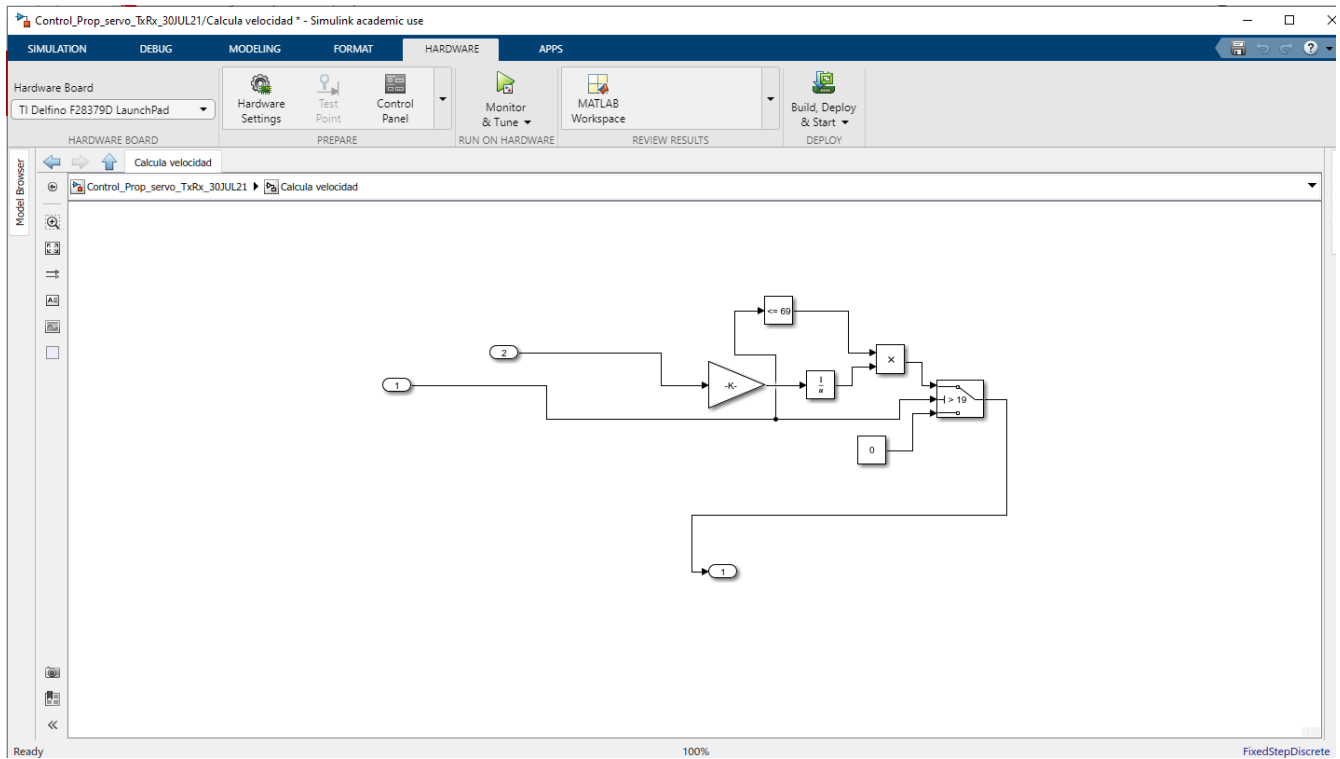
OK Cancel Help Apply



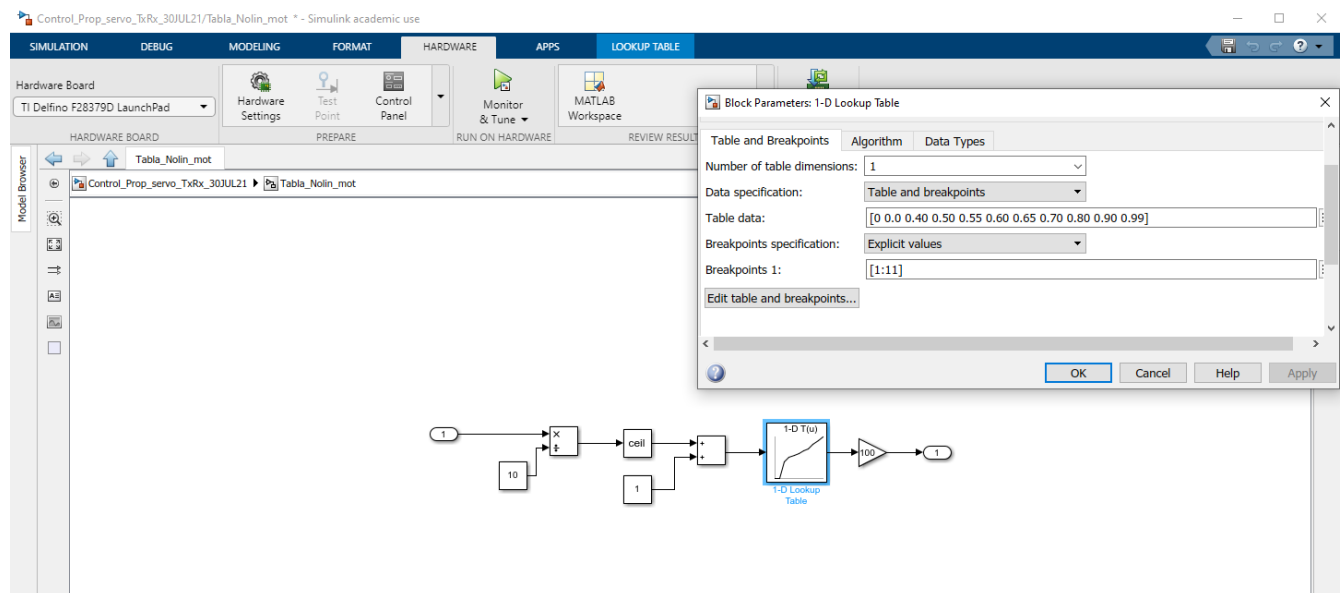
## C.4 Bloque Manejo del Encoder 2 (eQep2) del motor de la correa



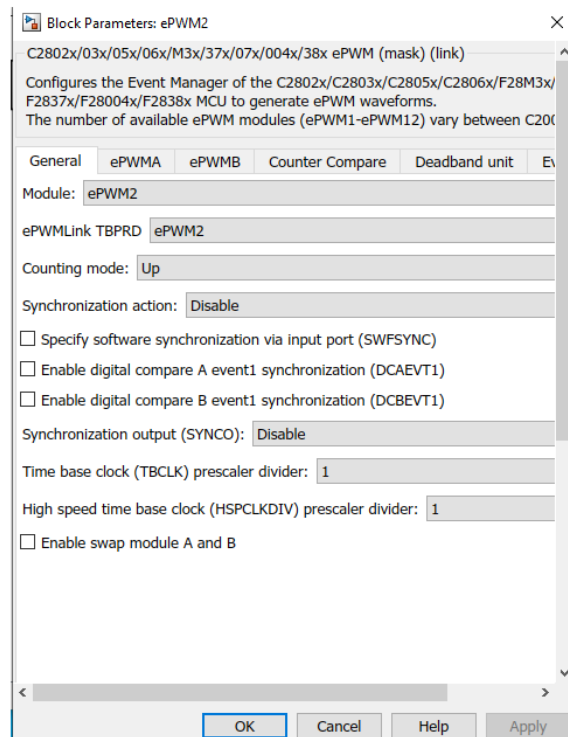
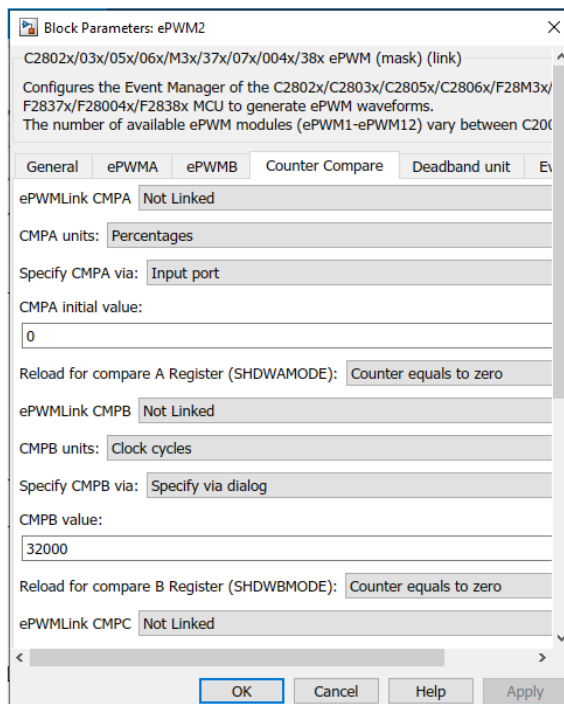
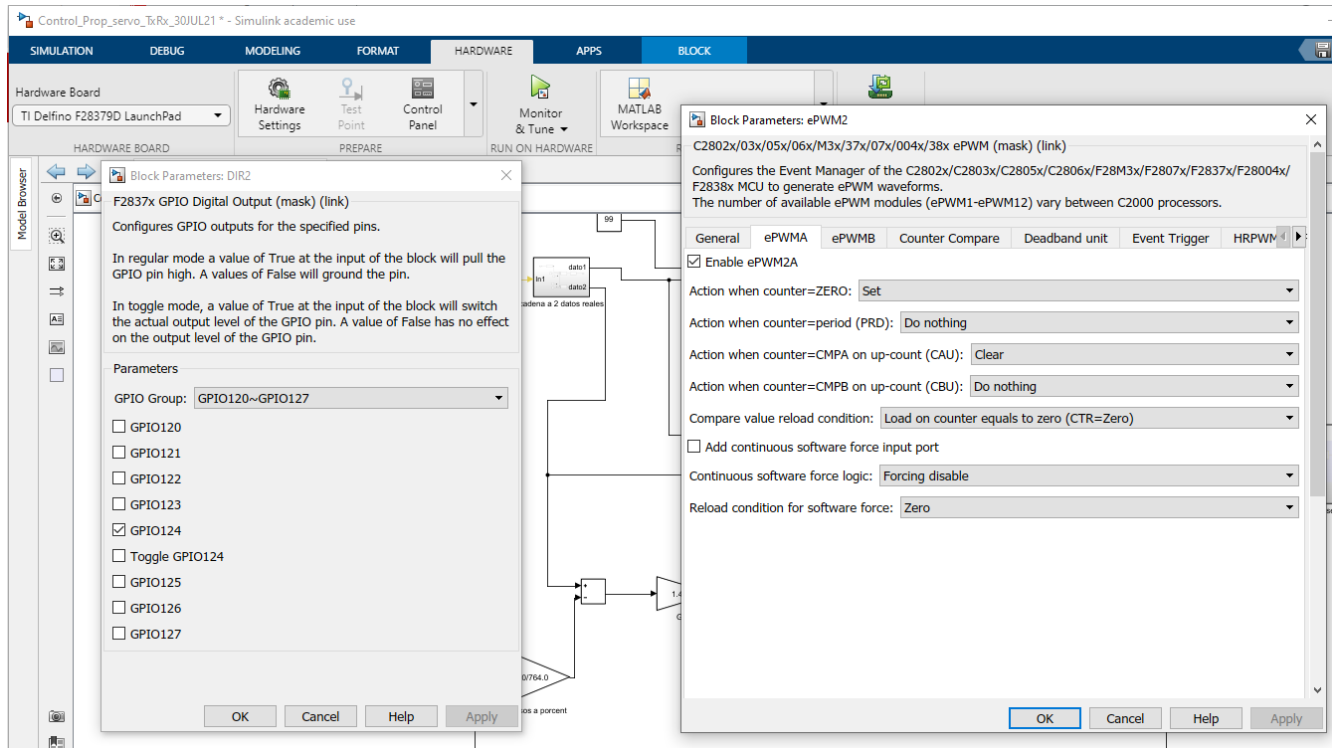
## C.5 Bloque para el calculo de la velocidad a partir de Información del encoder.



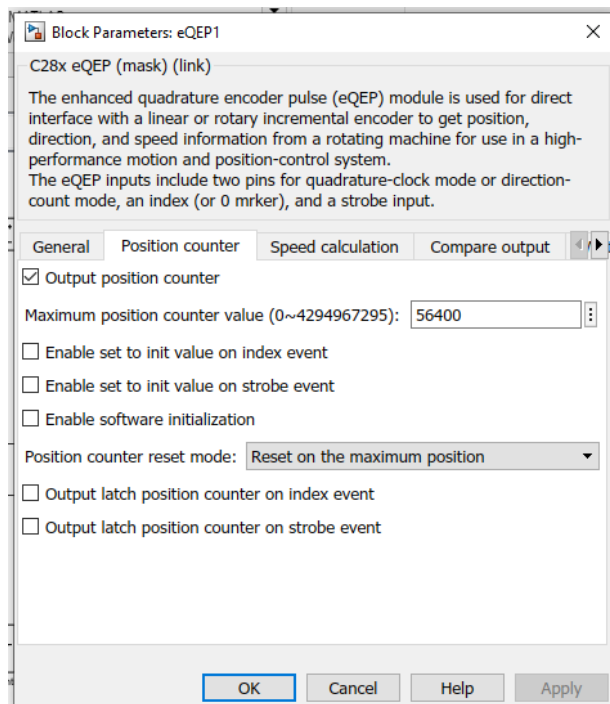
## C.6 Bloque para manejo de la no linealidad del motor del tornillo.



## C.7 Bloques ePWM2 y Dirección de giro (DIR) del motor del tornillo.



## C.8 Bloque Manejo del Encoder 1 (eQep1) del motor del tornillo.



## C.9 Configuración controlador PID.

