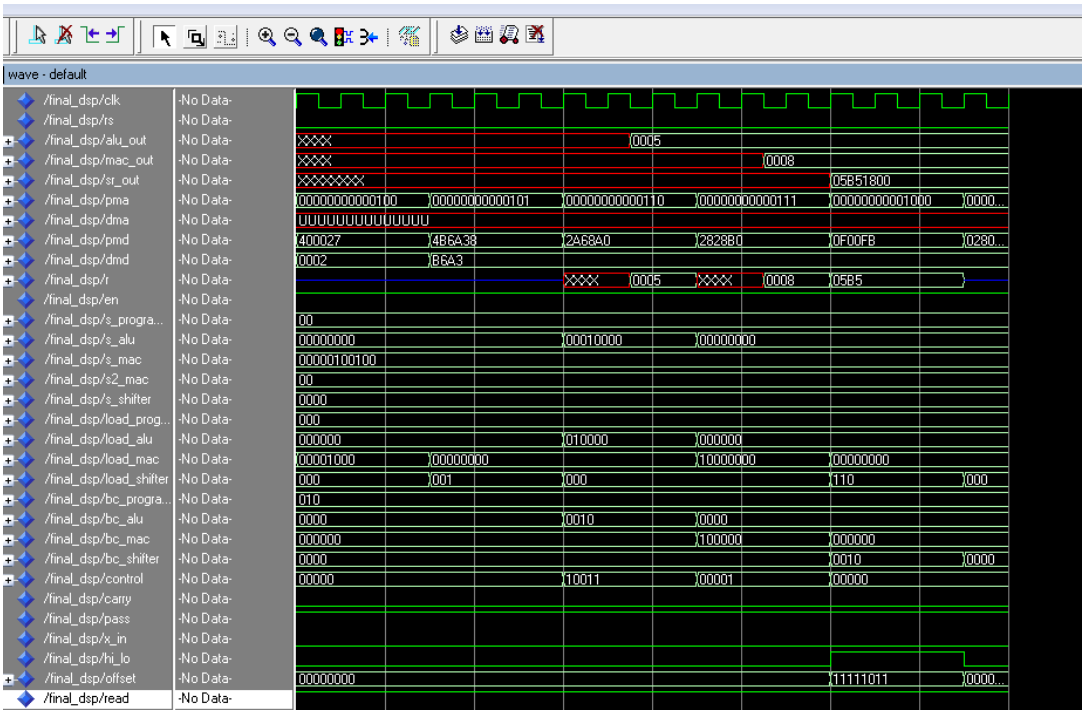

C:/Users/een455spring14_g2/Desktop/VHDL1/program_memory.vhd *

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ln #

```
1   library ieee;
2           use ieee.std_logic_1164.all;
3           use ieee.std_logic_unsigned.all;
4
5   entity program_memory is
6           port(PMA: IN std_logic_vector(13 downto 0);
7                PMD: INOUT std_logic_vector(23 downto 0);
8                read: IN std_logic
9               );
10  end program_memory;
11
12  architecture behav of program_memory is
13
14        type data is array(0 to 19) of std_logic_vector(23 downto 0);
15
16        begin
17          process(read, PMA)
18
19             variable memory: data;
20             variable index: integer;
21
22             begin
23               memory(1) := "010000000000000000100000";   -- 0. AX0 = 2
24               memory(2) := "010000000000000000110101";   -- 1. AY1 = 3
25               memory(3) := "010000000000000001000010";   -- 2. MX0 = 4;
26               memory(4) := "010000000000000000100111";   -- 3. MY1 = 2;
27               memory(5) := "010010110110101000111000";  -- 4. SI = B6A3
28
29               memory(6) := "001010100110100010100000";   -- 4. AR = AX0 + AY1;
30               memory(7) := "001010000010100010110000";   -- 5. MR0 = MX0 * MY1
31
32               memory(8) := "000001110000000011111011";   -- 6. SR = Lshift (-5)
33               memory(9) := "000000101000000000000000";   -- Idle
34
35
36                 index:=conv_integer(PMA);
37                 if (read = '1') then
38                   PMD<=memory(index);
39                 end if;
40           end process;
41  end behav;
```