UVM Interview Questions

1. With numerous user-defined test cases available, the question arises: how does one select and execute a specific test case?

2. What does typical testbench_top contains?

3. Why it's better to have all the fields registered to uvm_field_* macros in uvm_sequence_item?

4. Is there a particular component within UVM where it is necessary to write the assertion property?

5. Is it possible to set the config_db multiple times? If yes, how?

6. What's uvm_pool?

7. In tb_top module, we use the run_test("test_name") method to initiate the phases in UVM. But why we won't declare any handle for the class test inside top module?

8. What are all the arguments we've in type_id::**create()** method? Explain.

9. How to use a variable in uvm test and same variable in the sequence? Scenario is: a scenario where UVM tests has an int variable declared. (Variable increments in the test). The same variable/datatype is used as a checker in the sequence once the body completes.

10. Where should the reference model of the DUT be housed: within the driver, scoreboard, or another component?

11. Suppose I wish to drive only a single transaction. For example, I am driving '1'b1 to a 1-bit signal of the DUT at every positive edge of the clock. In this scenario, I do not require my sequence item. So, can I refrain from using a sequencer and driver handshake? Will the testbench function properly without any sequencer and sequence item?

12. What is the difference between early randomization and late randomization of sequences?

13. What is the difference between sequence_item, sequence and sequencer with respect to UVM?

14. Why phasing is used? What are the different phases in uvm?

15. In run_phase(), is it necessary to call super.run_phase(phase)?

16. Difference between m_sequencer and p_sequencer in UVM.

17. Advantages of TLM over mailbox?

18. The driver is raising objection but never dropping them, and the requirement is to move to the next phase (extract_phase) after #50 timeunits. However, since all objections are not dropped in the run_phase, the simulation is not progressing to the extract_phase. How can this be resolved?

19. Using uvm_event, we can pass data (transaction class) when an event is triggered. Then, why do we need TLM/Analysis ports in UVM?

20. Callback vs Factory in UVM.

21. Given an IP, you are the owner of the IP, what are the steps you start with and when will it be signed off?

22. What is the difference between a pipelined and a non-pipelined sequence-driver model?

23. What is the difference between get_next_item() and get() methods in UVM driver class?

24. How can you stop all sequences running on a sequencer?

25. Why should we register a class with factory?

26. What is the concept of objections and where are they useful?

27. How can we implement a simulation timeout mechanism in UVM methodology?

28. What is p_sequencer & where it's used?

29. Can we have a user-defined phase in UVM?

30. If, during a project, we observe high functional coverage (approaching 100%) and low code coverage (e.g., < 60%), what conclusions can be drawn?

31. During a project, if we observe high code coverage (close to 100%) and low functional coverage (say < 60%) what can be inferred?