Design of 2-Stage Op-Amp using gm/id methodology

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***Abstract* – In this paper we will design 2-stage Operational amplifier using gm/id method. Also, why and how to choose the gm/id of a particular transistor is discussed.**

Index Terms* - 2-stage Operational amplifier, *gm/id methodology.

I. Introduction

Let's start with the specifications of the given op-amp. As shown in Table 1 the specification includes OLDC (Open Loop DC Gain), Gain Bandwidth Product (GBP) also called open loop unity gain bandwidth, Phase Margin (PM), CMRR, power dissipation and load Capacitor (C_L).

TABLE I
SPECIFICATIONS

SR. no	System Specifications	Values
1	OLDC	1000 (v/v)
2	GBP	10 MHz
3	PM	75°
4	CMRR	50 db
5	Power Dissipation	30 uW
6	C_L	100f F

II. *Finding design parameters like gm, I_D and C_c from given specifications and deciding (gm/id) for each transistor : -*

As shown in figure 1 we have two stages and as we need total gain of 1000 (v/v) lets divide this gain as 40 (v/v) and 25 (v/v) for first stage and second stage respectively. The reason for deciding gain of first stage as high is if we connect a resistive load then gain of second stage will decrease thus first stage will provide the major part of gain in such situations.

a. *Using Phase Margin, we can find position of non-dominant pole: -*

As given phase margin is 75°, the phase of op-amp at GBP frequency would be -105°, thus the equation will be $-105^o = -\tan^{-1}(GBP/P_{dominant}) - \tan^{-1}(GBP/P_{non\text{-}dominant}) - \tan^{-1}(GBP/Z)$, where Z is Right Half Plane Zero. We are including zero cancelling resistor thus the effect of zero can be neglected and also the phase of dominant pole at GBP frequency will be approximately -90^o. Thus, solving above equation we get the relation $P_{non\text{-}dominant} = 3.73$ GBP.

As we know $P_{non\text{-}dominant} = gm_6/(C_L + C_c) \approx gm_6/C_L$. Here we will put a condition on C_c as we made an approximation and

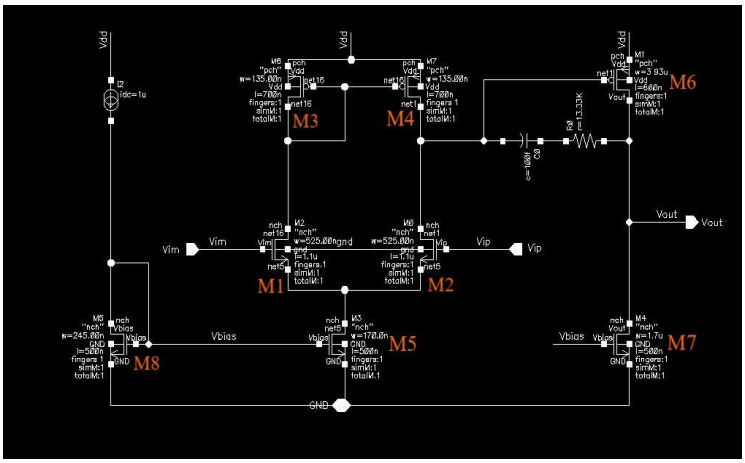


Figure 1. Circuit Diagram

the condition is $C_c \leq 2 * C_L$, hence whatever gm_6 we will calculate we will take 3 times the value in our design.

Thus, $gm_6/C_L = 3.73 * 2*\pi*10*10^6$ from which we get $gm_6 \approx 25$ uS. But as we will take three times the value so we get $gm_6 = 75$ uS.

b. *Using GBP to find value of $gm_{1,2}$: -*

We know that for 2 stage op-amp GBP is gm_1/C_c let's use $C_c = 100$f F, hence $gm_1/C_c \geq 2*\pi*10*10^6 \Rightarrow gm_1 \geq 6.28$ uS. Let's take $gm_1 = 7$ uS.

c. *Using gain of 1st and 2nd stages we find the required intrinsic gains of transistors M_1, M_2 and M_6: -*

As we decided that the gain of first stage is 40 (v/v), thus $gm_1/(gds_2 + gds_4) \geq 40$ where gds_2, gds_4 are channel length conductance of the mosfets M_1 and M_2. Let's take $gds_2 = gds_4$ so $gm_1/gds_2 \geq 80$. Similarly, for second stage $gm_6/gds_6 \geq 50$, for $gds_6 = gds_7$.

d. *Deciding **(gm/id)** for each transistor: -*

The transistors which provide gain should have higher (gm/id) as for the same current flowing through branch they should have higher gm compared to the transistors which are working as load. Also, for current mirror transistors like M_5, M_7, M_8 the (gm/id) should be such that they are in strong inversion region.

Hence, we came up with following (gm/id) values

TABLE 2
GM/I_D VALUES

SR. no	Transistor	(gm/id) value
1	M_1	20
2	M_2	20
3	M_3	10
4	M_4	10
5	M_5	15
6	M_6	15
7	M_7	15
8	M_8	15

III. *Deciding W and L for each transistor: -*

Before finding W and L we will find $id_{1,2}$ and $id_{6,7}$. From values $gm_{1,2}$, $gm_{6,7}$ and (gm/id) we found $id_{1,2,3,4} = 0.35$ uA , $id_5 = 0.7$u A, $id_{6,7} = 5$u A and $id_8 = 1$u A (biasing current).

M_1 and M_2 : -

From our previous discussion $gm_1 / gds_2 \geq 80$, from our (gm/id) plots of Nmos we look at the gm/gds vs $(gm/id)_{|20}$ and find the smallest channel length L for which this condition satisfies in our case it turns out to be $L_{1,2} = 1.1$ um. From id/W vs $(gm/id)_{|20}$ for L = 1.1 um we found $W_{1,2} = 526$ nm.

M_3 and M_4 : -

As $(gm/id)_{3,4} = 10$ and $id_{3,4} = 0.35$ uA we found $gm_{3,4} = 3.5$ uA. From $gm_1 / gds_2 \geq 80$ and $gm_1 = 7$ uS we get $gds_2 = gds_4 = 87.5$ nS. Hence, $(gm/gds)_{3,4} \geq 40$. Repeating same procedure to find $L_{3,4}$ and $W_{3,4}$ using Pmos (gm/id) graphs we found $L_{3,4} = 700$ nm and $W_{3,4} = 133$ nm.

M_6: -

Using $gm_6 / gds_6 \geq 50$ and $(gm/id)_{|6} = 15$ we found $L_6 = 600$ nm from gm/gds vs (gm/id) plot and $W_6 = 3.93$ um using (id/w) vs (gm/id) plot for L = 600 nm. Also, $gm_6 / gds_6 \geq 50$ and $gm_6 = 75$ uS we found $gds_6 \leq 1.5$ uS.

M_5, M_7 and M_8: -

We will use M_8 as the transistor which will set the bias for M_5 and M_7, as all of them must be in saturation for the current to be properly mirrored we took their (gm/id) = 15. To make sure that M_8 is in saturation we need $V_{gs} > V_{th}$ as due to diode connection $V_{gd} = 0$ V. Now from V_{th} vs (gm/id) plots we found that maximum value of V_{th} for Nmos at $(gm/id)_{|15}$ is around 350 mV. Hence, we looked at V_{gs} vs $(gm/id)_{|15}$ for Nmos such that $V_{gs} > 350$ mV and this condition was satisfied by L= 500 nm, thus $L_8 = 500$ nm. From this we select $L_5 = L_7 = 500$ nm. As we choose biasing current of 1 uA from M_8 using id/W vs $(gm/id)_{|15}$ we found $W_8 = 246$ nm. Now from current scaling we get $W_5 = 172.2$ nm and $W_7 = 1.23$ um. But during simulation we got less current in M_7 thus we changed $W_7 = 1.7$ um. A zero-cancelling resistor of value $1/gm_6 = 13.33$ KΩ is used. Table 3 summarizes the values of W and L for each transistor.

TABLE 3
W AND L VALUES

SR. no	Transistor	W	L
1	M_1	526 nm	1.1 um
2	M_2	526 nm	1.1 um
3	M_3	133 nm	700 nm
4	M_4	133 nm	700 nm
5	M_5	172.2 nm	500 nm
6	M_6	3.93 um	600 nm
7	M_7	1.7 um	500 nm
8	M_8	246 nm	500 nm

IV. *Simulation Results: -*

❖ *Input Common Mode Range (ICMR): -*

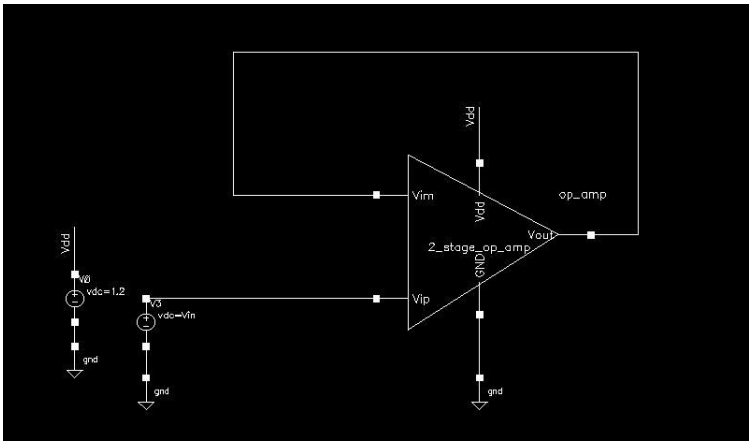


Figure 2. Voltage Follower

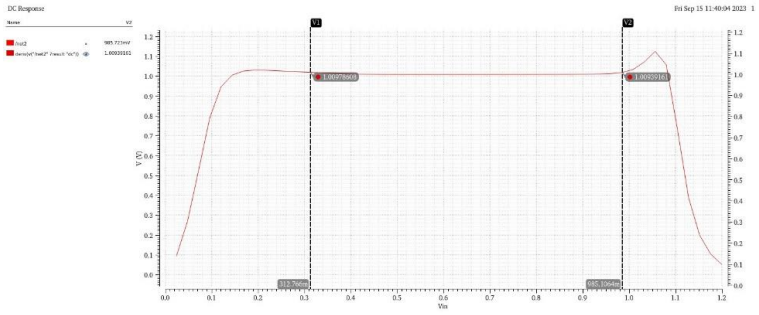


Figure 3. Input common mode range

We made a voltage follower and changed the input to at "+" terminal from 0 to V_{DD} (1.2 V), from this we will get a graph of V_{out} vs V_{in}. The Figure 3 shows the derivative of this graph from which we can see that the graph is constant from around 312 mV to 985 mV and this is our ICMR.

❖ *Output Voltage Swing Range (OVSR): -*

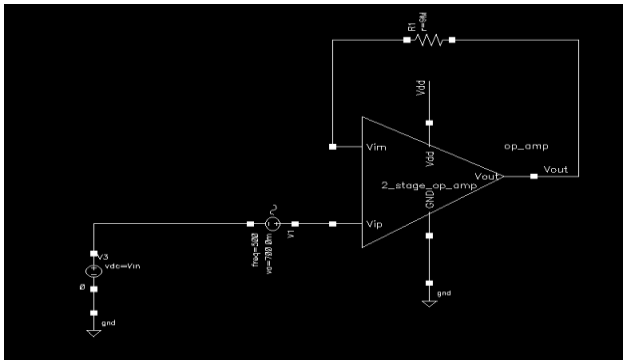


Figure 4 OVSR circuit

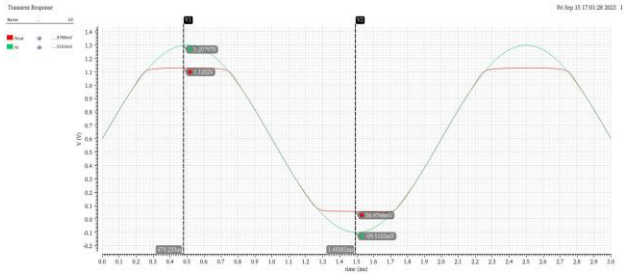


Figure 5 OVSR circuit

❖ *Differential Gain (A_{dm}): -*

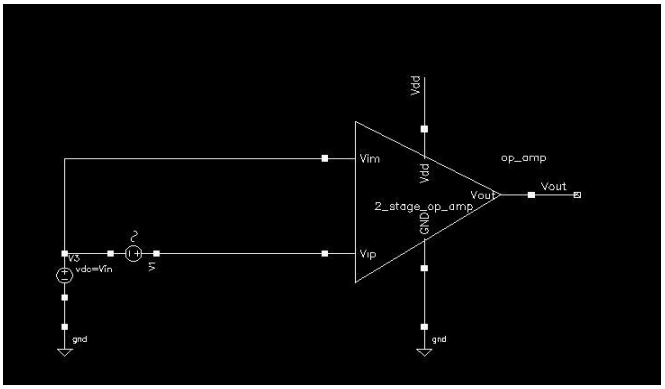


Figure 6 Differential gain circuit

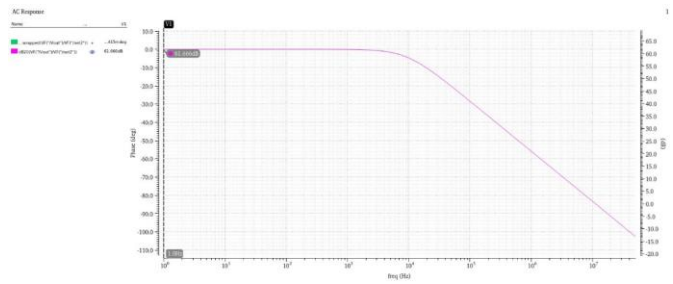


Figure 7 Bode Plot

We found that bode plot has 61.66 db open loop gain.

❖ *Common Mode Gain (A_{cm}): -*

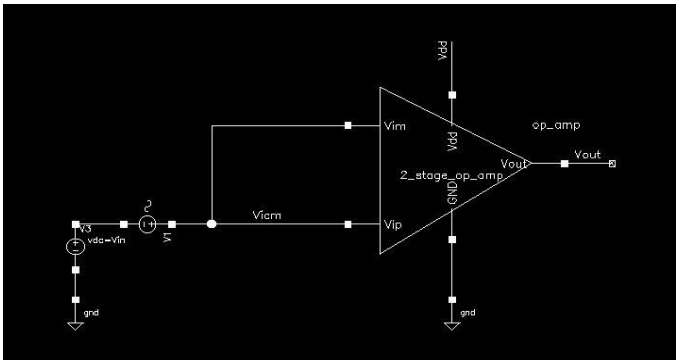


Figure 8 Common Mode Circuit

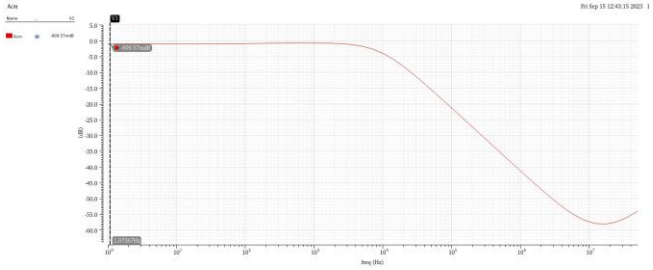


Figure 9 Common Mode Bode plot

From this we can calculate CMRR = 62.66 db. The input offset voltage is 210.16 uV

❖ *Slew Rate: -*

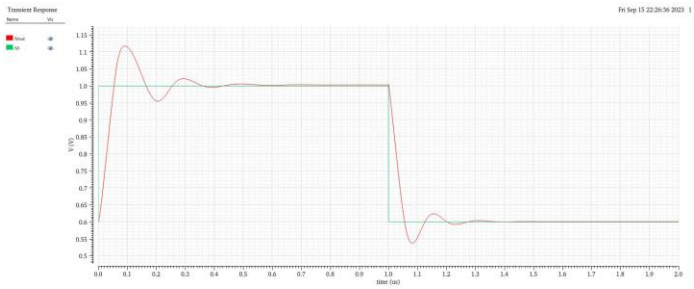


Figure 10 Positive Slew rate

Positive Slew Rate is 7.867 V/u sec.

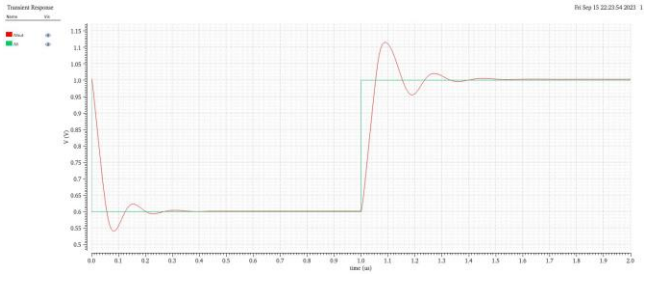


Figure 11 Positive Slew rate

Negative Slew rate -7.636 V/u sec.

❖ *Settling Time Response: -*

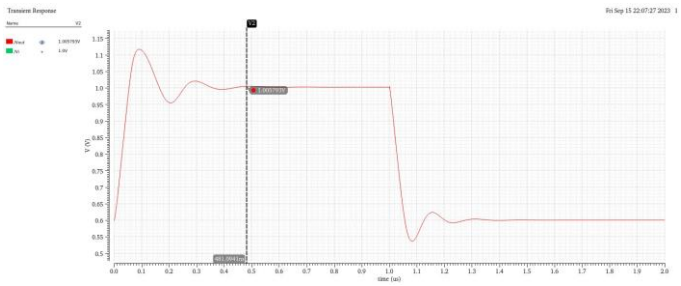


Figure 12 Settling Time Response

❖ *Stability Analysis: -*

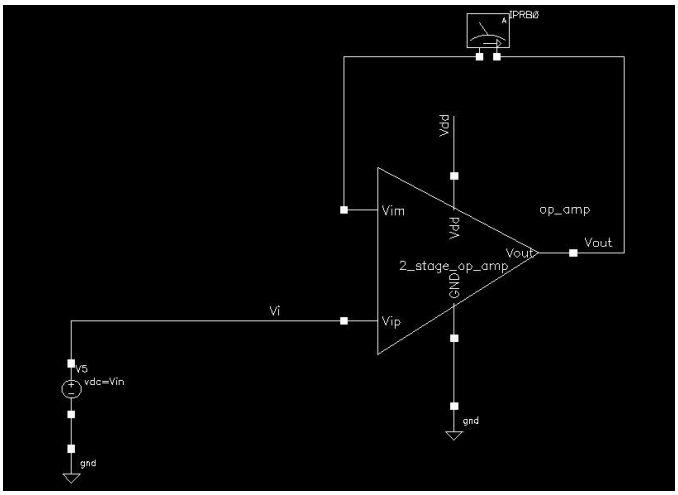
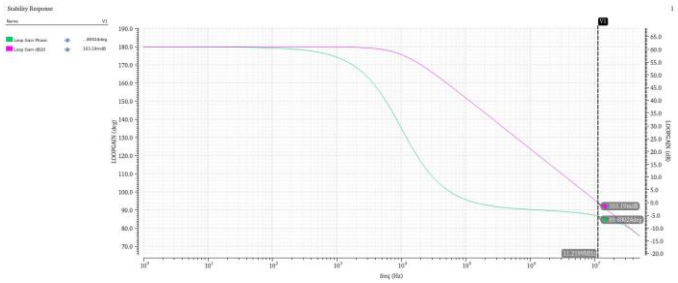


Figure 13 Stability Analysis Circuit



Phase margin = 86.7952 Deg at frequency = 11.2324 MHz.

Figure 14 Open Loop Bode Plot