Lab #7

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1. Objective

In this lab we will build a circuit which is able to set and actively control the speed of an electric motor. Devices needed for this lab include devices that we have previously used (transistors, counters, OpAmps) as well as completely new ones (such as bi-polar transistors, photo-transistors, etc.)

2. Introduction/Overview

A circuit that uses feedback for active control over a certain quantity (such as speed, temperature, etc) is called a servo control loop. Servo control loops are used in a wide array of applications, such as controlling the temperature in an oven and having a functioning robot. For this experiment, we will build a circuit that controls the speed of the motor (in revolutions per minute) by adjusting the amount of current that the motor receives. The process by which the circuit works is described below:

I) A disc with a single slit in it is attached to a motor

II) The disc rotates when the motor is turned on, and every time light (generated by an LED) falls on a phototransistor, the phototransistor causes current to conduct generating a CLK pulse.

III) A counter then counts the number of CLK pulses between RESET pulses.

IV) Right before a RESET pulse arrives, the counter output is stored in an 8-bit D-latch via the LATCH output.

V) The counter output is then converted from a binary digital signal to an analog signal via an R-2R DAC network.

VI) The analog output is then compared to an analog voltage (in which the analog voltage represents the set point for the speed of the motor)

VII) The output is then used to control the current through the motor via a power transistor.

The entire circuit is shown below:

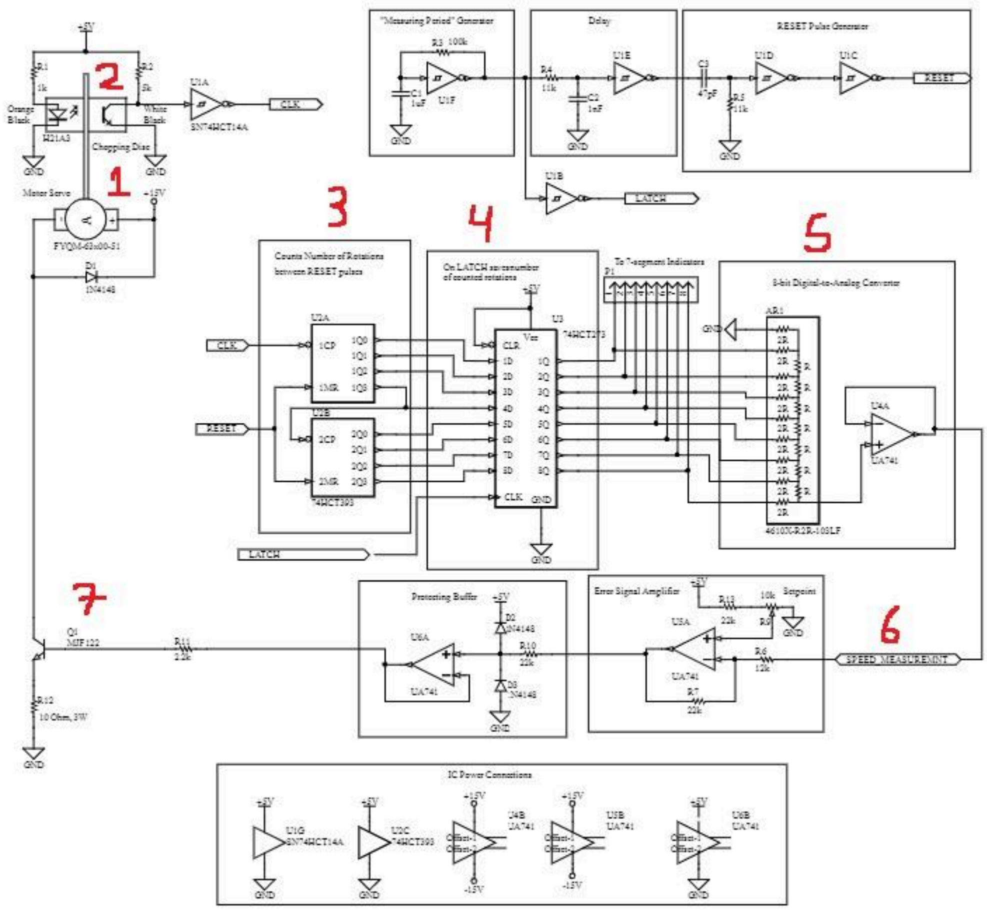

Figure 1: Circuit Schematic of the RPM Motor Control Lab.

3. Troubleshooting

1) For the first section (corresponding to part (a) of Figure 3), My graph was odd and unexpected. The graph had the shape of an irregular oscillating wave pattern like below:

I decided to continue with the experiment and once I measured the input and output across the section corresponding to part (b) of Figure 3, I knew something was wrong, the graph gave results which were inconsistent with the descriptions in the lab manual. I decided that the best option was to analyze if all of the circuit components were connected properly. I initially did not detect any false connections. However, then I realized that none of the unused inputs were grounded. I then grounded all the unused inputs, and the output turned into the expected output that was outlined in the lab manual.

2) For the section in which we build the counter (right before we start building the D-latch and the DAC):

If we place our counter facing away from the rest of the circuit, we get the following output below (for $V_{cc} = 5\ V$ and a square input wave with amplitude 4 V and offset 0 V). What happens exactly is odd; namely, the output will start at "00" but then progress to "80" with the zero in the tens digit flickering at an increasing rate until it reaches a steady value of 8. It is also noteworthy that if we physically press down on the wire corresponding to Q3 (Pin #9 on the 74HC273 device), the output instantly goes to "80".

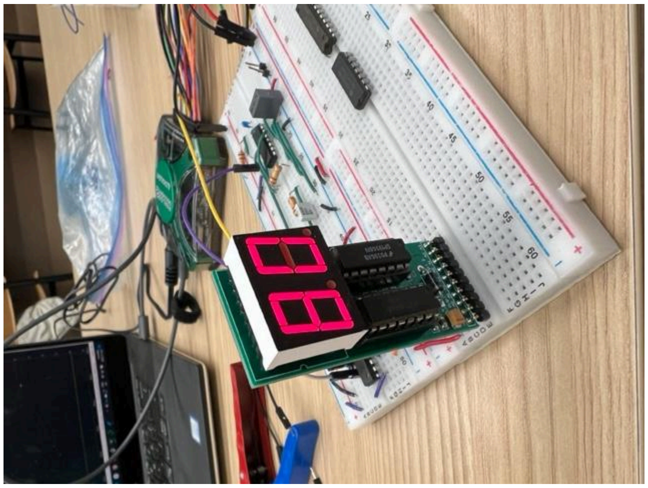

Figure 2: Output of flawed circuit (counter facing outwards)

If we place our counter facing towards our circuit (with the same input, $V_{cc} = 5\ V$ and a square input wave with amplitude 4 V and offset 0 V), we find that the counter will oscillate between "00" and "01" at the frequency of the square wave input. In image form:

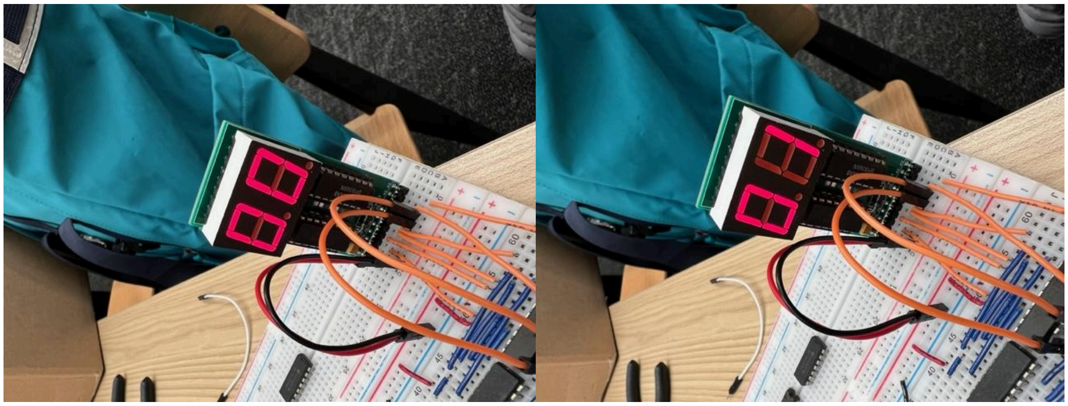

Figure 3: Output of flawed circuit (counter facing inwards)

I decided to do a thorough check of the placement of the wires from the very beginning (while also using the Ch. 1 wires from the AD2 to check to see if the wires were connected properly in the first place). I quickly realized my mistake; namely, the LATCH and RESET pins were mixed up (i.e the LATCH output from the Schmidt-

Trigger inverter was going to the input that was designed for the RESET output and vice versa). As soon as I switched the placement of the LATCH and RESET outputs, the circuit started working perfectly.

3) Once I finished the construction of the circuit with the motor and ran a test, I received a strange result; namely the motor was spinning perfectly and we could easily change the speed of the motor by adjusting the potentiometer, but the counter was displaying a constant 0. Because the motor itself was working as intended, I figured there was a problem with the connection to the counter. I started by troubleshooting the very first part of the circuit; the LATCH and RESET generator. I checked the wiring of the LATCH and RESET generator and I could not find any mistakes. I then decided to troubleshoot by measuring the actual output of the individual LATCH and RESET outputs and compared it to the expected output (the LATCH section should provide a square wave with 50% symmetry with an amplitude = 5 V, the input voltage of the LATCH and RESET generator, while the RESET output should be a series of pulses). I confirmed the outputs for the LATCH and RESET portions of the circuit. However, when I checked the CLK output, I was getting a constant value of 0 V (the expected output should have been an oscillatory wave with repeated small bumps). I thought there was something wrong with the inverter itself, so I manually inputted a square wave with a symmetry of 10% into the inverter, and I detected an inverted version of the input for the output, as expected. I figured that there was a problem with the motor, so I switched my motor with the motor of one of my friends, and the counter began working perfectly.

4. Experiment

4.1 Schmidt-Trigger Inverters

The image on the left below is the logic diagram for a Schmidt-Trigger inverter, (Schmidt-Trigger inverters incorporate a process called "Hysteresis" in its operation - described in more detail in the next paragraph). The diagram below indicates that Ai and Yi corresponds to the input and output of the Schmidt-Trigger inverter respectively (here, i stands for the input number; 1, 2, 3, 4, 5, and 6). The second number on the left diagram below represents the corresponding pin number on the right diagram below. For the Schmidt-Trigger Inverter test (Section 4.1), we are only using pins #1 and #2 (pin #1 as out input and pin #2 as our output).

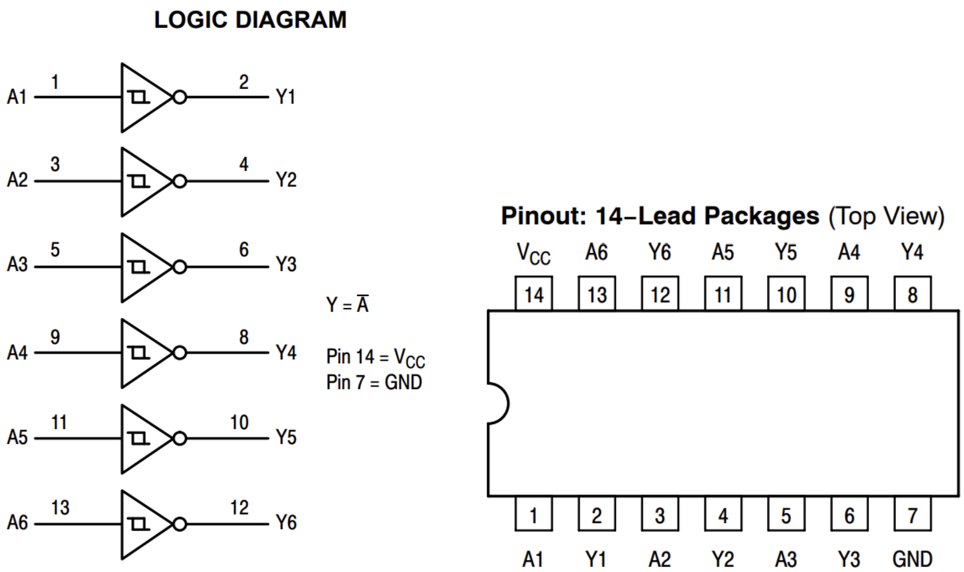

Figure 4: Logic Diagram of 74HC14A Schmidt-Trigger Inverter (Left) vs Pin Diagram of 74HC14A Schmidt-Trigger Inverter (Right)

The symbol in the middle of the Schmidt-Trigger Inverter represents the fact that the Schmidt-Trigger Inverter incorporates hysteresis. Hysteresis describes a characteristic in which the input voltage value needed for the device to make a transition from one state to another depends on the value of the state itself (i.e. the input voltage value to go from HIGH to LOW would be different than the input voltage needed to go from LOW to HIGH). A graph of the hysteresis effect is shown below:

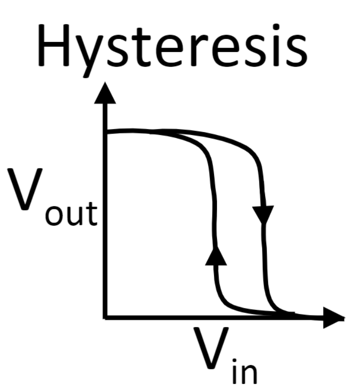

Figure 5: Diagram used to visualize the process of hysteresis

Below is the circuit schematic for our set-up. We have a constant $3.3\ V$ input (as shown in the upper red wire in the diagram below). We also have a sawtooth - or triangle - input with an amplitude of $3.3\ V$ and an oscillation of $1\ \mathrm{kHz}$ (represented by the yellow wire) and a $12\ k\Omega$ resistor (the resistor was used to stabilize the output). The orange wires are there to measure the value of the output over time, while the blue wires are used to measure the value of the input over time.

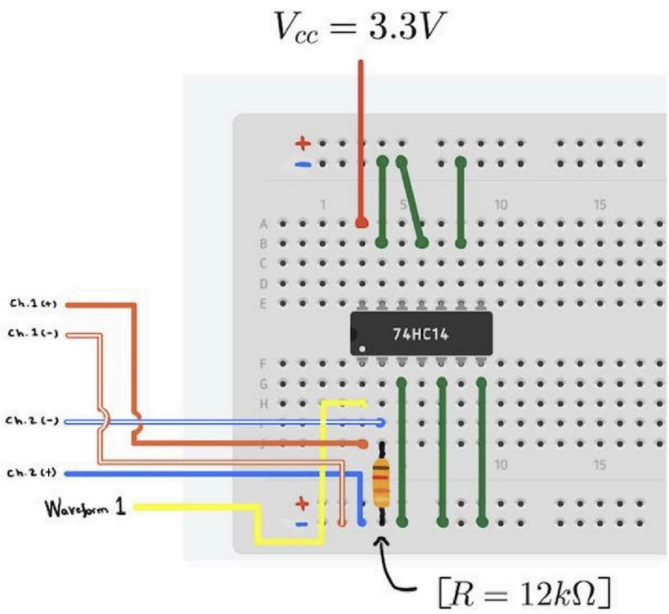

Figure 6: Circuit Schematic of our Set-up testing out our one of the inverters in our 74HC14A Schmidt-Trigger Inverter.

Below is the actual circuit for the Schmidt-Trigger inverter:

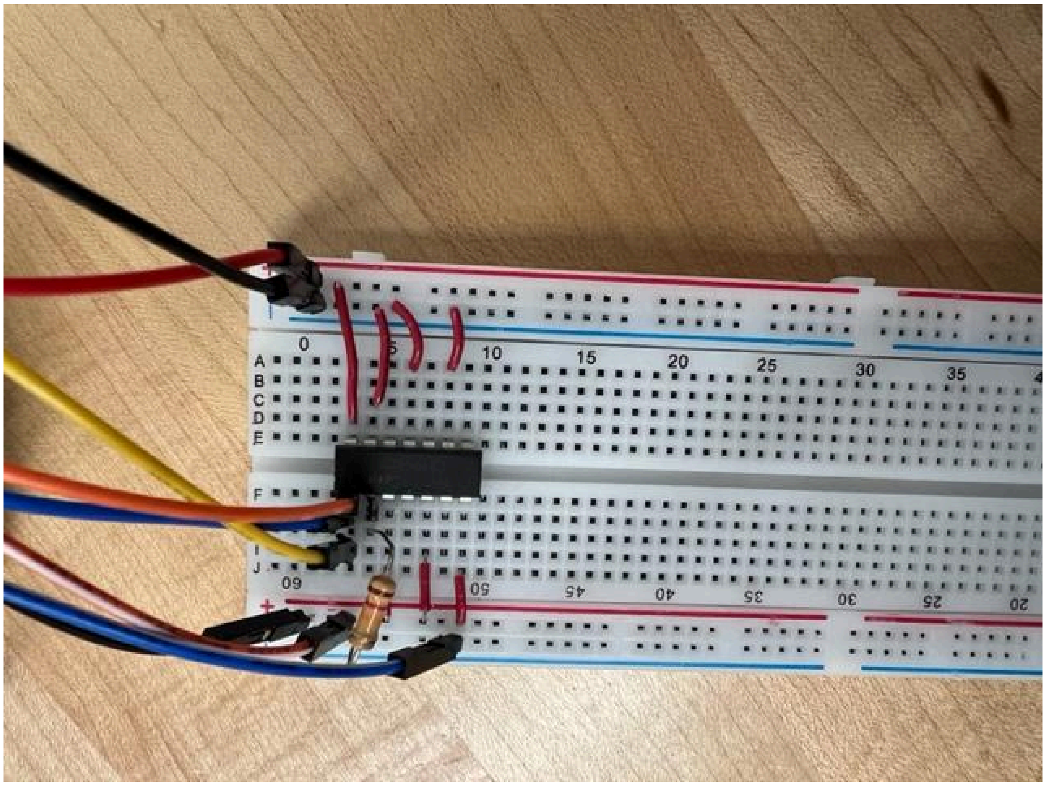

Figure 7: Circuit Set-up for experimental test of the 74HC14A Schmidt-Trigger Inverter.

If we measure the output of our circuit, we get the following output below. The yellow graph represents the voltage output and the blue graph represents the sawtooth input. In order to function properly, all of the inputs for the the Schmidt-Trigger inverters that were not used are connected to ground.

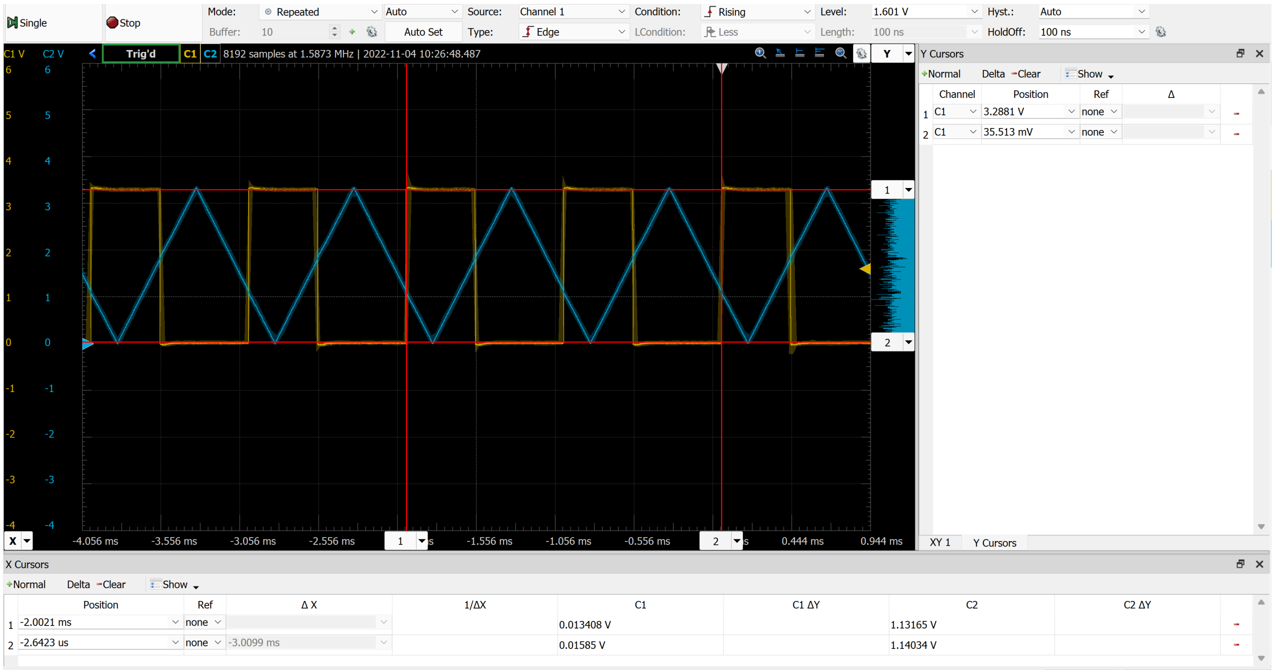

Figure 8: Output for Schmidt-Trigger Inverters.

If we create a separate graph on the right for measuring the voltage output vs the voltage input, we get the following output:

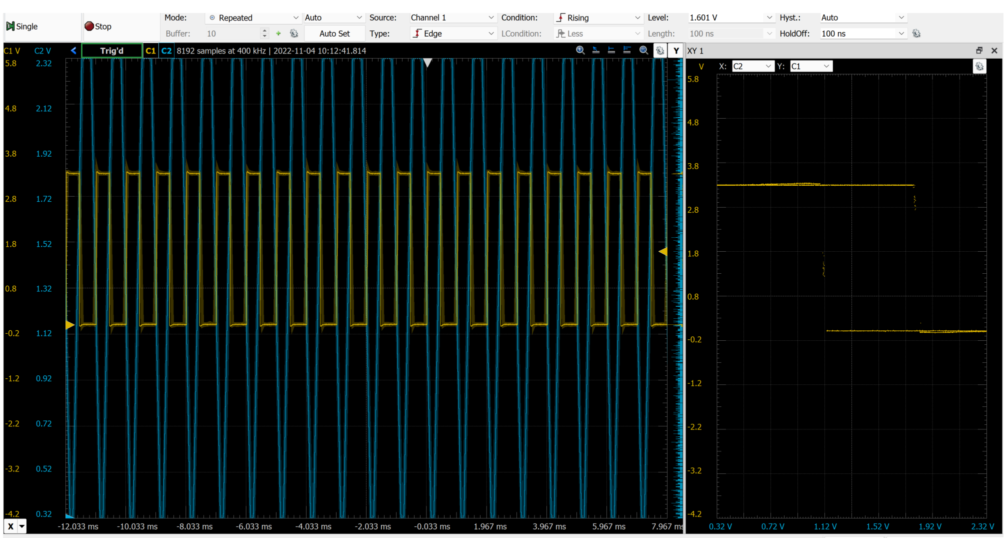

Figure 9: Voltage Output vs Voltage Input for the Schmidt-Trigger Inverter (shown in the right part of the image above).

If we indicate the directions of each of the jumps in the graph (which is consistent with Fig. 5), we get the following image below:

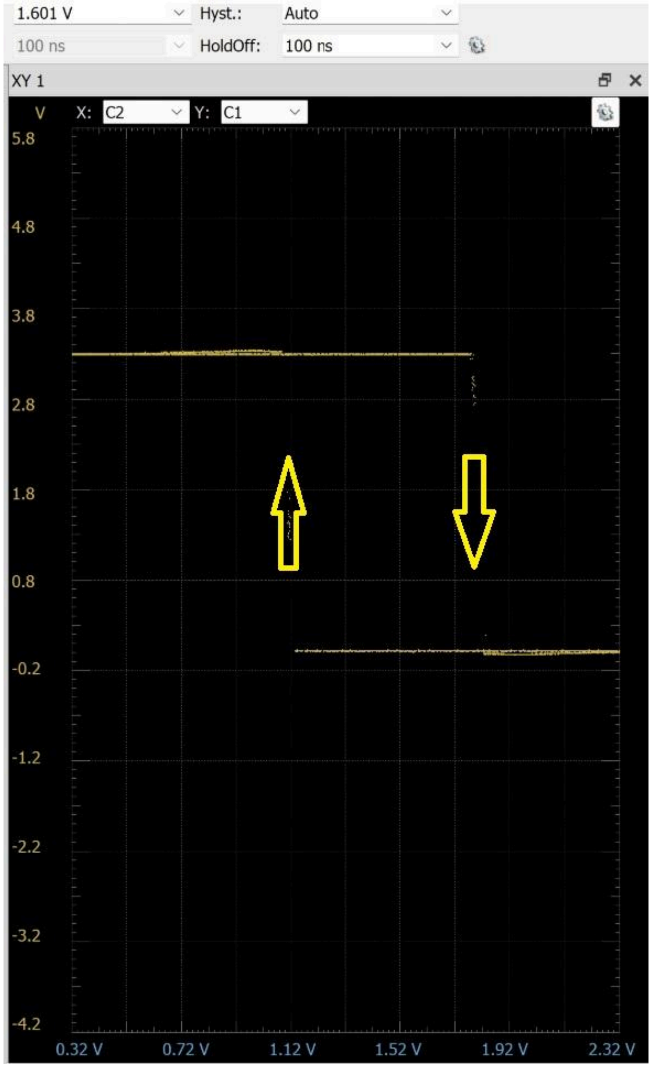

Figure 10: Plot experimentally showing the process of hysteresis

If we actually measure the quantitative values of the input and output voltages, we find that the lower value of $V_{\text{in}} = 1.0703\ V$ and the higher value of $V_{\text{in}} = 1.78714\ V$. The theoretical maximum value of V_{out} should be $3.3\ V$. Our actual maximum value is measured to be $3.32137\ V$. This discrepancy is likely due to measurement errors due to the fact that the AD2 scope has to measure a sudden jump in the voltage.

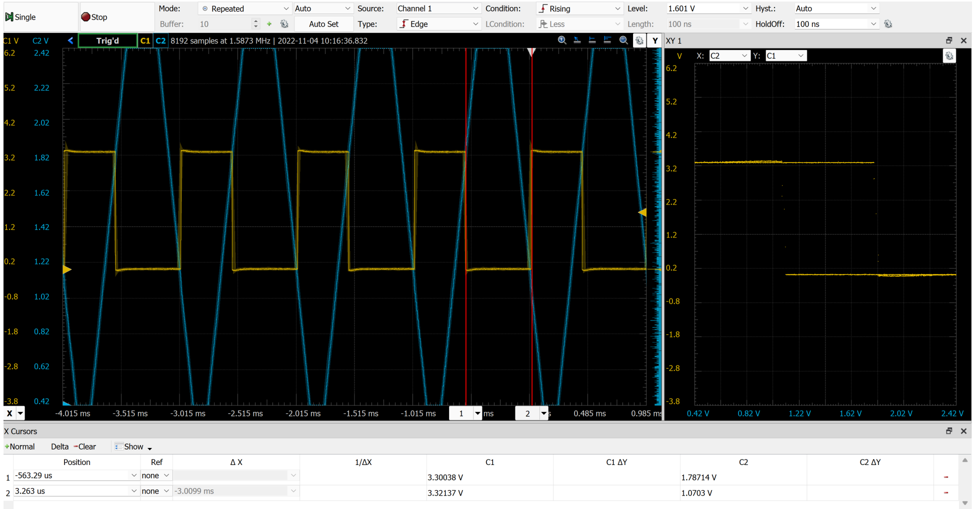

Figure 11: Plot showing quantitative values for measuring the input voltages needed for the hysteresis process.

4.2 *LATCH* and *RESET* generator

Below is the diagram for the LATCH and RESET generator. For this section of the lab, it will be necessary to use the 74HC14A logic device.

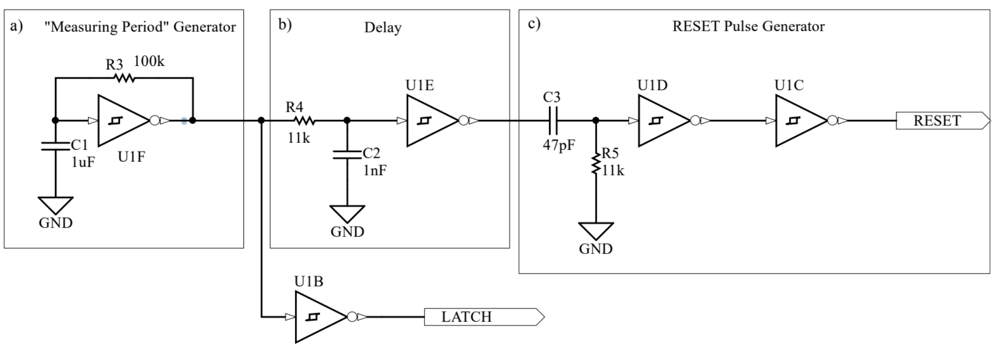

Figure 12: Diagram of LATCH and RESET generator.

Period Generator and LATCH output:

The inverter in section (a) below is a Schmidt-Trigger Inverter. The inverter by itself obeys the process of hysteresis as outlined in Section 4.1 above. It works by having the input alternate between the input due to the path of the 100 kΩ resistor and the $1\ \mu F$ capacitor. The capacitor becomes charged as some of the current from the path with the 100 kΩ resistor goes into the inverter and some goes to the capacitor. The capacitor then discharges when the input from the path from the 100 kΩ resistor is low.

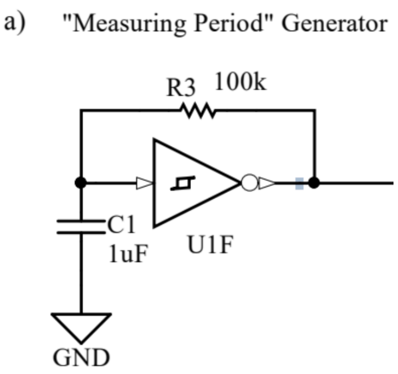

Figure 13: Circuit Schematic of "Measuring Period" Generator.

If we focus on just part (a) of the section above (called the "Measuring Period" Generator), then the circuit schematic for that subsection is shown below. The only input was $V_{cc} = 3.3\ V$ input. Notice how we measure our output across the inverter itself.

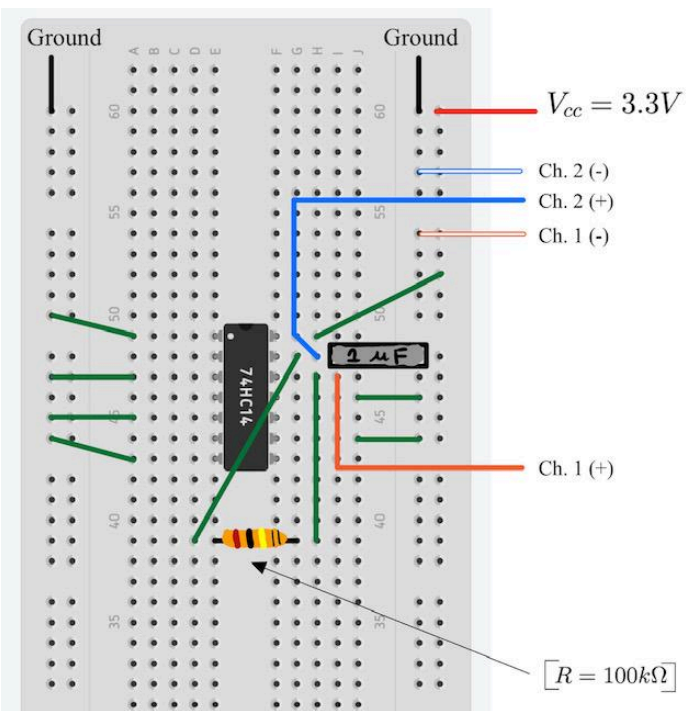

Figure 14: Circuit Schematic for "Measuring Period" Generator

The actual circuit is for the "Measuring Period" Generator is shown below. Note that the original picture did not have the grounding wires plugged in, so they were digitally added. The corresponding results are for when the grounding wire was placed.

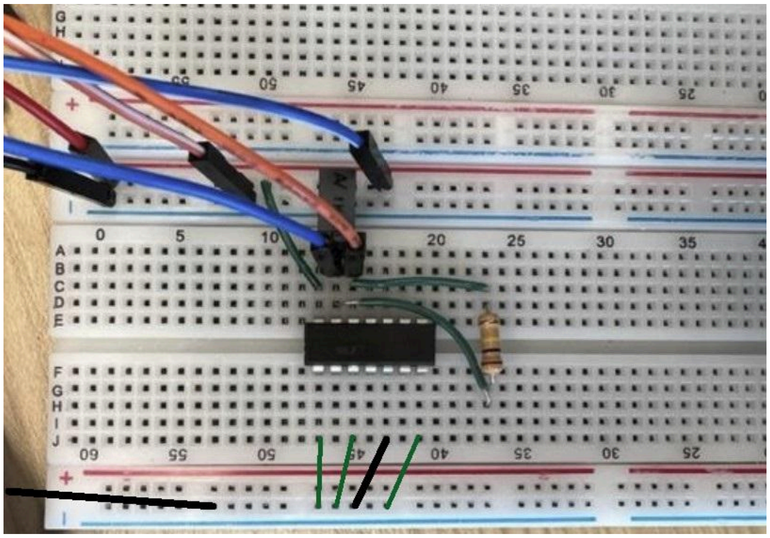

Figure 15: Circuit Set-up for "Measuring Period" Generator

If we measure the output (in yellow) vs our input (in blue), we find that our output looks like a constant voltage.

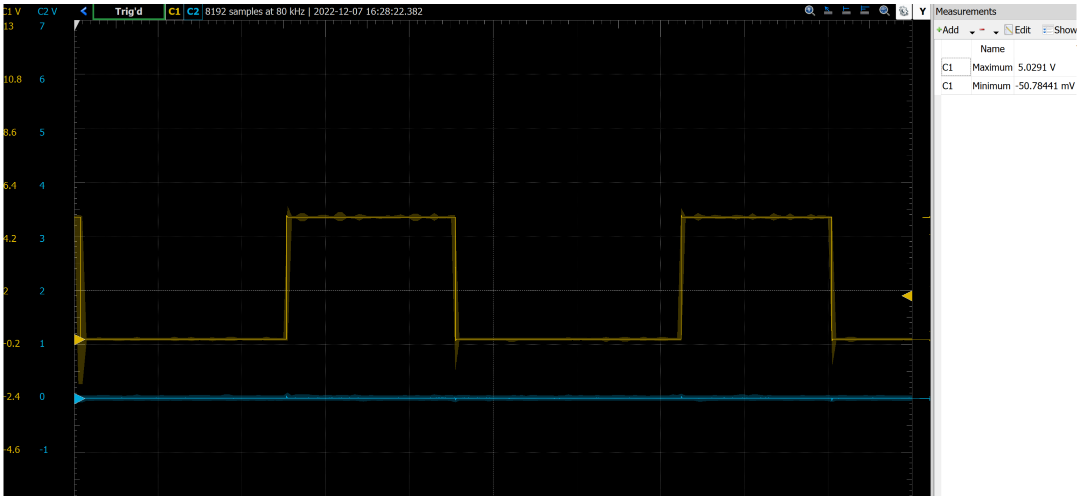

Figure 16: Voltage output for the "Measuring Period" Generator

Lastly, the LATCH output is simply the inverted version of the square wave produced by our "Measuring Period" Generator. The circuit diagram showing the LATCH output and its relation to the "Measuring Period" Generator is shown below:

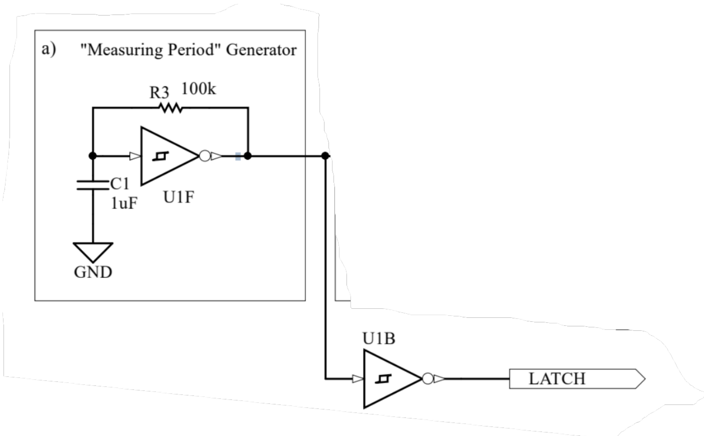

Figure 17: Circuit Diagram with the "Measuring Period" Generator with the LATCH output

If we were to measure the output of the LATCH output (this time with $V_{cc} = 5\ V$), we get the following output below:

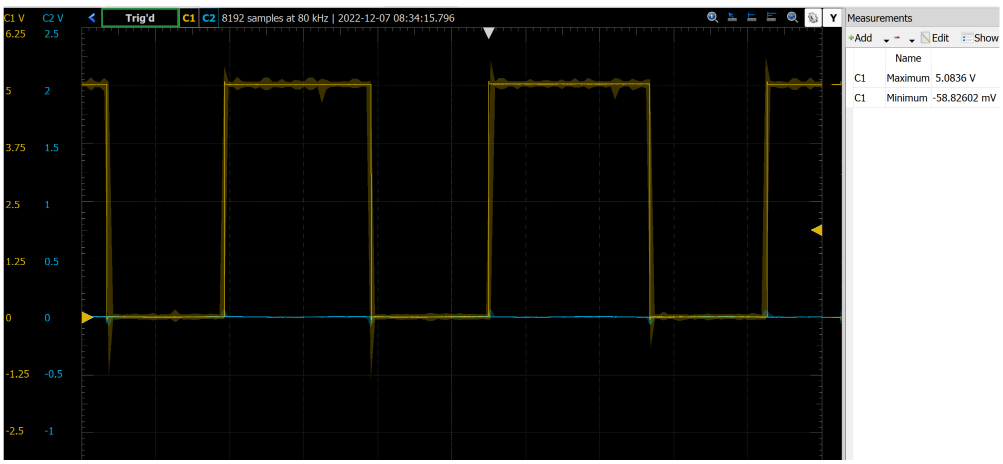

Figure 18: LATCH output

Delay Section:

The circuit diagram for the delay section from part (b) of Fig. 12 is shown below. The delay section produces a delay in the circuit. The reason a delay is introduced is because capacitors oppose spontaneous changes in voltages. Initially, the capacitor is at a voltage of 0 V, and will gain potential as current flows to the capacitor, as it gradually gains potential, so too will the potential applied at the input of the inverter. Once the potential at the inverter is high enough (the operating range is 2 V to 6 V, as per the datasheet), the inverter will activate and produce a square wave.

b) Delay

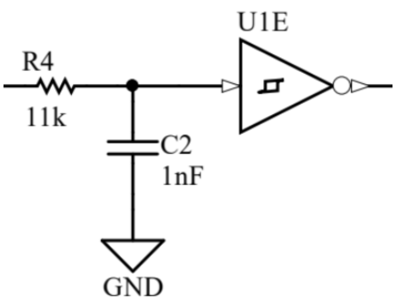

Figure 19: Circuit Schematic of Delay section.

The net part of section 4.2 is constructing section (b) (or equivalently the Delay section of the circuit). The circuit schematic for the construction of the delay circuit is shown below. The only input was $V_{cc} = 3.3\ V$ input. We are measuring the output across the inverter (shown as U1E in the figure above).

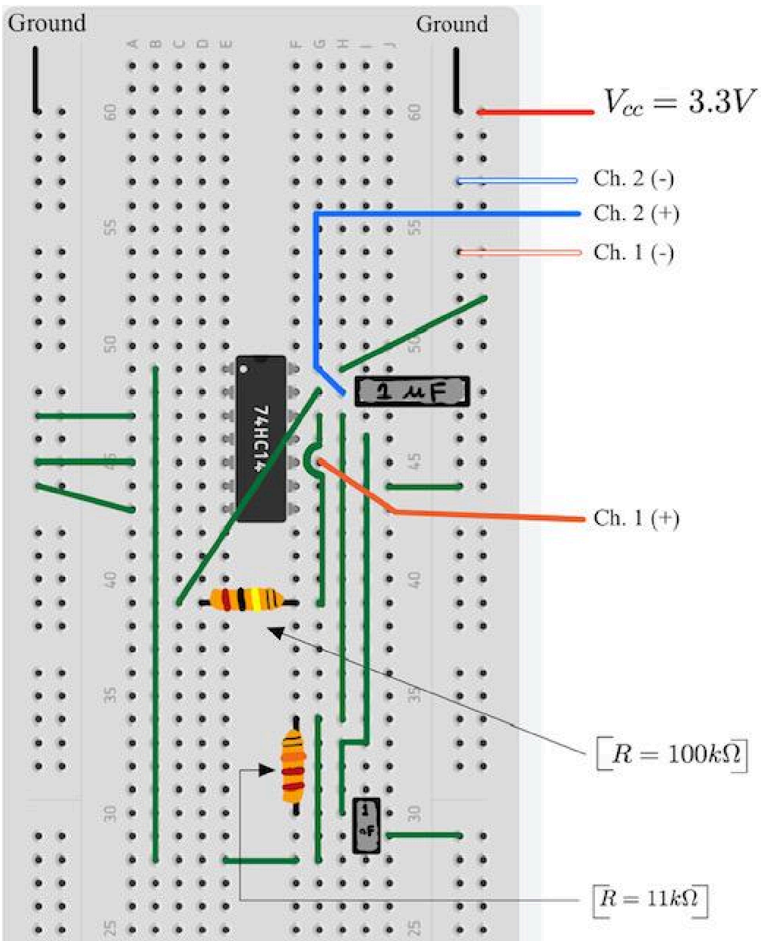

Figure 20: Circuit schematic for the combined "Measuring Period" Generator and Delay section

The actual construction of the combined "Measuring Period" Generator and Delay section is shown below:

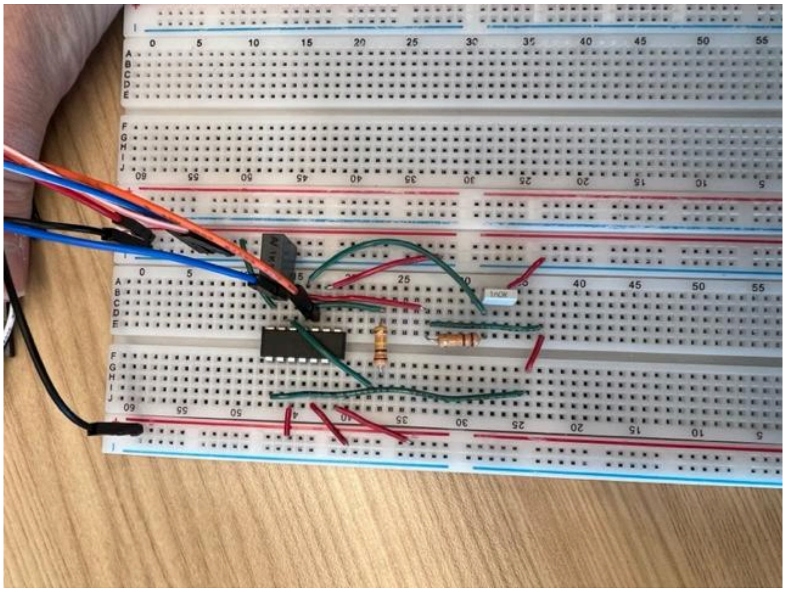

Figure 21: Construction of the combined "Measuring Period" Generator and Delay section

If we measure the output voltage (yellow) vs the input voltage (blue) for our combined "Measuring Period" and Delay section, we get the following graph below:

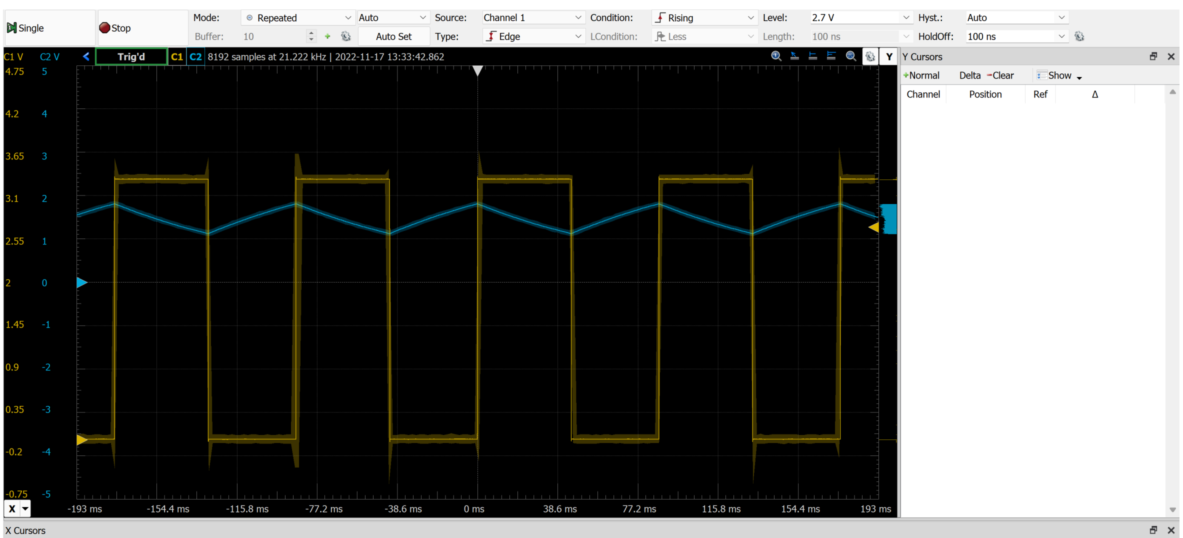

Figure 22: Graph of voltage output vs voltage input for our combined "Measuring Period" and Delay section

Doing some measurements, we find that the output voltage oscillates between 3.3117 V and 4.6408 mV with a period of 87.419 ms. The input voltage oscillates between 1.8119 V and 1.1098 V with the same period as the output voltage:

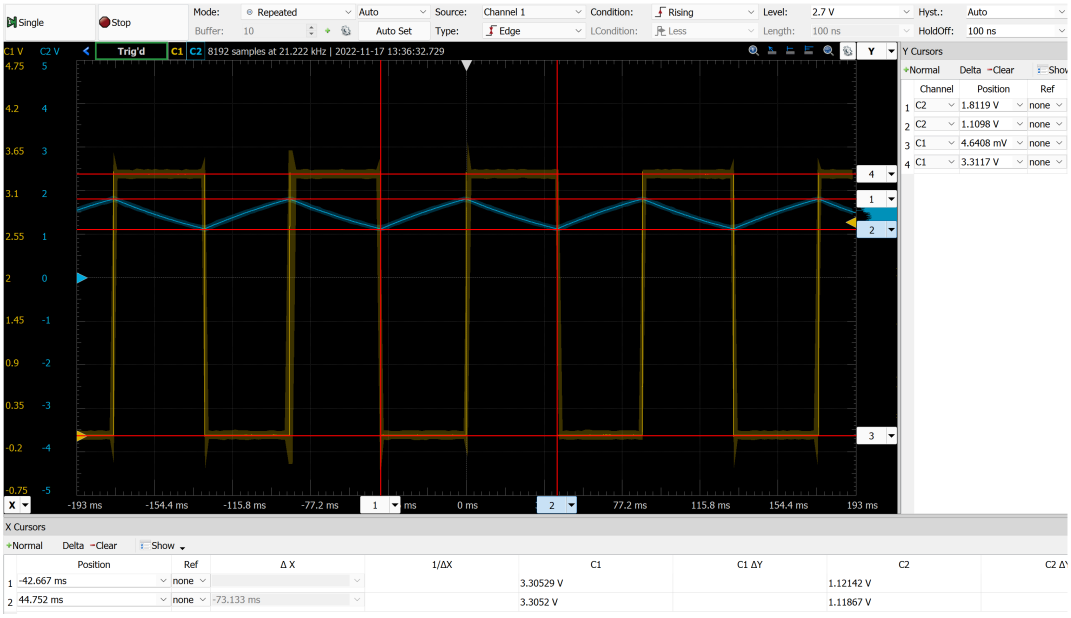

Figure 23: Measuring voltage output vs voltage input for combined combined "Measuring Period" and Delay section

If we zoom in on our input, we can detect a slight delay in our graph. This is due to the combined effect of the capacitor and the resistor. Because we have a capacitor and a resistor, we find that the decay should be related to a time-constant, $\tau = \mathrm{RC} = (11k\Omega)(1\mathrm{nF}) = 1.1 * 10^{-5}\, s = 0.011\ \mathrm{ms}$. If we look at the two numbers below, we find that the edge of the graph has a sudden drop and this drop occurs within a (very rough approximation) scale of 0.01 ms, as shown below:

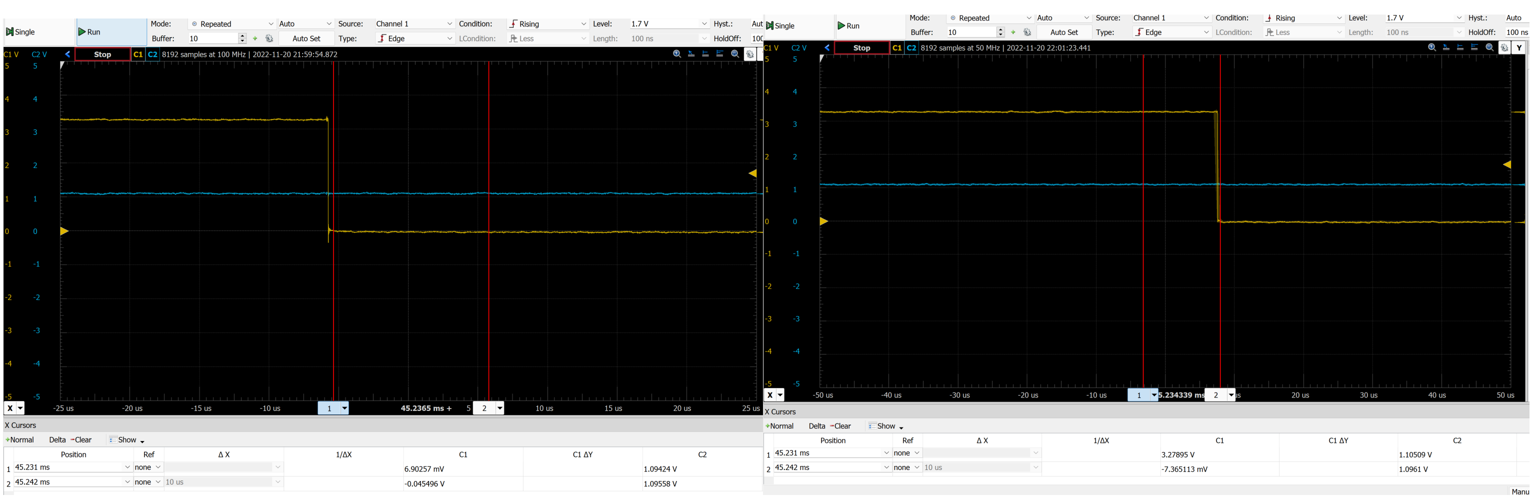

Figure 24: Measuring voltage delay in the circuit "Measuring Period" and Delay section

The delay is necessary for the operation of the circuit because the delay allows the D-latch to store the counter output before the RESET pulse arrives, all using the LATCH output.

Reset Generator:

The RESET generator generates a brief pulse (called the RESET pulse) which will eventually be used to reset the counter back to zero. The method by which this device works is, much like the Delay section, largely due to the presence of the capacitor. Because of the small value of the time constant of the combined capacitor resistor combination ($\tau = \mathrm{RC} = 11 * 10^3\,\Omega * 47 * 10^{-12} = 5.17 * 10^{-7}\,s$), the capacitor will charge and discharge very quickly. This means that for a very short amount of time, the voltage at the input of the first inverter (labeled U1D) below will be high enough for the inverter to be activated. This will generate a short pulse which will be inverted once more by the inverter labeled U1C below in order to produce a RESET pulse of the correct polarity.

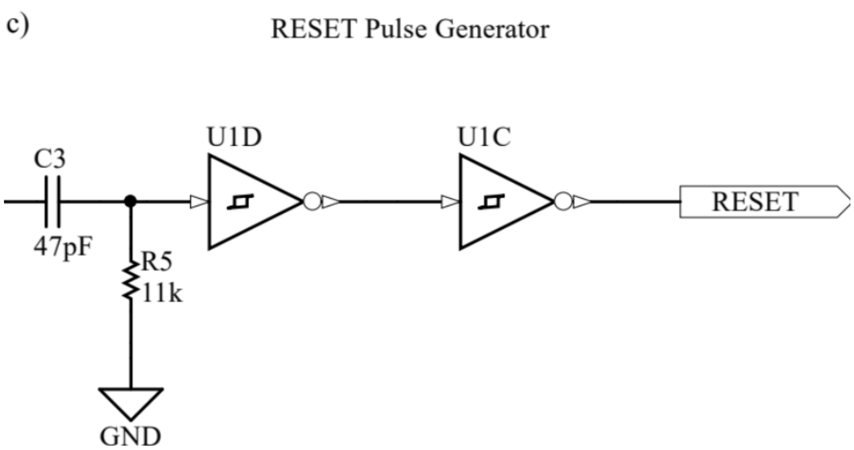

Figure 25: Circuit Schematic of the RESET Pulse Generator.

Lastly, if we do the last part of the circuit (i.e. the RESET Pulse Generator corresponding to part (c)), we get the following circuit schematic below (NOTE: For clarity the output corresponding to LATCH was moved from pin #2 to pin #6) of the 74HC14A Schmidt-Trigger. The only input was $V_{cc} = 3.3\,V$. The voltage is right before across the $47\,\mathrm{pF}$ capacitor with respect to the ground.

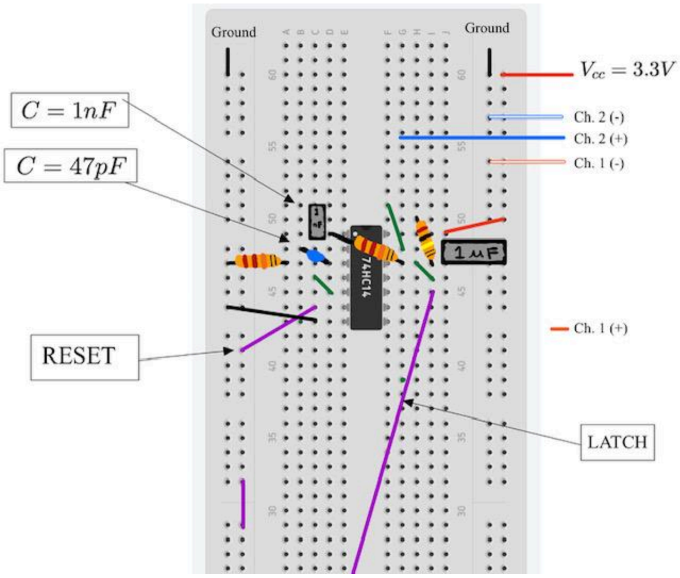

Figure 26: Circuit Schematic for combined "Measuring Period" Generator - Delay - RESET Pulse Generator

Our actual circuit looks like:

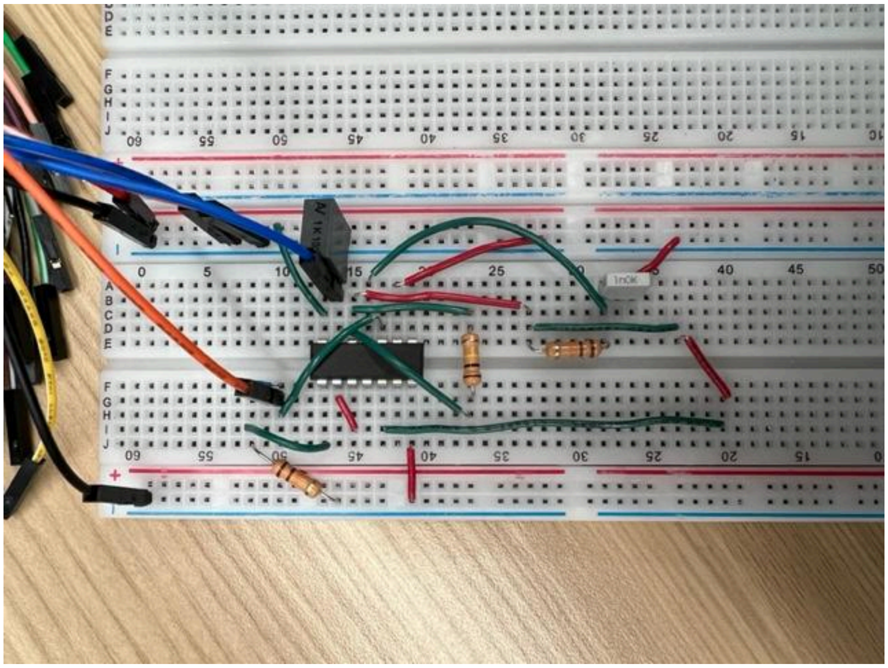

Figure 27: Circuit Setup for combined "Measuring Period" Generator - Delay - RESET Pulse Generator

This is what our output looks like. The output is similar to that of the delay sub-section above. The yellow graph represents the output voltage and the blue graph represents the input voltage.

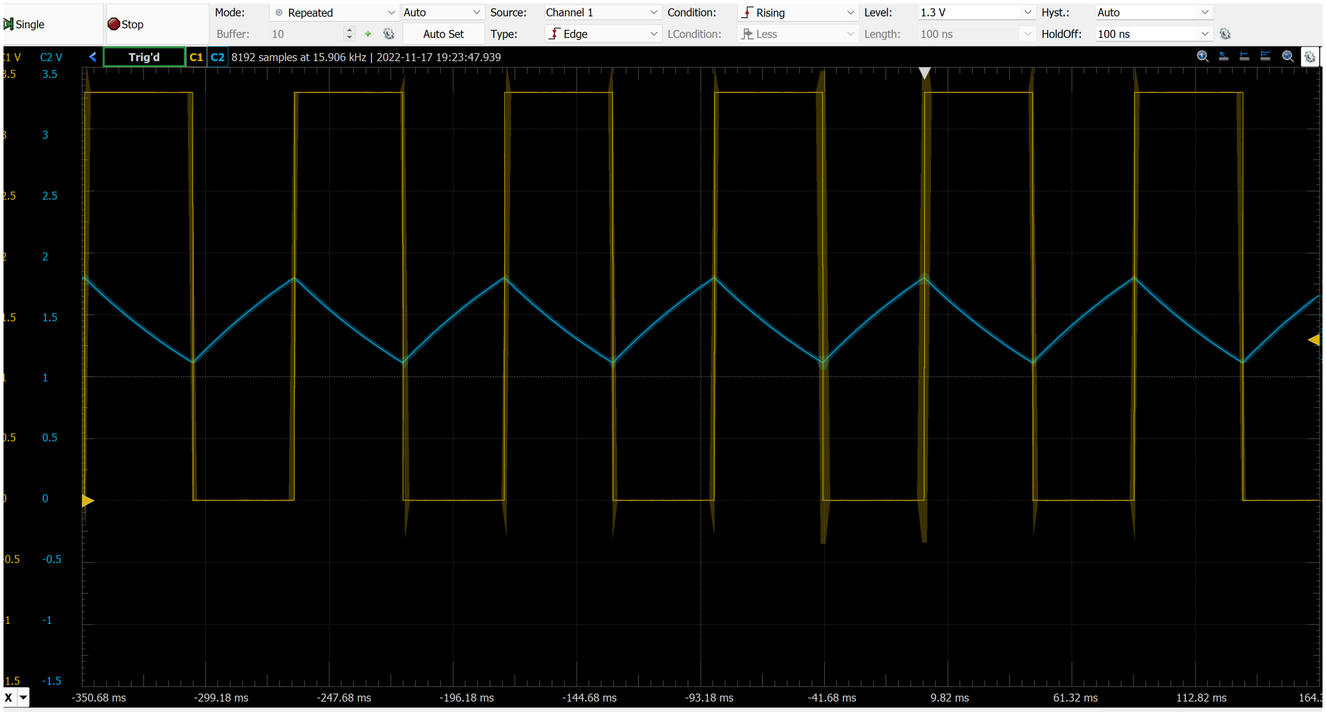

Figure 28: Voltage output vs voltage input for combined "Measuring Period" Generator - Delay - RESET Pulse Generator

If we measure the values, we get the following. The maximum and minimum voltages of the output are 3.3 V and 0 V respectively. The maximum and minimum voltages of the input are 1.797 V and 1.115 V respectively. The period of both the input and output signals is 87.67 ms, a very similar number to the Delay section above.

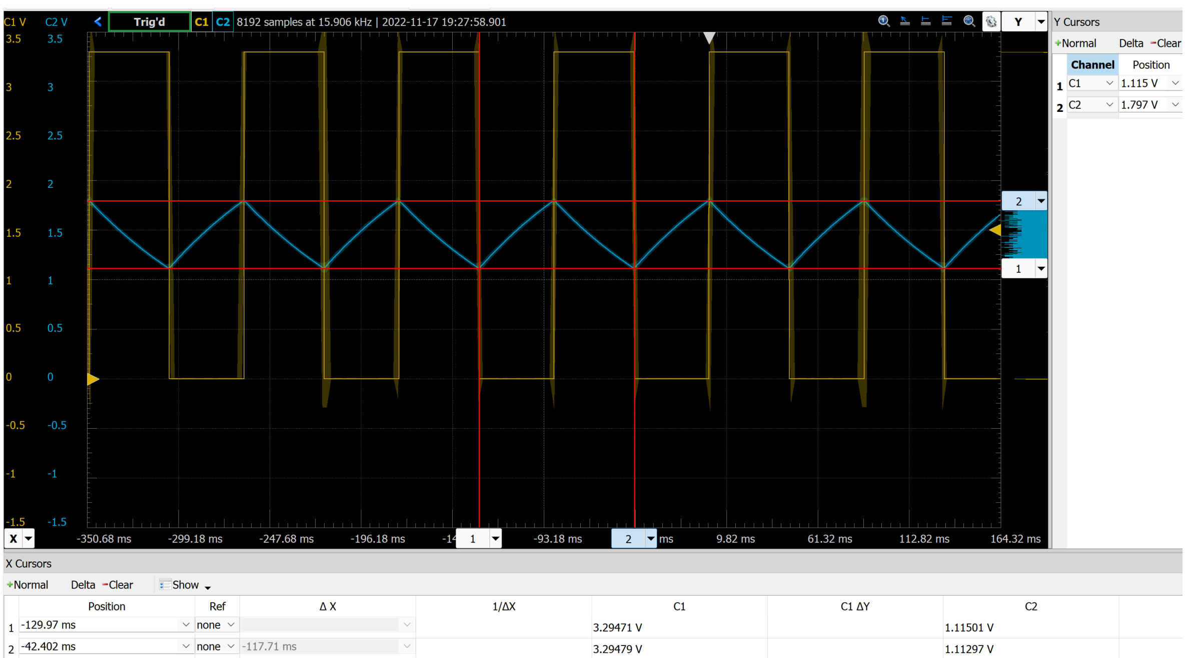

Figure 29: Measuring the numerical voltage values for combined "Measuring Period" Generator - Delay - RESET Pulse Generator

To detect the actual RESET pulse itself, we can measure the voltage output of the inverter that corresponds to the RESET pulse and get the following output below. We find that, despite the occasional irregular period of the RESET pulses, the period of the RESET pulses is $-190.75\text{ ms} - (-231.22\text{ ms}) = 40.47\text{ ms} \pm 0.01\text{ ms}$. The period of the RESET pulse is the same as the LATCH pulse. Therefore, the frequency of both the LATCH and RESET pulses is $\dfrac{1}{40.47\text{ms}} = 24.71\text{ Hz}$.

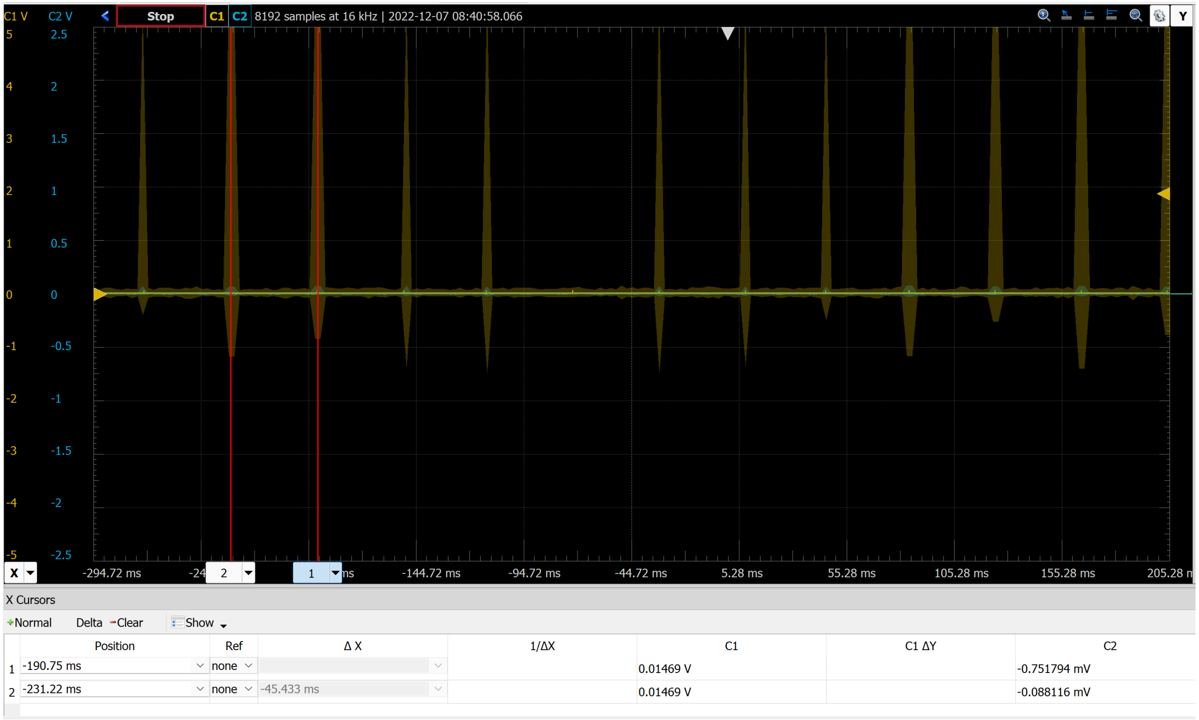

Figure 30: Graph showing RESET pulse.

4.3 Counter, D-latch, and DAC

The circuit schematic for the counter, D-latch, DAC, and buffer combined is shown below:

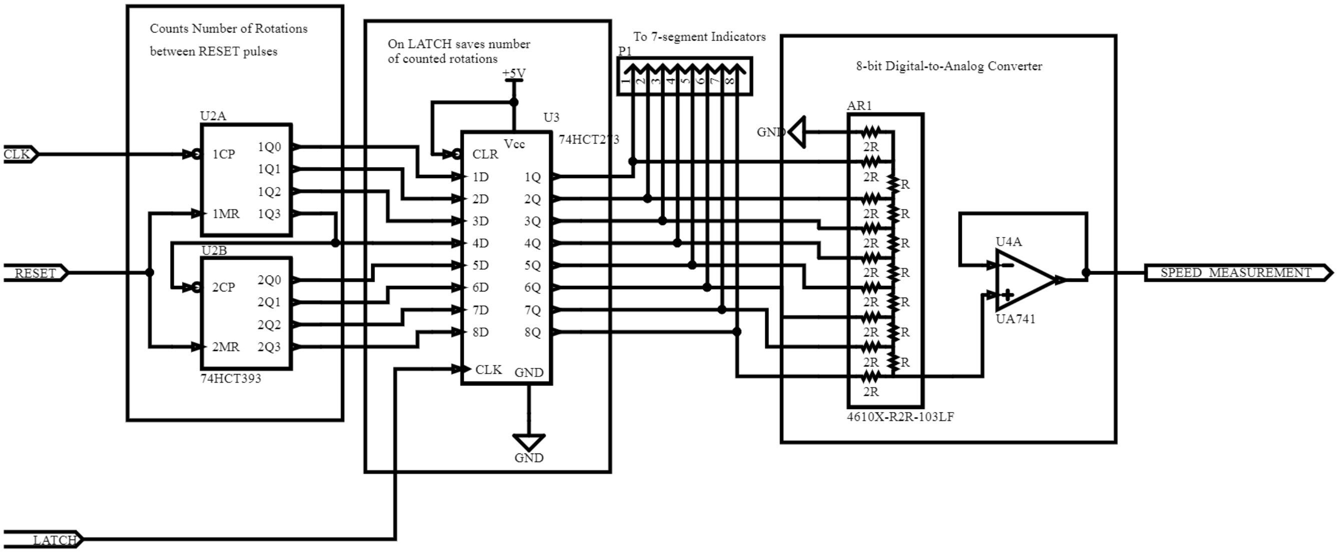

Figure 31: Circuit schematic for counter, D-latch, DAC, and buffer combined.

The functional diagram of the 74HCT393 Dual 4-bit binary ripple counter and its pin configuration are shown below:

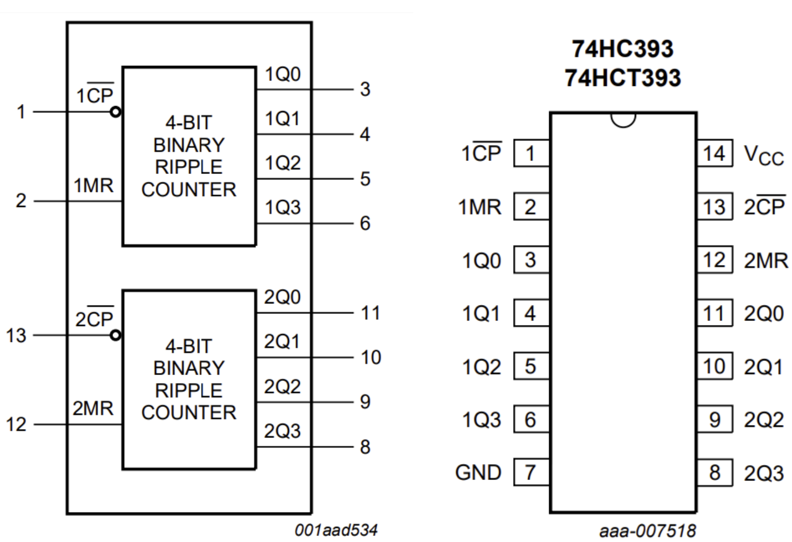

Figure 32: The functional and pin diagram of the 74HC393 device

The functional diagram of the 74HC273 Dual 4-bit binary ripple counter and its pin configuration are shown below:

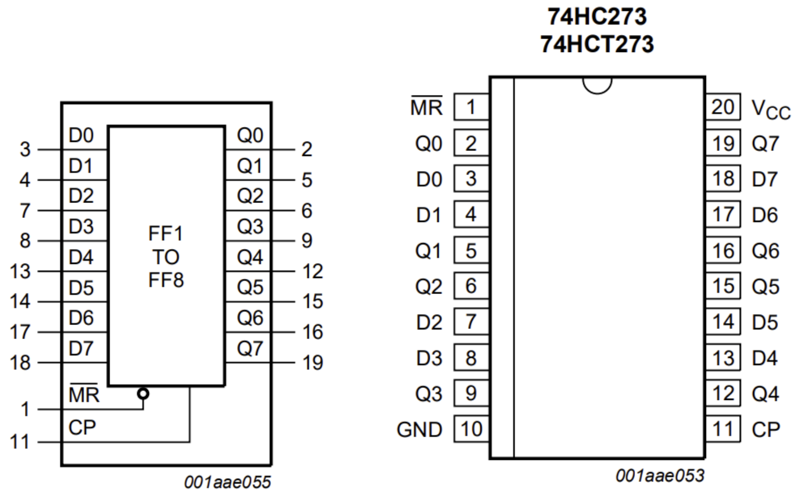

Figure 33: The functional and pin diagram of the 74HC273 device

Counter:

The circuit schematic for the counter alone is shown below:

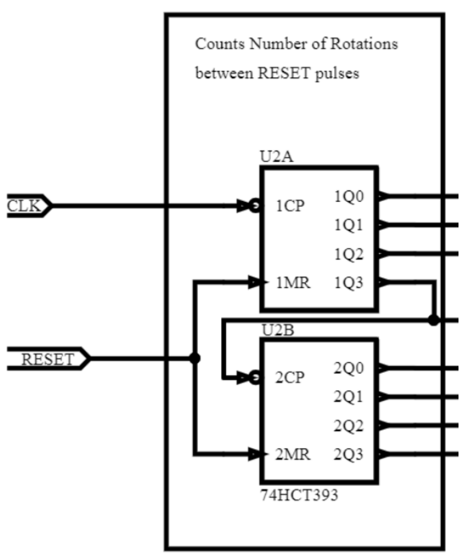

Figure 34: Circuit Schematic of counter by itself.

The method by which the counter works is that we have a CLK impulse which counts (in hexadecimal) at the frequency of the CLK output. The counter resets to 0, each time the RESET pulse is detected. For example: If the CLK pulse is at 123.5 Hz, and the RESET Pulse is at 24.7 Hz, we find that the counter will display 123.5/24.7 = 5. Once our circuit is finished, the CLK pulse will be dependent on the speed of the motor itself, as the CLK pulse will be proportional to the RPM of the disc.

The first step is to test out to see if the 74HC273 device works properly, we can test this by checking the counter. The circuit Schematic to test the counter with the 74HC273 device is shown below: We apply a $V_{cc} = 3.3\ V$ input as well as a 1 Hz square waveform (indicated by the yellow wire) with an amplitude of 4 V as our CLK pulse.

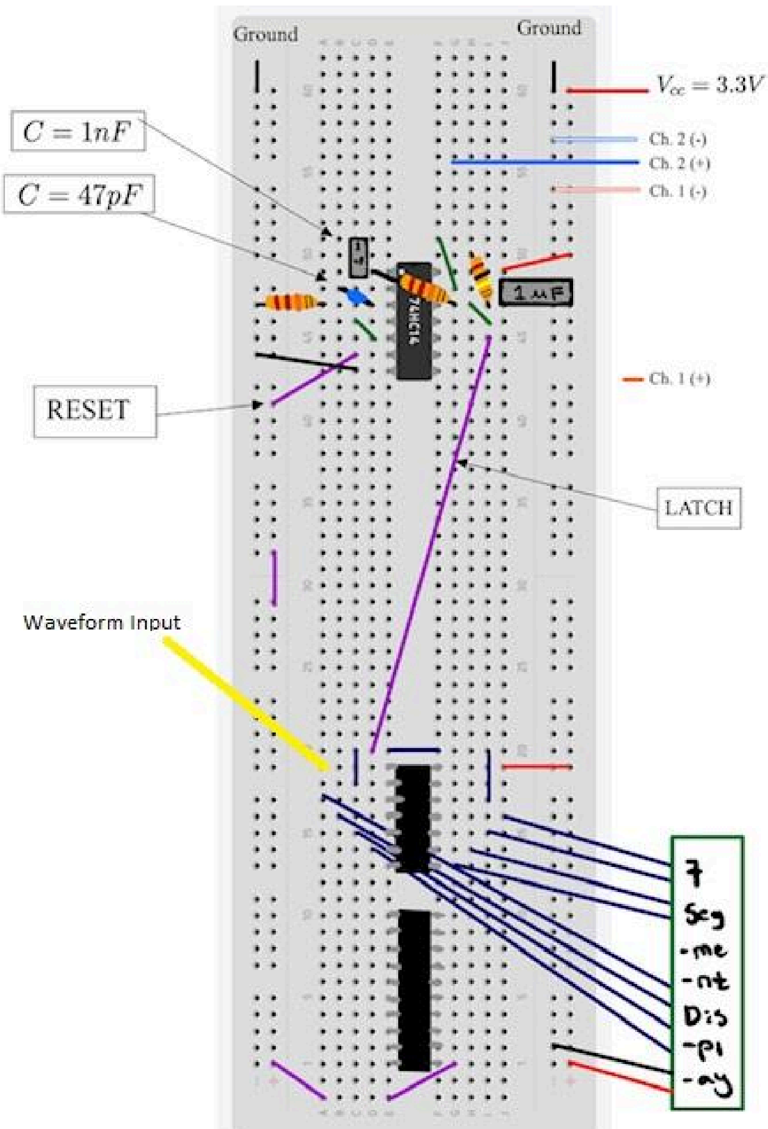

Figure 35: Circuit Schematic the for counter of section 4.3

If we actually build the circuit, we get the following image below:

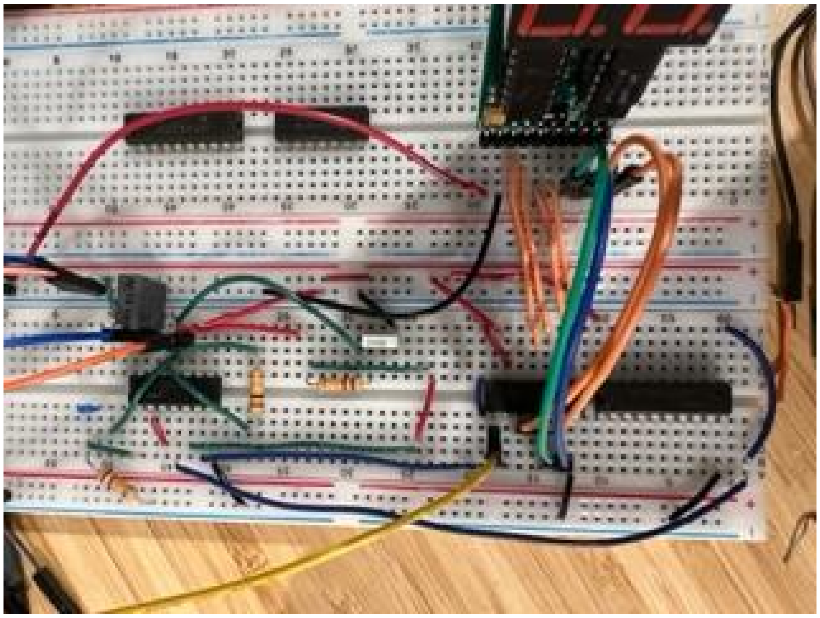

Figure 36: Images showing the actual circuit setup for the counter

We can test to see if the counter is working (by disabling the RESET function) to see if it is properly displaying a number as shown below:

Figure 37: Visual proof of the the counter working as intended

Counter + D-Latch:

Below is the circuit diagram for both the counter and the D-latch.

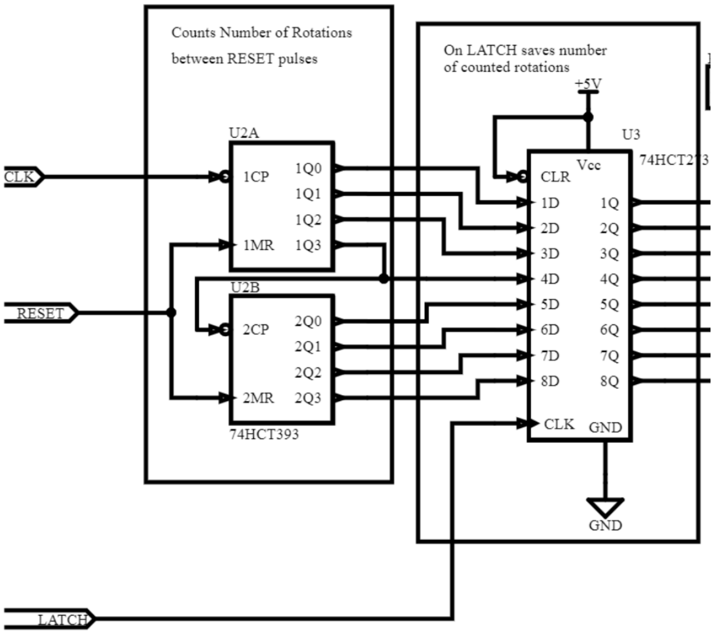

Figure 38: Circuit diagram of Counter and D-latch

The circuit schematic below is for the counter plus D-latch:

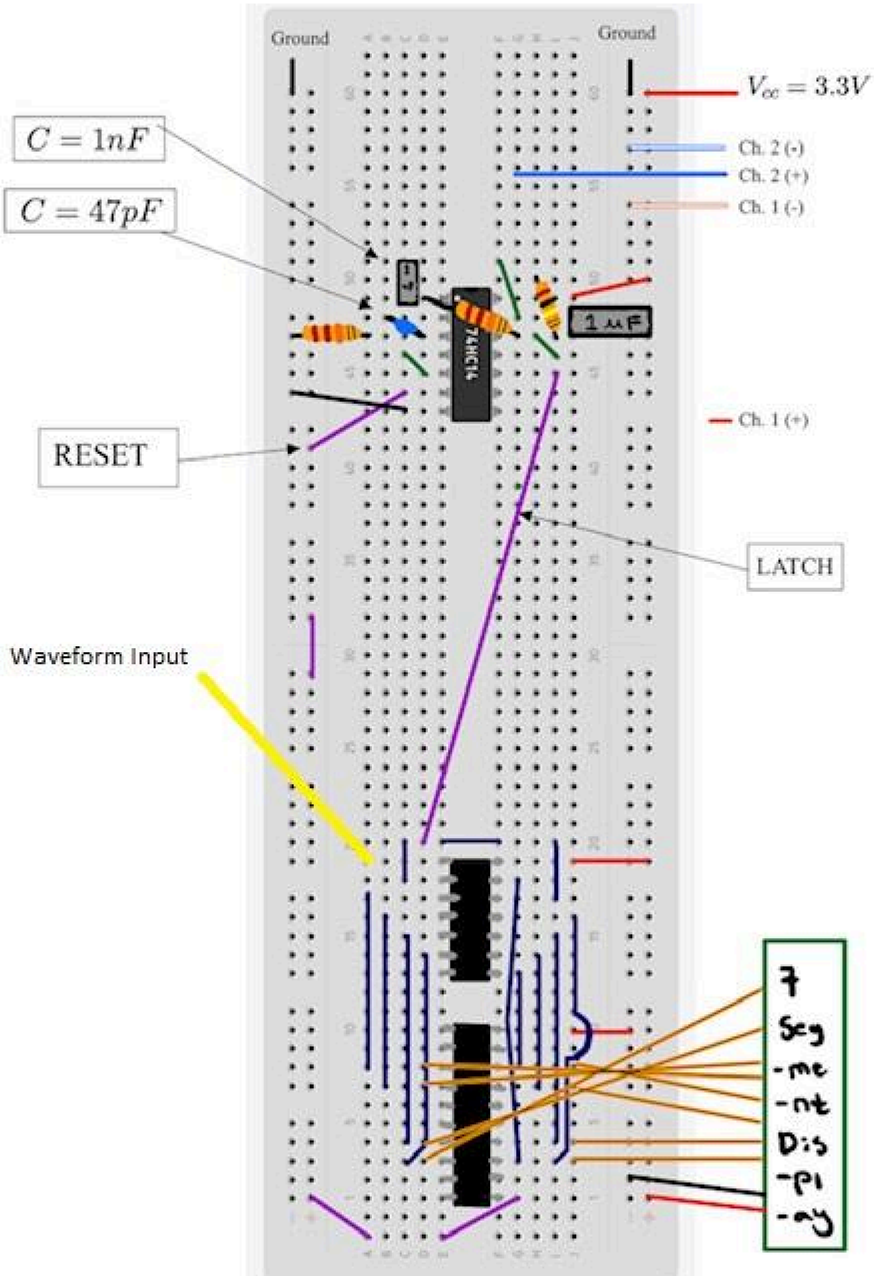

Figure 39: Circuit Set-up of the Counter and D-latch

As described earlier at the start of the "Counter" section of the lab report, the CLK pulse will be proportional to the number of rotations (a higher motor speed will correspond to a more rapid CLK pulse). The purpose of the D-latch is to store the output of the CLK pulse in order to properly display it on the counter.

We have two digits, and each digit is composed of four bits (The first digit is composed of the bits labeled 1Q0, 1Q1, 1Q2, 1Q3, while the second digit is composed of the bits labeled 2Q0, 2Q1, 2Q2, 2Q3 in the original diagram for the counter). Therefore, for each digit we have 2^4 possible values, and since we are dealing with binary logic, each digit represents a hexadecimal number from 0 to F (where F is the hexadecimal representation of 15) and since we have two digits, we have $2^4 * 2^4 = 256$ possible values. This means that the maximum number that we can count up to is 255 (0 to 255) as we have two 16 bit counters, and 16x16 = 256 different numbers. Once the counter reached the maximum value, it would then reset to 0 and then count back up again.

The following image below is our circuit with the Counter and the D-Latch:

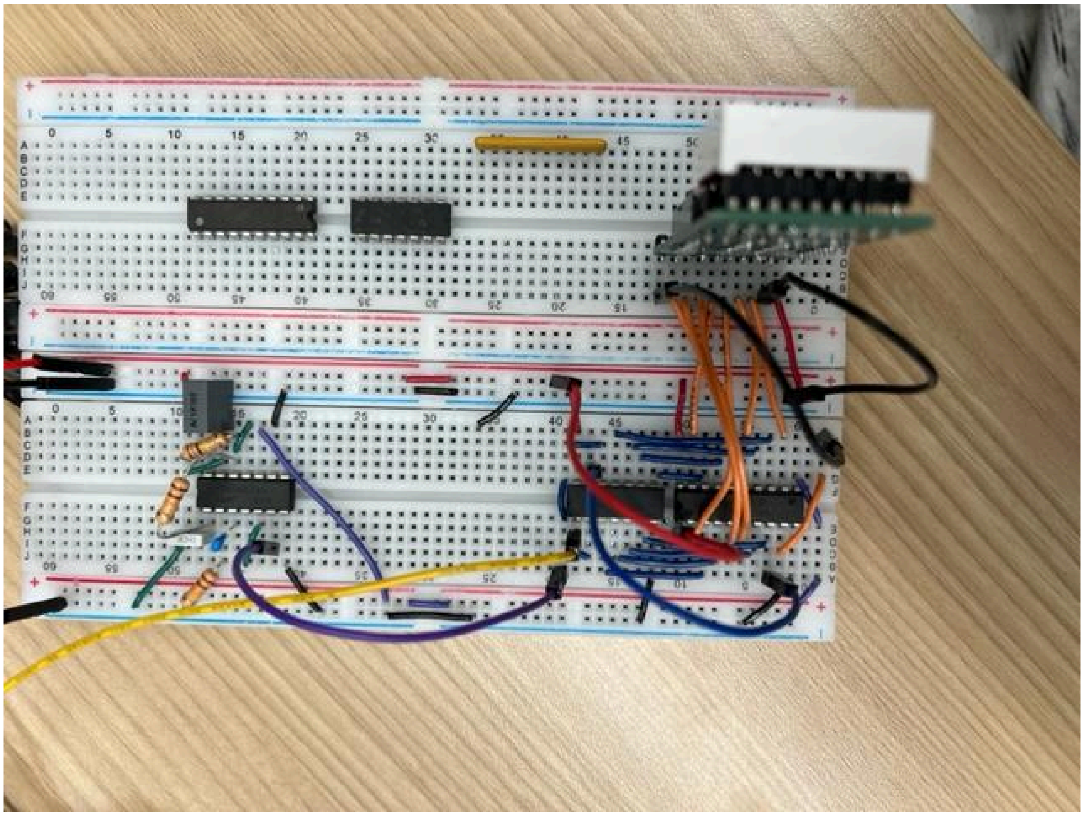

Figure 40: Circuit Setup with both counter and D-latch

If we attach the D-latch (with $V_{cc} = 5\ V$ and a square wave input, $2.5\ V$ amplitude with an offset of $2.5\ V$), we find that the counter counts up from hexadecimal as long as the square wave input and the voltage supplied are on. Below is an example number:

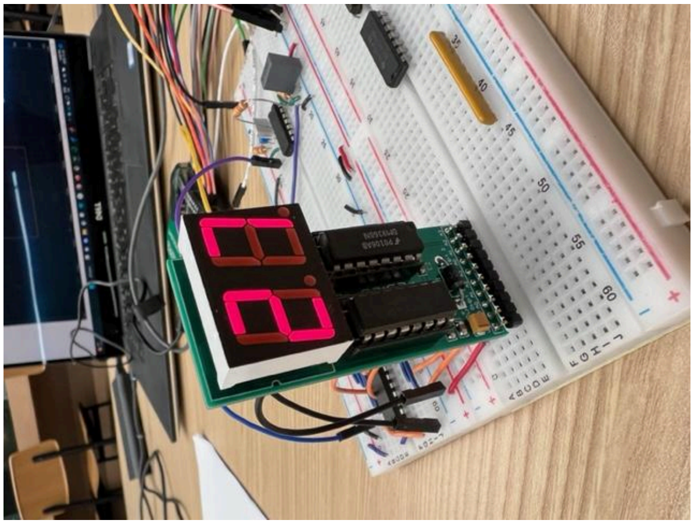

Figure 41: Number displayed indicating number of latches

Counter + D-Latch + DAC:

The circuit diagram containing the counter, d-latch, and the DAC is shown below:

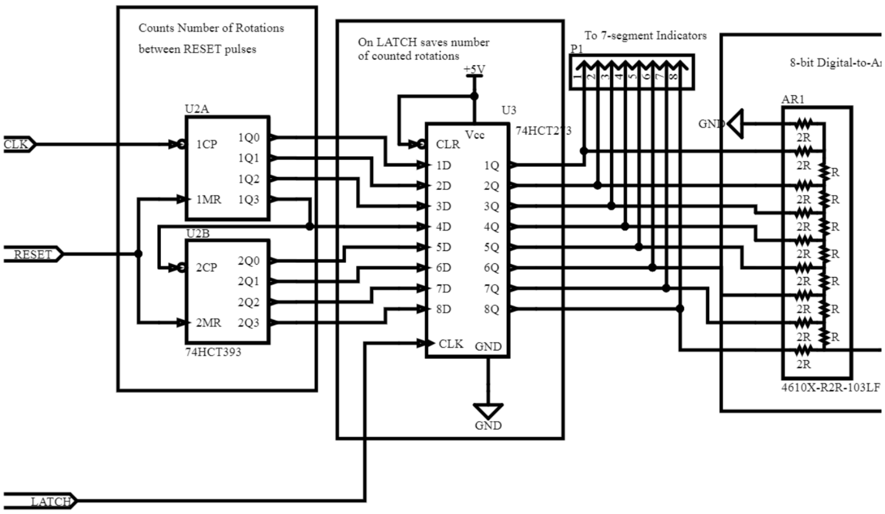

Figure 42: Circuit diagram containing the counter, d-latch, and the DAC.

The voltage output of the D-latch is a digital signal (i.e. a signal that is composed of values from a discrete set). However, for the remaining sections of the circuit, voltage outputs in the form of a digital signal will not be useful. Therefore, we need a DAC to convert the output signal from digital to analog.

The actual circuit for the buffer is shown below:

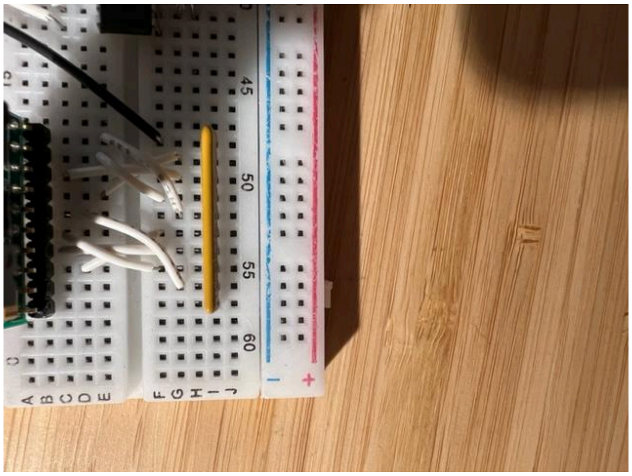

Figure 43: Circuit setup of the buffer

If we measure the output of the DAC without a buffer, we see a sawtooth wave that goes from 1 V to 5 V.

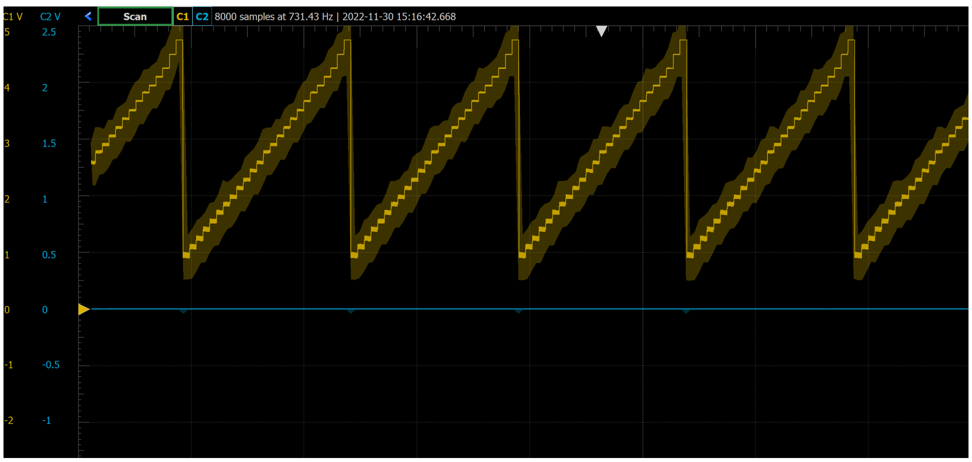

Figure 44: Output of the DAC

Counter + D-Latch + DAC + Buffer:

The circuit diagram containing the counter, d-latch, DAC, and the buffer is shown below:

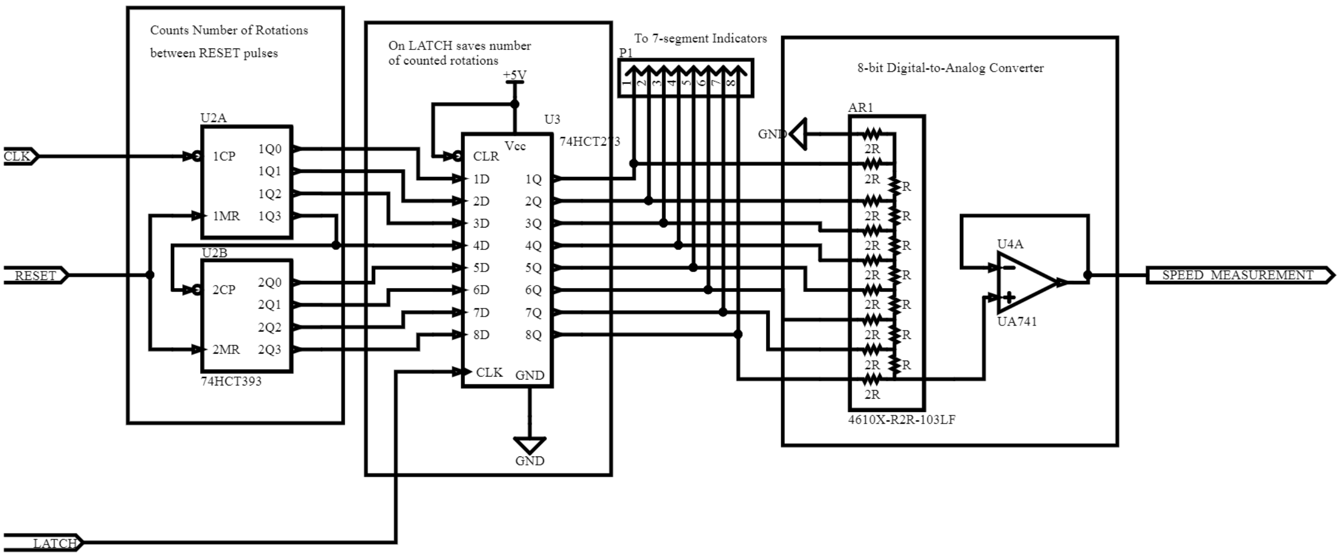

Figure 45: Circuit diagram containing the counter, d-latch, DAC, and the buffer

The circuit diagram (left) and the pin-diagram (right) for the UA741 opAmp is shown below. The UA741 OpAmp is used for the buffer and is also used twice more in the construction of the motor driver in section 4.4 of the lab report.

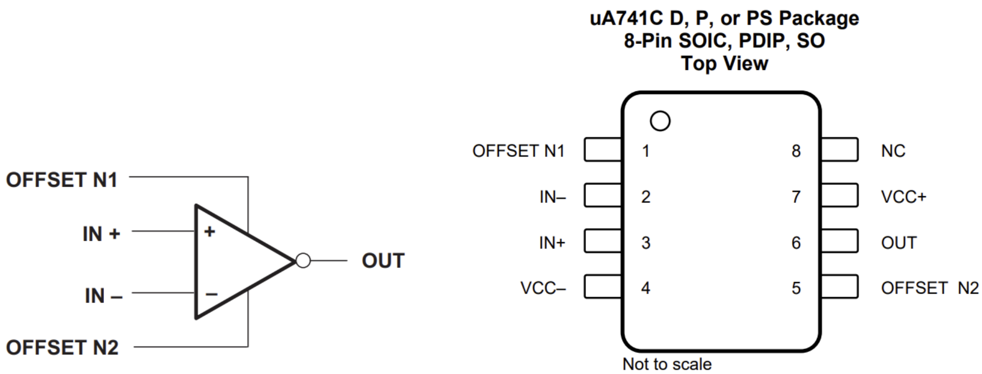

Figure 46: Circuit diagram (left) and the pin-diagram (right) for the UA741 OpAmp

The circuit setup of the buffer by itself is shown below:

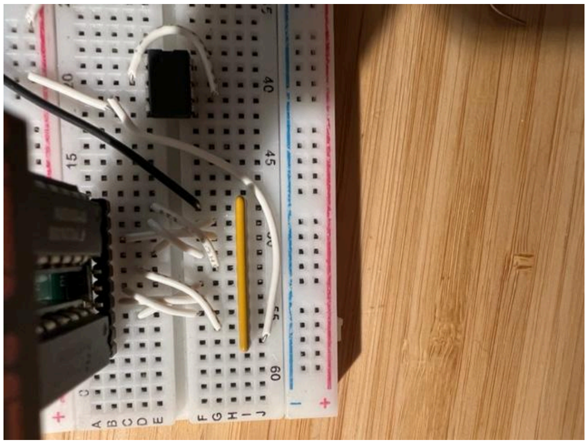

Figure 47: Circuit setup of the buffer

The buffer works by changing the amplitude of the sawtooth wave. The amplitude is changed for operation in the last part of the circuit (i.e the motor sensor and the motor driver).

If we measure the output with a buffer, we see that the output is a sawtooth wave:

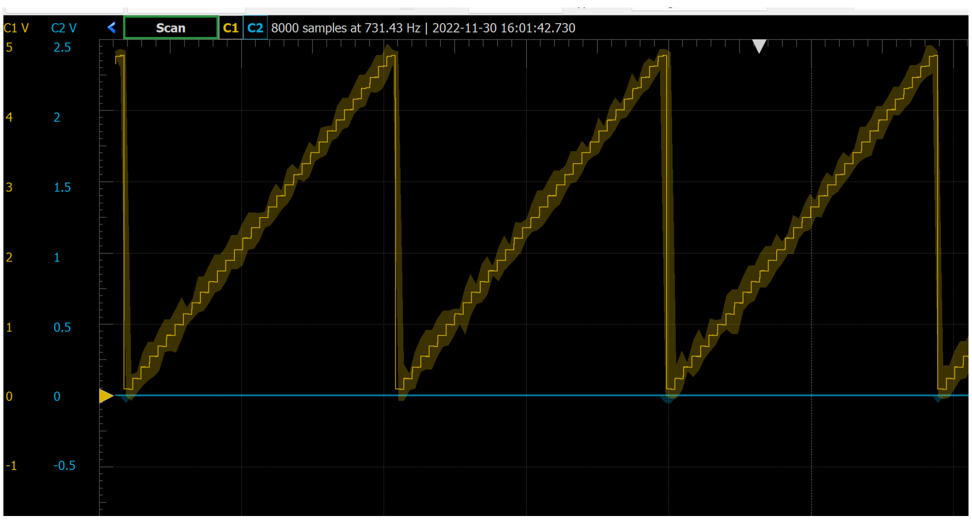

Figure 48: Sawtooth output with a buffer

If we actually measure our voltage:

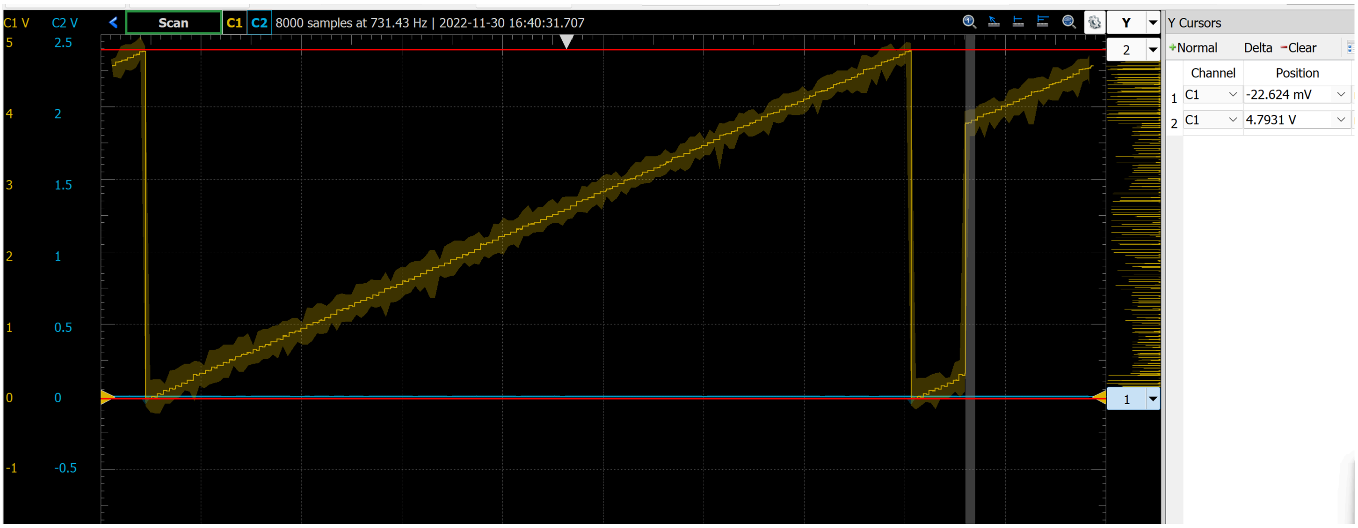

Figure 49: Measuring sawtooth output with a buffer

4.4 Motor sensor and motor driver

The circuit diagram for the the combination of both the motor sensor and the motor driver is shown below:

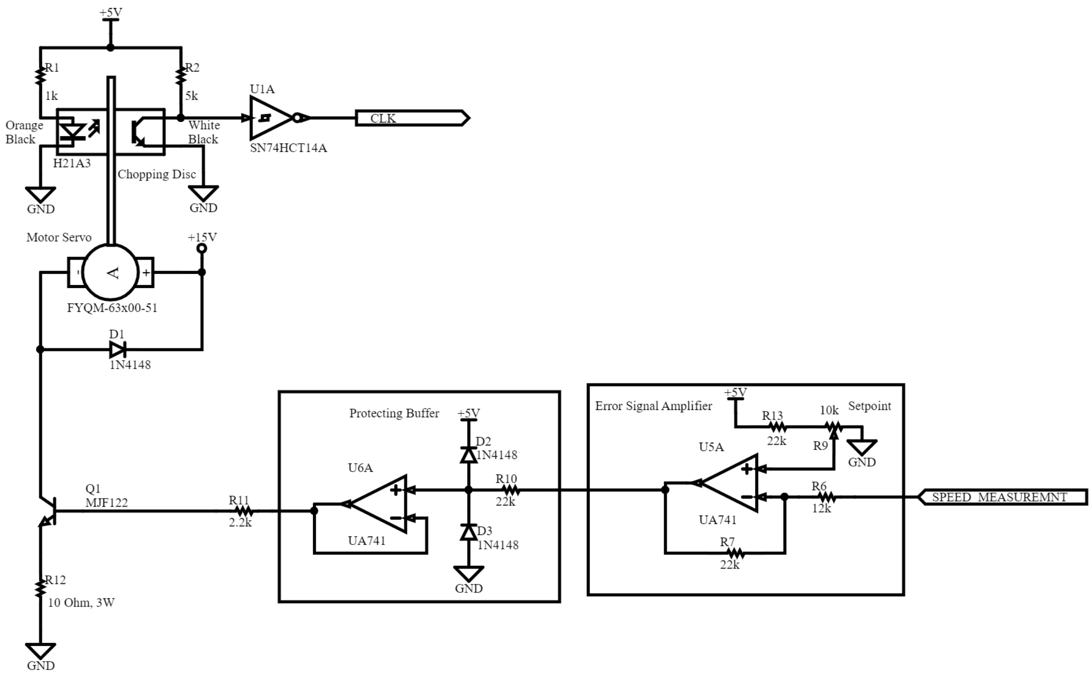

Figure 50: Circuit diagram for the Motor sensor and the motor driver

Individually, the motor sensor (left) and the motor driver (right) are shown below:

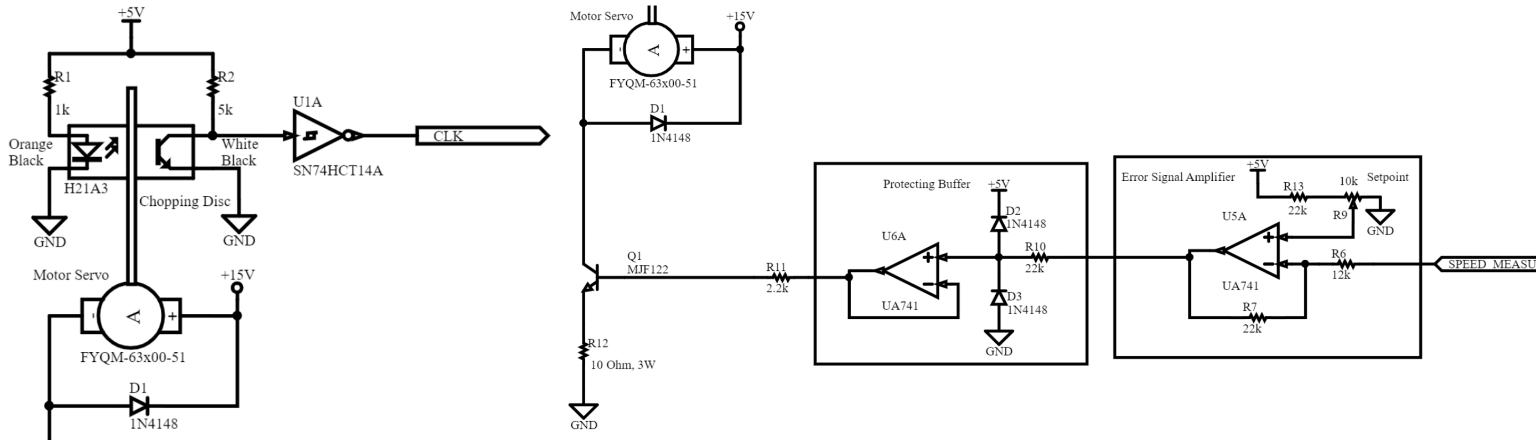

Figure 51: Circuit diagram of the motor sensor (left) and the motor driver (right)

The motor sensor consists of a photodiode (labeled as H21A3) next to a phototransistor. When a current goes through a photodiode, light is generated (the light generated is represented as the two arrows angled upwards in the leftmost diagram above). The light is then detected by the phototransistor, which then generates a voltage output. This output is then inverted by the Schmidt-Trigger inverter labeled as U1A and outputted as our CLK pulse (we need to connect the white wire to the input pin of the inverter on the other end). Both the photodiode and the phototransistor are connected to a +5V source at one end (the brown and white wires are connected to a +5V input an a resistor) and a ground at the other end (the black and red wires are both connected directly to ground) because a current is needed to power both the photodiode and the phototransistor.

The diode labeled D1 in the leftmost image in the figure above is to used to make sure that no current will go through the diode from right to left as the diode will only allow current to flow in the direction of the arrow (assuming the voltage across is high enough) and will prevent voltage from flowing in the opposite direction of the arrow (unless the voltage is at the "break down" voltage).

Figure 52: Graph showing the positive and negative parts of the diode

The output of the inverter labeled as U1A is represented, or equivalently the CLK pulse, is represented by the voltage output below:

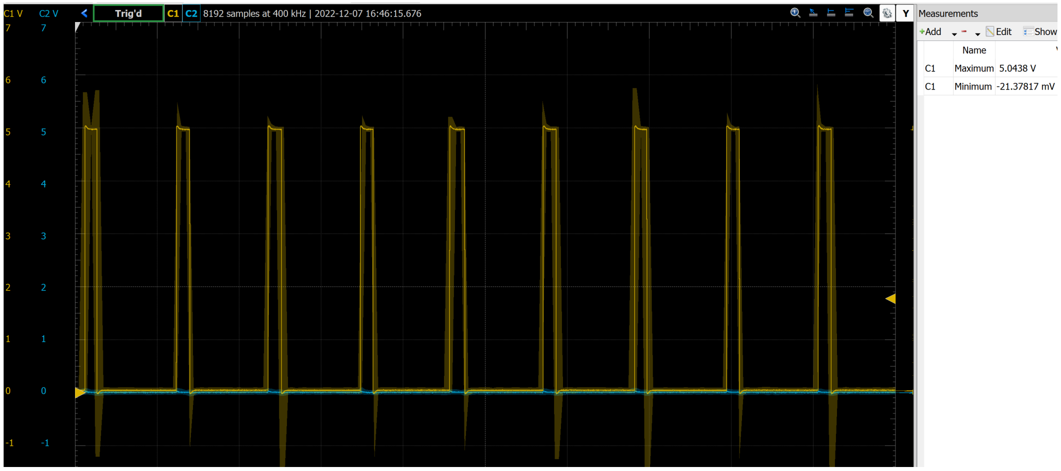

Figure 53: The output of the inverter, or the CLK pulse, as a graphical representation

The motor driver consists of the Error Signal Amplifier and the BJT, both of which are explained in the following sections below.

4.4.1 BJT background

We are using an *npn* flavor of the BJT (BJT stands for Bipolar Junction Transistor) (there are two flavors, *npn* and *pnp*) for this lab. An *npn* BJT is shown below. The letter "C" in the figure below stands for "Collector", while "B" stands for "Base", and "E" stands for emitter. It is generally true that the base-emitter and base-collector ports effectively act like diodes (as shown in part b) of the figure below). It should be noted, however, that a BJT cannot be formed via connecting two diodes as portrayed in the figure below. The BJT will effectively act like a current amplifier (following the relation, $I_C = \beta I_B$, where β is generally in the ranges of 20 to 100, depending on the transistors) if the following three conditions are met:

- The collector voltage relative to the emitter voltage obeys $V_C > V_E$ (i.e collector voltage is more positive than emitter voltage).
- The base-emitter diode is forward biased.
- The base-collector diode is reverse biased.

The fact that we can use a small current I_B to create a larger current I_C is a useful property and will be used to control the current of a DC motor.

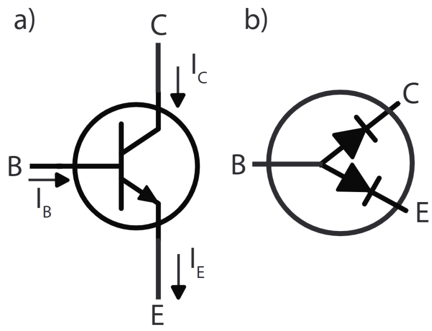

Figure 54: a) Block diagram of BJT. b) Simplified diode model equivalent of BJT

If we measure the voltage across the BJT in our circuit, we see an oscillating wave, indicating the process by which the current goes through the transistor only if the three conditions above are met

Figure 55: Voltage across BJT in our circuit

4.4.2 Motor control with BJT

The BJT is circled in the diagram below:

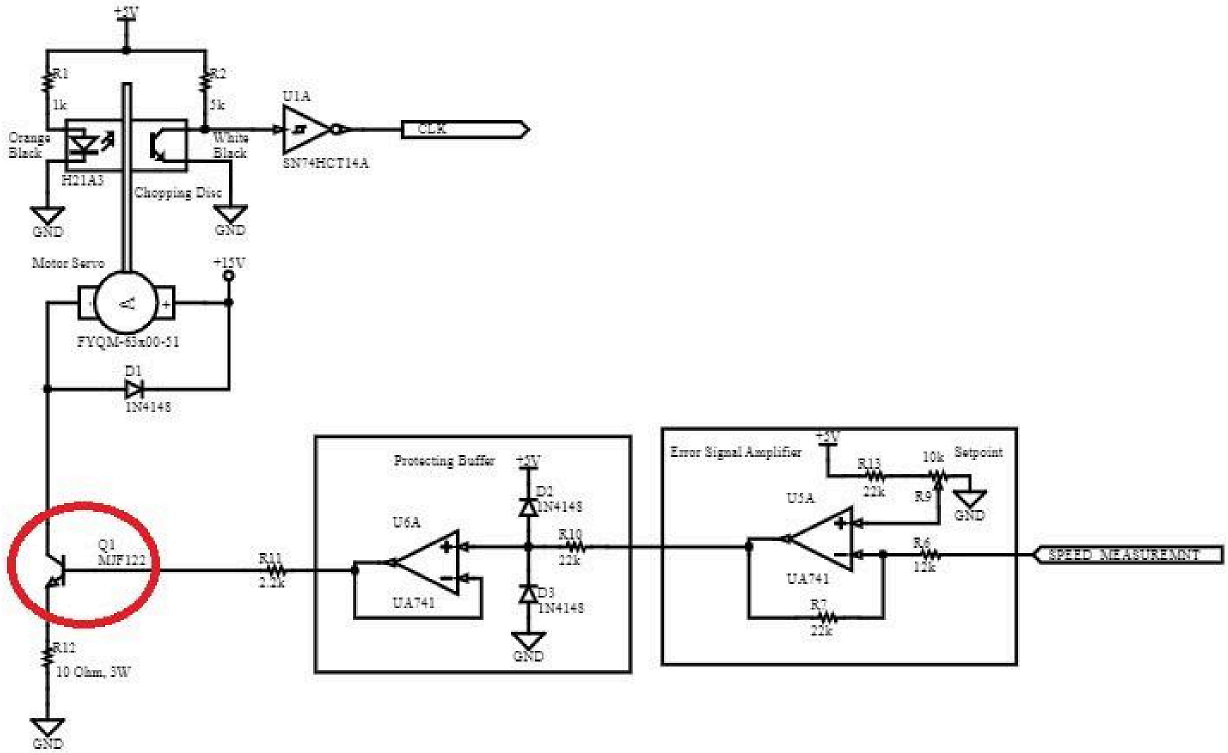

Figure 56: BJT circled in the circuit diagram

Because the BJT effectively acts like a current amplifier, the current to the motor can be adjusted based on the relative values of V_C and V_E.

4.5 Error signal amplifier/buffer

The circuit diagram for both our Protecting Buffer and our Error Signal Amplifier is shown below:

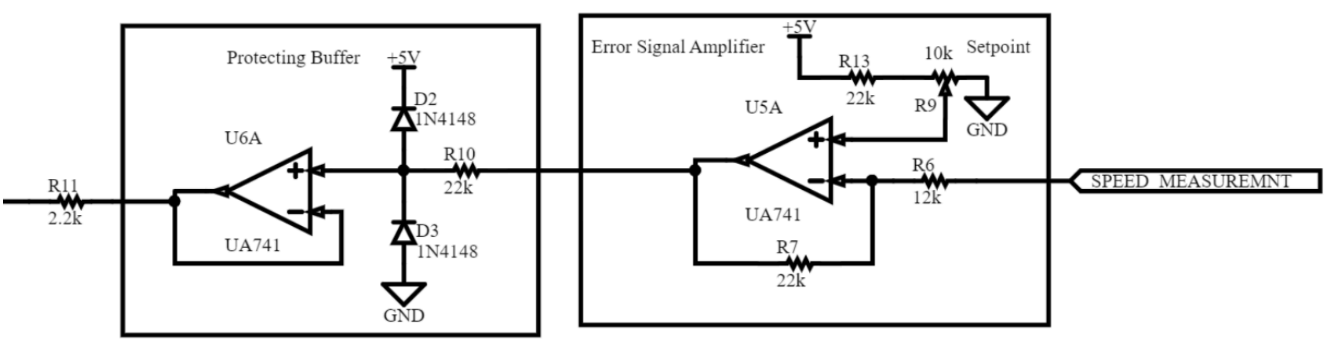

Figure 57: Circuit diagram for both our Protecting Buffer and our Error Signal Amplifier

The speed measurement is generated by the DAC (meaning it is an analog signal) and goes through a buffer. The signal then enters the Error Signal Amplifier, which amplifies the difference between the voltage of the negative input of the OpAmp (i.e the voltage that corresponds to the number of rotations) and the voltage at the setpoint (the point labeled "Setpoint" in Fig. 39 above, which we can control via the potentiometer). The reason we have the error signal amplifier is to amplify our voltage to a value that can be used by our BJT (which is described in sub-section 4.4.1 below).

The protecting buffer is used to keep the output voltage of our Error Signal Amplifier within a stable range (specifically between 0 V and 5 V because we the OpAmp is connected to a +5 V source and the ground) in order to be used by the BJT. Because the diodes restrict the motion of current through them to only one direction, the diodes play a role in stabilizing the voltage signal to be applied to the BJT.

The voltage across the diode in the protecting buffer is shown below. The voltage across the diode remains relatively constant (staying between 1.6511 V and 1.8312 V), indicating the diode's importance in stabilizing the output voltage signal.

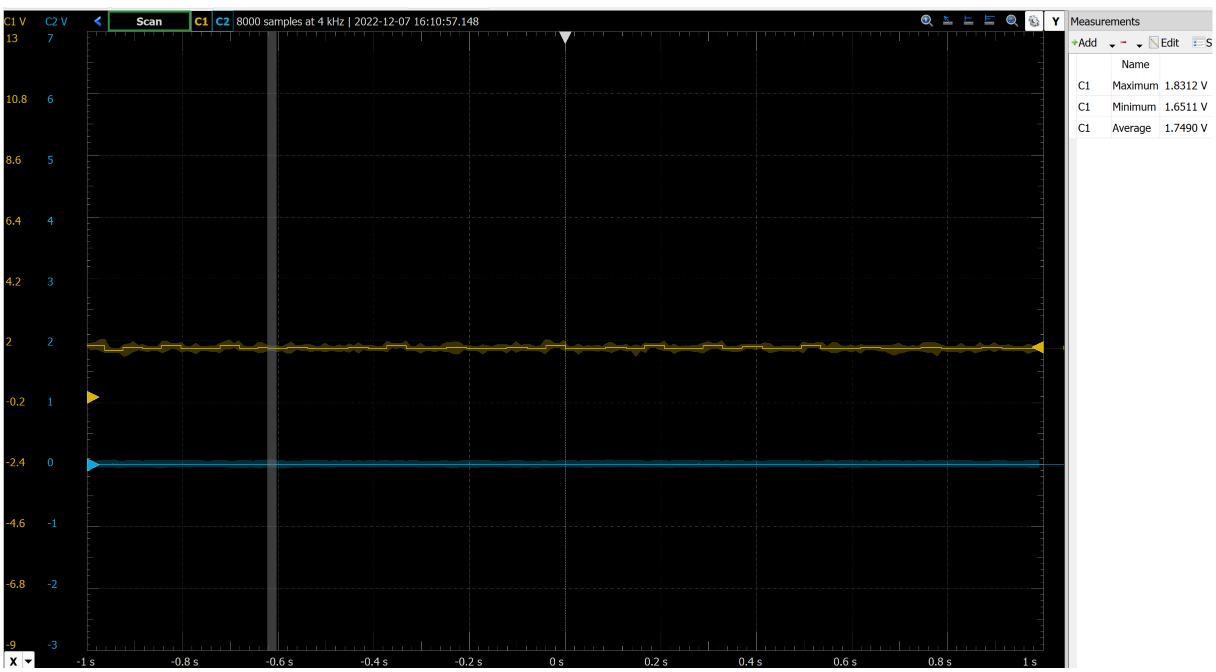

Figure 58: Graph showing the voltage across a diode in the protecting buffer over time

The combined circuit (with the BJT and Error Signal/Amplifier) is shown below:

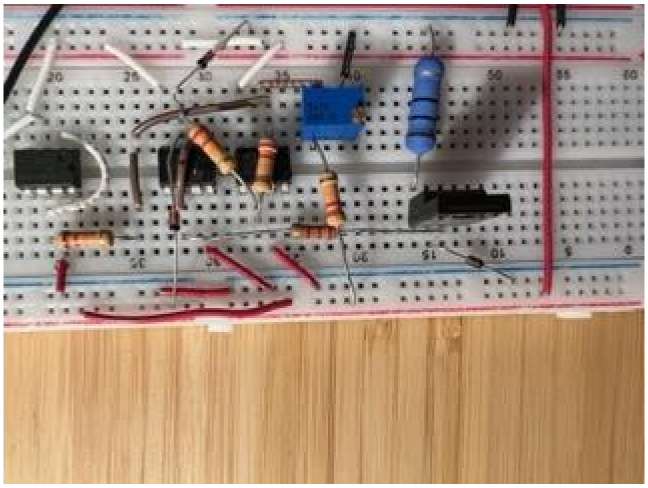

Figure 59: Image of combined circuit with the BJT and Error Signal/Amplifier

5. Conclusion

Image of our finished circuit:

Once finished, the entire circuit looks like:

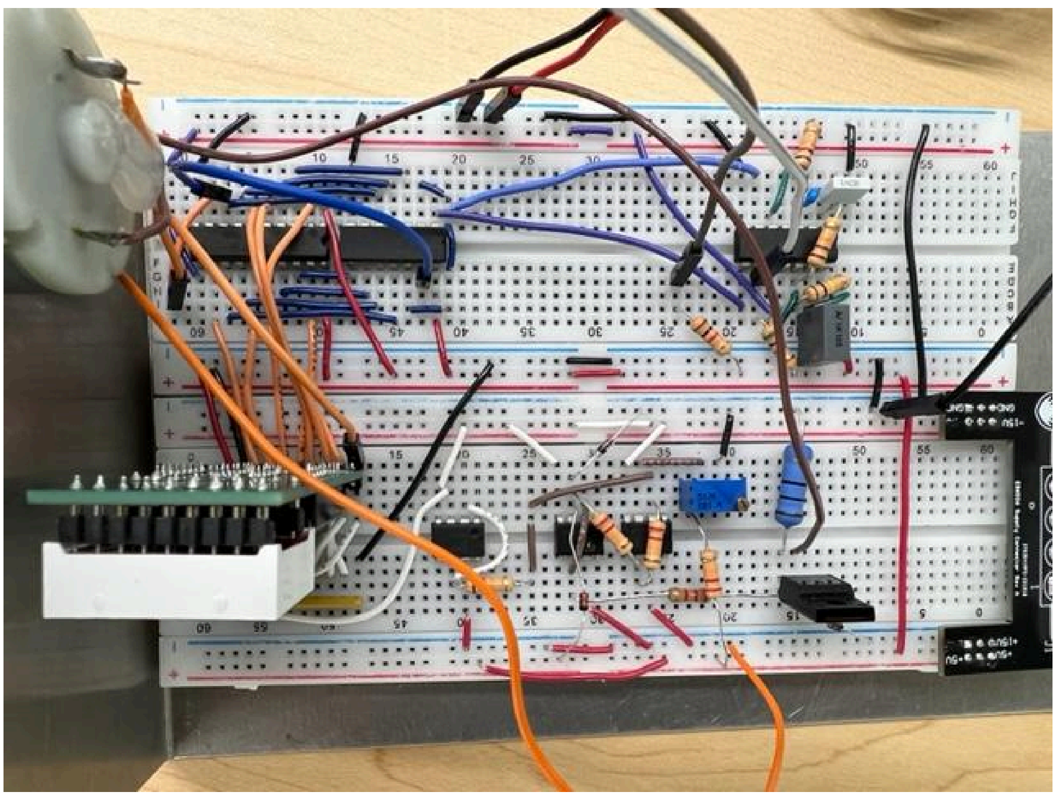

Figure 60: Image of the entire circuit

Voltage output corresponding to different numbers on the counter:

Important Facts:

- Rotating potentiometer coutner clockwise decreases the rotation speed, and rotating clockwise increases rotation speed.
- Yellow line in graph corresponds to voltage output across potentiometer
- To calculate RPM (Rotations Per Minute):
- $\text{RPM} = \text{counter number converted to decimal}\left(\frac{\text{clk}}{\text{reset}}\right) * 24.7\ \frac{\text{reset}}{s} * \frac{1\ \text{revolution}}{10\ \text{clk}} * 60\ \frac{s}{\text{min}}$
- To convert from heximal to decimal, starting with a hexadecimal number of n digits ($d_{n-1}...d_2d_1d_0$):

$$\text{decimal number} = 16^{n-1}(d_{n-1}) + 16^{n-2}(d_{n-2}) \ldots + 16^1(d_1) + 16^0(d_0)$$

For a counter output of 5, we get the following voltage (if we measure the voltage across the potentiometer):

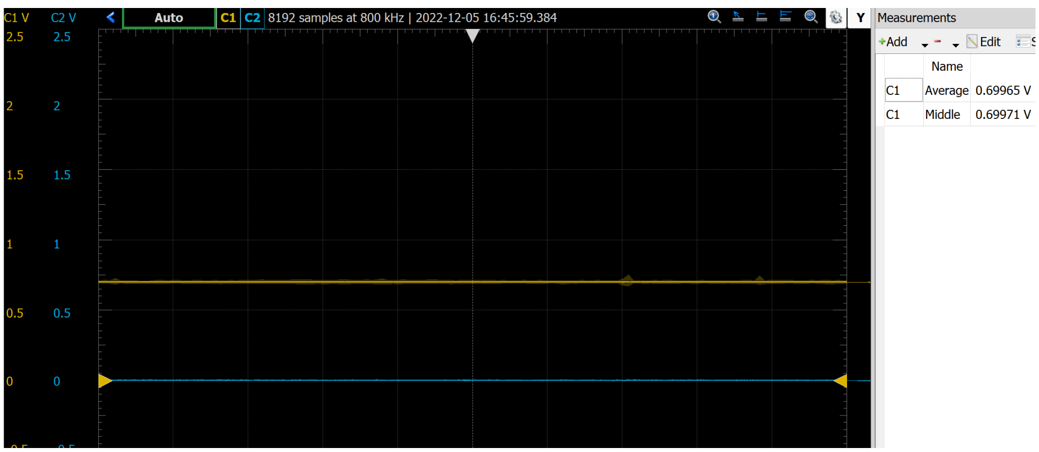

Figure 61: Voltage output for counter output of 5

For a counter output of 7, we get the following voltage:

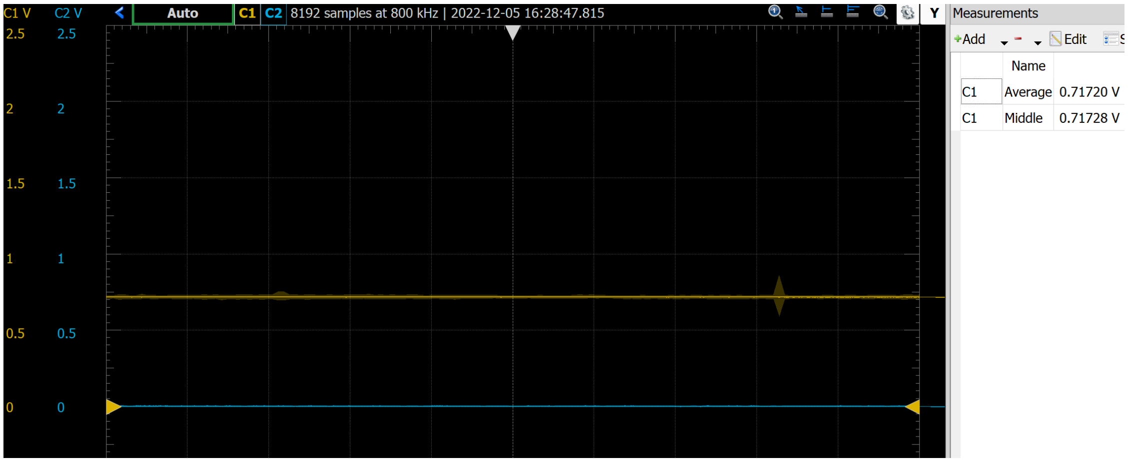

Figure 62: Voltage output for counter output of 7

For a counter output of 12, we get the following voltage:

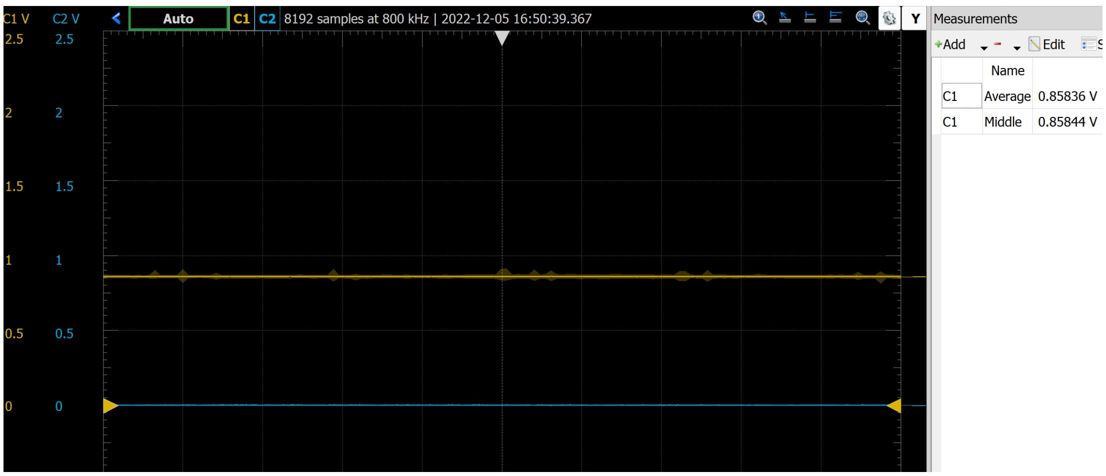

Figure 63: Voltage output for counter output of 12

For a counter output of 15, we get the following voltage:

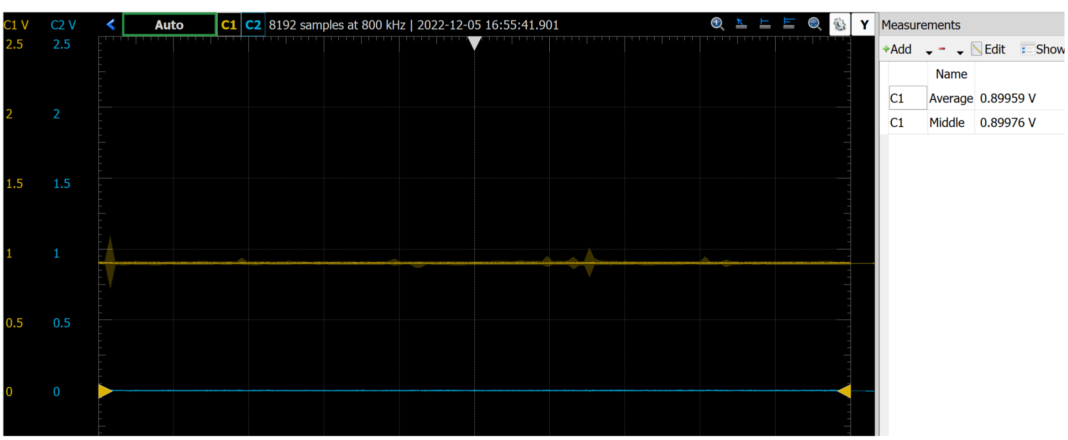

Figure 64: Voltage output for counter output of 15

For a counter output of 23, we get the following voltage:

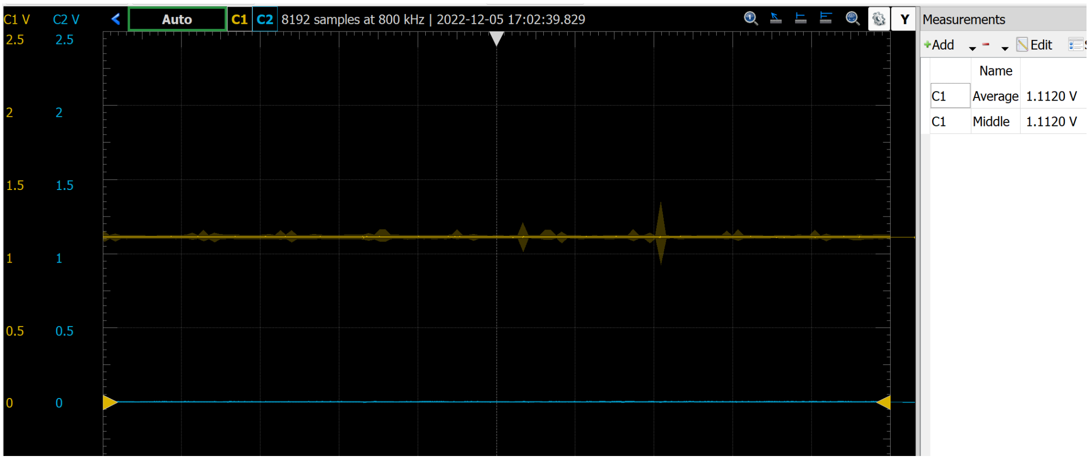

Figure 65: Voltage output for counter output of 23

Conversion Table and Graph:

If we make a table showing the relationship between the counter output, voltage across the potentiometer and the RPM we get:

Counter Number (in hexadecimal)	Counter Number (in decimal)	Voltage	RPM
5	5	0.69965	741
7	7	0.7172	1037.4
12	18	0.85836	2667.6
15	21	0.89959	3112.2
23	35	1.112	5187

Figure 66: Table showing the relationship between the counter output, voltage across the potentiometer and the RPM

How circuit could be modified so display shows RPM:

If we could modify the circuit so that the RPM is displayed, we would need to do multiple things. We would initially need to add a second seven segment display in order to display all the relevant digits. We could also add a $\div 5$ and a $\div 2$ counter (via the 74HC390 device, whose circuit schematic is shown below) to convert our signal into decimal:

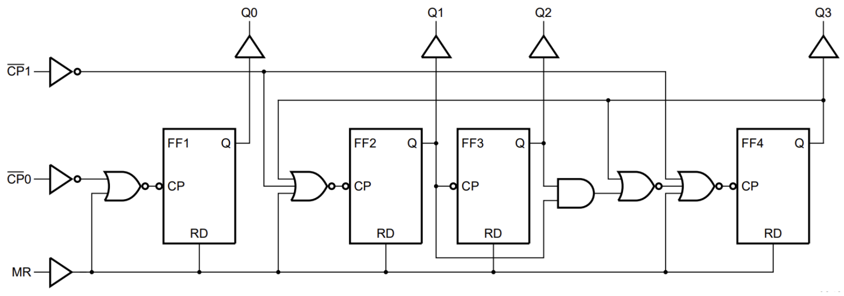

Figure 67: Circuit schematic of the the 74HC390 device

Therefore, the only step left is to use resistors and capacitors of different values so as to change the frequency of the LATCH pulse.

Maximum Speed of Motor:

If we convert the counter number on the seven segment display from hexadecimal to decimal, we get the following graph below:

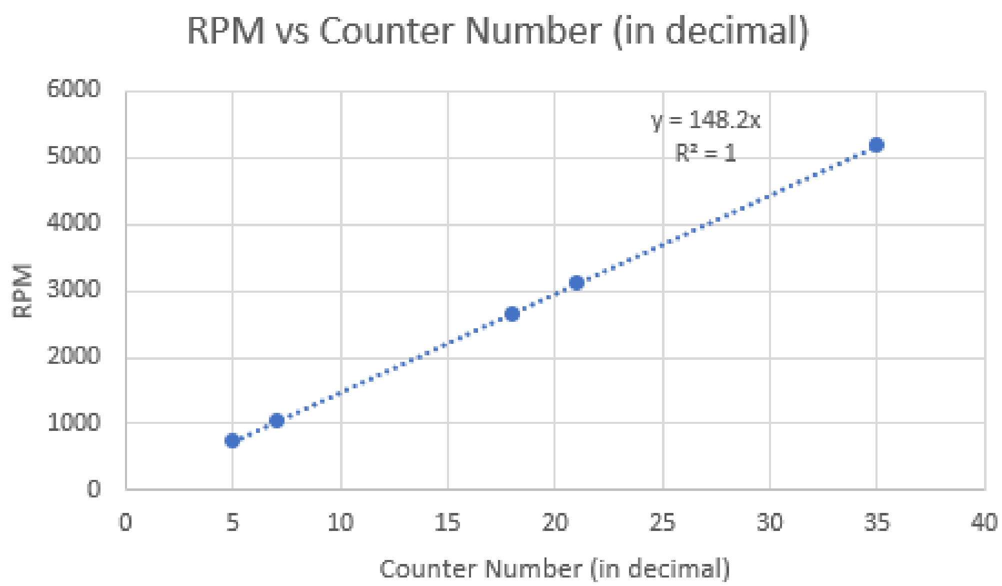

Figure 68: Graph showing RPM as a function of decimal counter number

Eventually, we will reach a point in which the number on the seven segment display will not change even though we are increasing the voltage at the potentiometer. This number rapidly oscillates between 2F, 30, and 31. The average is 30. We have to convert this number from hexadecimal to decimal, the result being 48.

Therefore, if we use our formula $\mathrm{RPM} = 148.2 * \mathrm{Decimal\ Number}$, we find that the maximum RPM of the motor is $148.2 * 48 = 7113.6\ \frac{\mathrm{rotations}}{\mathrm{min}}$

Final Words:

The ultimate goal of this lab was to build a circuit in which we were able to actively control the speed of an electric motor, with the speed displayed. Without question this lab was the most challenging project so far in my Engineering studies. The lab was a summation of everything we had learned all year and it was gratifying to be able to put all the knowledge about the different components together in one circuit. More importantly, however, I found out about how many potential things can go wrong. I would say the most important thing I learned in this lab is how to efficiently troubleshoot. If I could time travel back to the beginning of this lab, I would put more emphasis during troubleshooting on measuring the output signals of the components rather than checking to see if my circuit matches that of the schematic in the lab. For example, when my circuit was not working due to a faulty motor, I spent too much time checking to see if all the wires were placed in the right location, when I could have simply checked the output signals from the very beginning to detect the flaw in the motor. I ended up analyzing the output signals of each individual pin of my 74HC14A device to finally conclude that the phototransistor within my motor was flawed. This will hopefully help me not only for future co-ops but in Robot Summer where we will be building much more complex circuits for our robot.