Electronics for the Belle II Time-of-Propagation Counter

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Abstract

This document describes the electronics for the Belle II particle identification system, the time-of-propagation counter. This description, last updated June 3, 2011, is preliminary, and will likely change prior to final system deployment. It details the various hardware components and documents the required specifications of each, including any accompanying firmware, drivers, or software. The requirements for the upcoming fall 2011 beam test are also described, when they differ from those of the final system. A schedule is proposed for completing both the beam test and final development, with major milestones enumerated.

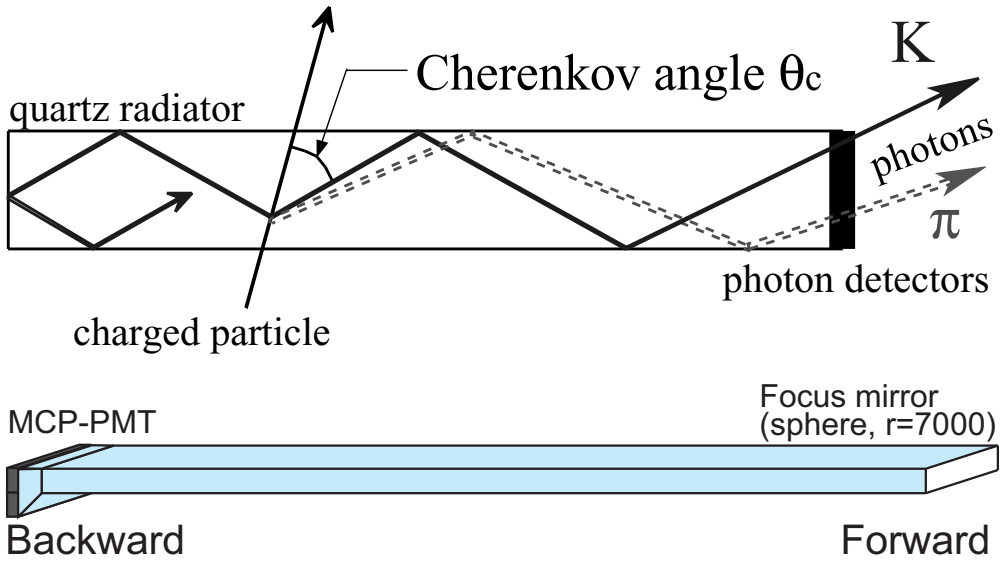

FIG. 1: (Above) A diagram of the general TOP concept, as used to distinguish kaons and pions. (Below) A single Belle-II TOP module (readout electronics not shown).

I. INTRODUCTION

The time-of-propagation (TOP) counter will serve as the primary particle identification device in the barrel region of Belle II. The TOP counter is described in detail elsewhere, both generically and the configuration planned for Belle II [1–4]. We describe its geometry only briefly here. A set of 16 fused-silica bars with refractive index ~ 1.45, each approximately 265 cm $\times$ 45.4 cm $\times$ 2 cm, are arranged in a barrel configuration around the interaction point. A diagram of one of the 16 modules is shown in Figure 1. Charged particles emit Cherenkov radiation as they pass through the bar, some fraction of which undergoes total internal reflection down the bar. Light emitted in the forward direction is focused and reflected by a spherical mirror at the front end of the bar. At the backward end of the bar, a 10 cm fused-silica trapezoidal expansion "wedge" couples the 45.4 cm $\times$ 2 cm cross-section of the main bar with an image plane of area 45.4 cm $\times$ 5.5 cm. At the image plane, photons are detected by a micro-channel plate photomultiplier tube (MCP-PMT), the Hamamatsu SL10 [5].

From this point, the remainder of the system consists of the front-end electronics and its associated back-end, trigger, and support electronics. Since the effectiveness of the TOP technique relies on precision measurements of photon arrival times, the primary requirement

of the TOP electronics is to determine and record these arrival times at the limit of the photodetector timing resolution ($\sim$ 50 ps). A system overview is provided in Section II, along with more detailed descriptions of various system components in Sections III through VI. Each section begins with the description of the expected Belle II TOP configuration. Beam tests of TOP modules occurring before Belle II begins operation, such as that scheduled for September of 2011, may have a different configuration than the final system. As such, we also list any such differences in each section. Section VIII closes with a discussion of the current status of various systems, including milestones toward readiness of the full and beam test versions of the TOP, and an estimated schedule for completion.

II. SYSTEM OVERVIEW

A block diagram of the electronics system for each bar is shown in Figure 2. The front-end electronics read signals from, and are mechanically coupled to, the MCP-PMTs. The front-end digitizes selected waveforms in a region of interest, as indicated by the Belle II global trigger, using a variant of third-generation Buffered Large Analog Bandwidth (BLAB3) ASICs [6]. These waveforms are transmitted to the back-end electronics for feature extraction and data reduction. The front-end also provides coarse timing information ($\mathcal{O}$(ns)) on the arrival time of all photo-electron signals from the SL10s. These times and their associated channel numbers are transmitted to dedicated TOP trigger electronics. Both the waveform data and trigger data are sent by fiberoptic links to the back-end and trigger electronics, respectively. The overall timing between front-end modules is synchronized by running all state machines on all modules from a distributed clock, provided by the support electronics.

The back-end electronics accepts raw digitized waveforms from the front-end modules via fiberoptic cable. The back-end can then pass along these waveforms as the final output data stream, or, as intended for the final system, apply all applicable calibration constants, perform some feature extraction algorithm to determine the charge and time (analogous to ADC and TDC values), and pass along only this reduced, feature-extracted data as the final output.

The TOP trigger electronics receives by fiberoptic the coarse time and channel information of each photo-electron signal detected on the front-end. These modules collect and

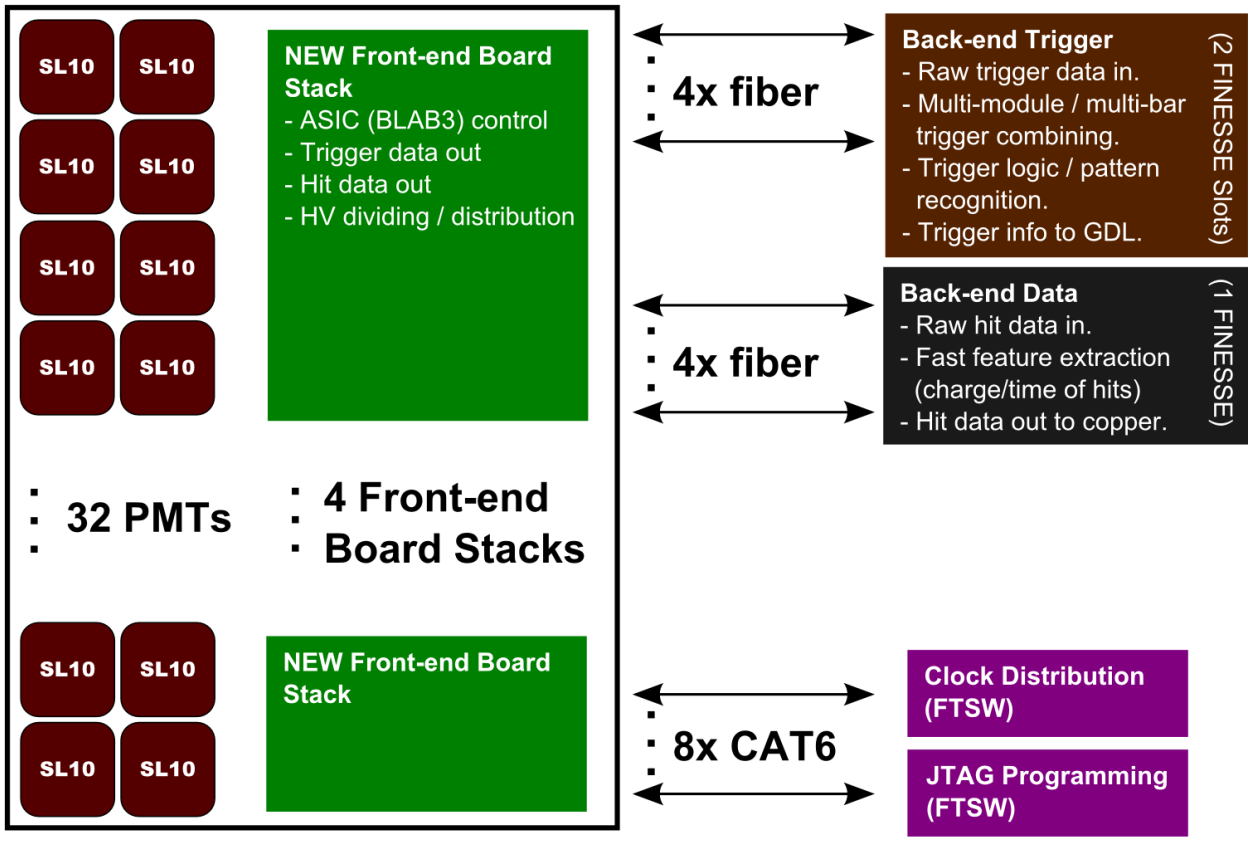

FIG. 2: Block diagram of the electronics corresponding to one of the 16 barrel PID modules.

combine this data from multiple front-end modules. This combined trigger data set is used to estimate, at the $\sim$ ns level, the time of the collision event, which is in turn provided to the Belle II Global Decision Logic (GDL) to reduce out-of-time hits from the Silicon Vertex Detector (SVD).

Support electronics modules facilitate timing synchronization between front-end modules as well as allowing for remote programming of the front-end FPGAs.

Although the beam test and final systems are functionally identical, the number of modules, data and hardware protocols, and some details of the data streams, vary between the two systems.

A. Final System

The final system block diagram is shown in Figure **??**.

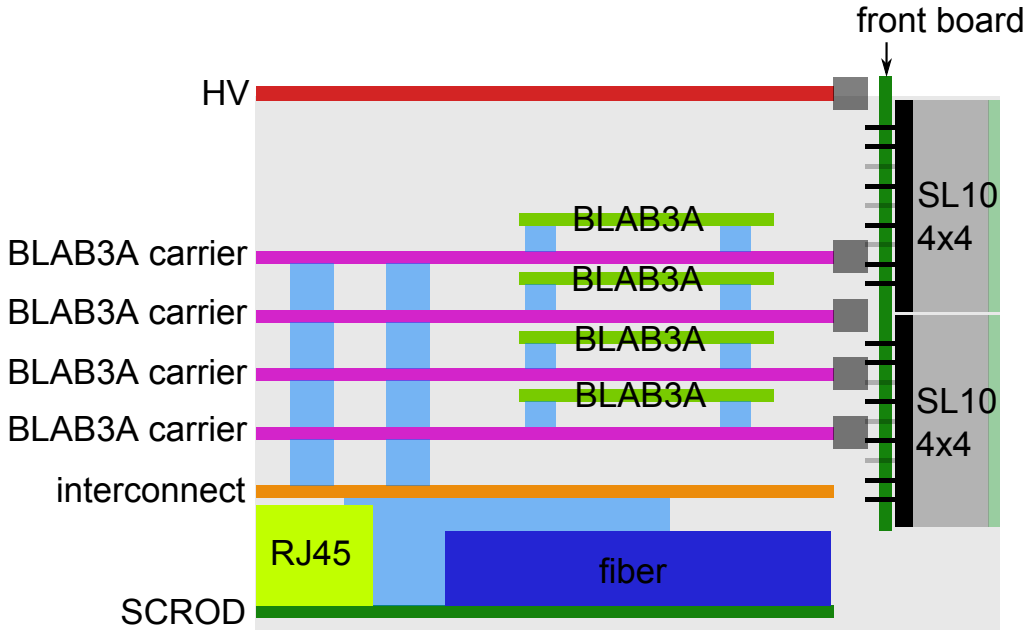

FIG. 3: Scale diagram of the front-end board stack.

B. Beam Test System

The beam test system block diagram is shown in Figure **??**.

III. FRONT-END ELECTRONICS

A. Final System

The front-end electronics is the first point-of-contact to the photodetectors. The current design consists of a set of PCBs, sometimes referred to as the "front-end board stack" or "front-end readout module." A scale sketch of this board stack is shown in side view in Figure 3. The following are the boards that are a part of this stack.

1. Standard control, read-out, and data (SCROD)

A photograph of the current SCROD is shown in Figure 4. The final version of the SCROD has the following hardware features:

- Xilinx Spartan-6 (XC6SLX150T, package FGG676, speed grade 3). This FPGA provides all the logic signals necessary for the front-end board stack.
- Two fiberoptic transceivers, Avago model AFBR-57R5AEZ. One link carries waveform data (and support data necessary to process waveforms). The other carries trigger information.
- Two RJ45 connectors for receiving LVDS data. One connects to an LVDS transceiver, and allows for remote JTAG programming of the SCROD. The other connects directly to the FPGA. This link is used to receive the distributed clock, orbit, and trigger signals from the support electronics. One extra LVDS pair is reserved as a spare.
- A JTAG header for direct USB programming. This is primarily for standalone testing and debugging. Three jumpers can be added or removed to toggle the programming interface between the JTAG header and the RJ45.
- Two onboard clocks (frequencies 250 MHz and 156.25 MHz). Jumpers allow these clocks to be disabled. In this case, the FPGA clock must be provided remotely. The clocks will not be populated for the final boards.
- A USB connector and Cypress FX2-LP USB controller. This is primarily for development and debugging, allowing a PC interface to the SCROD without the extra infrastructure needed for the fiberoptic interface.
- Sixteen LEDs for limited visual debugging and monitoring.
- An EEPROM with I^2C interface that allows idenfication and enumeration of specific SCROD modules.

The firmware for the SCROD must perform the following tasks for final operation of the board stack:

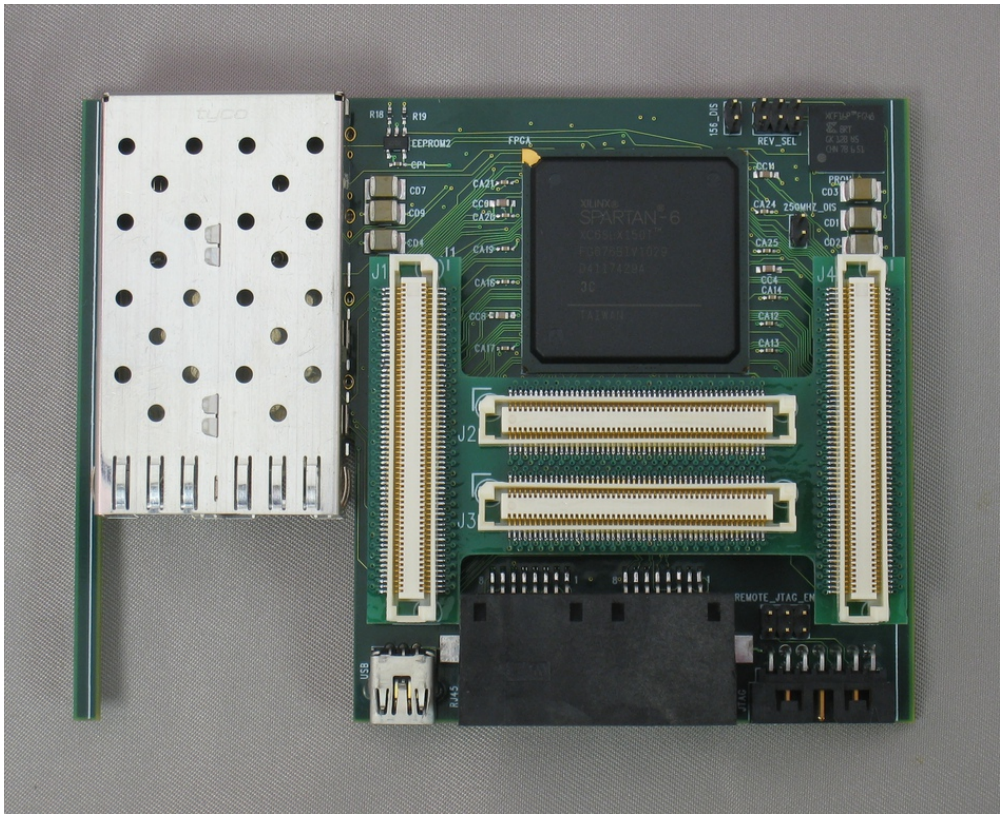

FIG. 4: Photograph of SCROD, revision A.

- Control of the 16 ASICs in the board stack to continuously sample and buffer waveforms from the SL10s.
- Slow control for the same ASICs, to set DACs which control sampling rates and digitization parameters.
- Transmission of triggers received from any SL10 anode (128 anodes per front-end module). The channel and time of each trigger are encoded and sent to the trigger system for inclusion in the Belle-II GDL.
- Control of digitization in the ASICs for the appropriate time window of interest upon receipt of a global trigger signal from the GDL.
- Transmission of the waveform data from selected ASICs to the back-end electronics for feature extraction. This transmission will most likely occur using the Belle-II link format and protocol.
- ASIC dead channel testing, using AC coupled FPGA pulse outputs.

2. Interconnect board

The interconnect board distributes unregulated low-voltage DC power to the other boards in the stack. Other boards in the stack requiring power have local power regulation. The interconnect board also passes logic signals between SCROD and all ASICs in the board stack.

3. ASIC Carrier Board

Each board stack contains four ASIC carrier boards. Each carrier board connects to the front board (described below) to pass the analog signals to the ASIC daughter cards.

4. ASIC Daughter Card

Each ASIC carrier board connects to four ASIC daughter cards. These hold one ASIC each, as well as any voltage regulators required to operate the ASIC.

5. High voltage board

This board contains voltage dividers to supply various high voltages for the SL10s. Five voltages are required for each SL10, so 40 high voltages in total are distributed out to the front-board for eventual distribution to the SL10s.

6. Front board

The front board is the point of contact between eight SL10s and the rest of the board stack. High voltage signals are accepted from the HV board and distributed to the SL10s. Analog signals are accepted from the SL10s and passed to the ASIC carrier cards.

B. Beam Test System

1. Hardware Differences

The beam test front-end board stack consists of all the same components as the final system. The main differences in hardware are the following:

- The beam test version is too large to fit in the current bPID envelope. The front board, in particular, was split into two front boards. The first, designated the "front-front" board, primarily handles HV distribution from the HV board to the SL10s and simply passes the signals through to the "front-back" board. The front-back board then distributes the anode signals to the ASIC carrier boards for digitization.

- The HV board is larger than the final version so that it mates properly with the front-front board.

- The ASIC for beam test is nominally the BLAB3A. The final planned ASIC is the BLAB3B. The two ASICs should have similar performance, but some components, such as tri-state buffers and DACs, which control trigger thresholds, sampling rates, and biases, are not built-in to the BLAB3A. Rather, these tasks are performed by commercial components that reside on the ASIC daughter cards. As a result, the BLAB3B carrier cards may be significantly smaller than the existing BLAB3A carrier cards.

- The interconnect board is significantly longer in the z-direction than the final version. This extra room allows for monitor headers and probe pads that facilitate debugging.

- Some minor problems have been identified on the SCROD board, which will require a redesign for the final version, but do not preclude its use as-is for beam test.

- Since Belle-II link will not yet be available, fiberoptic communication will be conducted through a standalone Xilinx Aurora core.

2. Operational Differences

In addition to these differences in hardware, there are also a number of features and specifications required for final Belle-II operation that will not be required or exercised at beam test.

- The trigger fiberoptic link will not be utilized. Instead, data packets that contain trigger information will be sent through the primary data fiberoptic link when a system trigger is received.
- The final system will require the SCROD to interface with each BLAB3B's internal DACs and tri-state buffers. For beam test, the SCROD must control the two external DACs on each ASIC carrier card through an I^2C interface. The SCROD must also control the external tri-state buffer on each ASIC carrier card.

IV. BACK-END ELECTRONICS

The "back-end" consists of an array of "DSP_FIN" boards, which are responsible for feature extraction and data reduction before data is archived for offline analysis. Each DSP_FIN board has the following hardware features:

- Four multi-gigabit fiber optic transceivers to talk to the front-end board stack.
- An FPGA for control (Xilinx Spartan 6 XC6SLX45T FGG484 speed grade 3) and interfacing with the fiber optic transceivers.
- Two Analog Devices Blackfin BF561 dual-core DSPs, each core of which is capable of running software at 600MHz.
- Two banks of 128MiB of SDRAM, each of which is connected to a Blackfin DSP for holding calibration data as well as for deep storage of bursts of waveforms.

The DSP_FIN boards are "FINESSE" (Front-end INstrumentation Entity for Subdetector Specific Electronics) boards, which is an elecromechanical interface originally designed for Belle. Up to four FINESSE boards can mount on a single "COPPER2" (second version of the COmmon Pipelined Platform for Electronics Readout) motherboard (see Figure **??**). COPPER2 is a 9U VME motherboard that interfaces the FINESSE boards via

deep (1MiB) FIFOs to an FPGA that talks over PCI to a Radisys PMC single board computer running linux, which sends data via ethernet to the "DAQ" subsystem downstream for archiving and further processing.

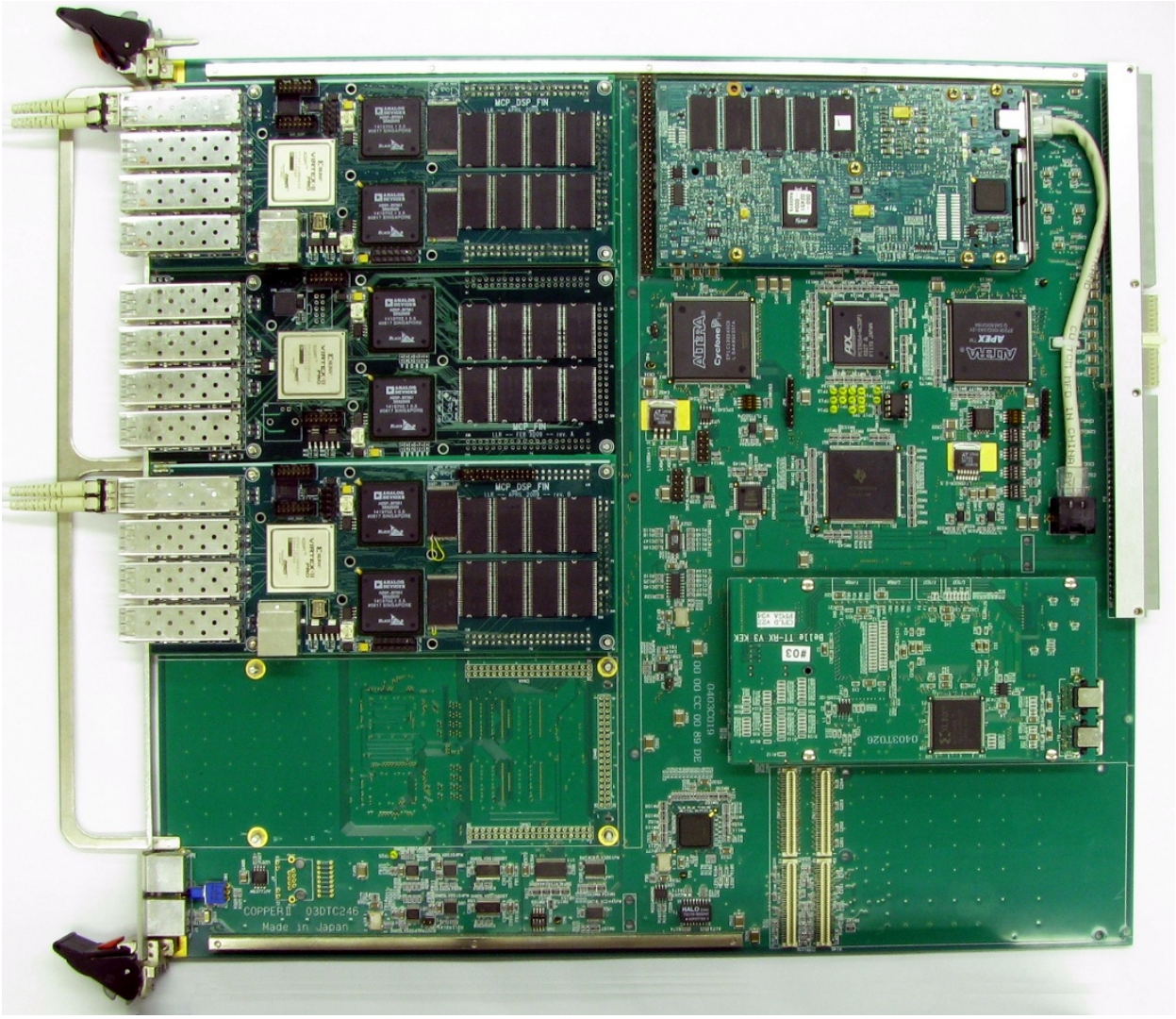

FIG. 5: DSP_FIN boards mounted on COPPER motherboard with Radisys PMC Single-Board Computer

The beam-test version of the back-end is very similar in that it has the same number of fiber optic transceivers, FPGAs to accept data and DSPs to process that data. However, the board also includes a dedicated FPGA to talk via a "cPCI" (compact Peripheral Component Interconnect) interface to a computer running linux to archive data locally for further processing, storage and offline analysis.

The FPGA firmware for the fiber transceiver side of either back-end system must perform the following tasks:

- Generate clocks and control signals to allow Analog Devices Blackfin DSPs to boot and start executing software.
- Transmit and receive data with an Aurora protocol layer riding on a Xilinx Spartan 6 RocketIO Gigabit Transceiver (GTP).
- Buffer received waveform data from front-end and send it via DMA (Direct Memory Access) to Blackfin DSP over the PPI (Parallel Peripheral Interface) for processing.
- Accept processed waveform data and results via DMA from Blackfin DSP and send it downstream to PC for archiving and further processing.
- Accept housekeeping and other data from front-end and deliver it directly downstream to PC for archiving and further processing.
- Accept calibration and other data from PC and send it upstream to front-end.

For the 2011 beam-test version (DSP_cPCI), the firmware for the PCI transceiver FPGA must perform the following tasks:

- Take data packets from the other two FPGAs on the board (that control the fiber optic transceivers and interface with the Blackfin DSPs) and deliver them in consolidated form to the PC via the PCI interface.
- Deliver data packets from the PC to the two other FPGAs on the board for distribution to the DSPs and/or the front-end boards via the fiber optic link.

The DSP firmware must perform the following tasks:

- Setup the PLL (Phase-Locked Loop) inside the DSP to generate all necessary clocks for operation at desired frequency based on the clock from the FPGA.
- Setup the SDRAM controller based upon this clock rate and the speed grade of the SDRAM on the board.
- Setup one channel of PPI (Parallel Peripheral Interface) and DMA (Direct Memory Access) to accept data from the FPGA.

- Setup a queueing system via interrupts whereby the software has a count of how many waveforms it has received and is yet to process.
- Setup the other channel of PPI and DMA to send processed data back through the FPGA downstream to the PC for archiving and further processing.
- Setup a queueing system whereby the software keeps track of how many waveforms have been processed whose results are waiting to be sent back to the FPGA.
- Enable / wake up the second core of the dual-core DSP and allow it to process waveforms in parallel with the first core.
- The main part of the program for each DSP core performs the following tasks for each loop iteration:
  - Checks the unprocessed waveform counter and if there is at least one unprocessed waveform waiting to be processed, it processes a waveform.
  - Checks the processed waveform counter and if there is at least one processed waveform waiting to be transmitted, it initiates a DMA/PPI transmission of processed data back to the FPGA (which occurs in the background).
  - In this manner, the waveforms get processed one at a time until the buffer is empty and the processed data gets transmitted until that buffer is empty.

The innermost algorithm that actually processes the waveform data must perform the following tasks:

- Perform linearity correction.
- Perform pedestal subtraction.
- Perform timebase correction.
- Determine whether there is a pulse in the waveform from the PMT (PhotoMultiplier Tube).
- Extract the time and charge from the PMT pulse.

Various optimizations must occur to make this efficient enough to keep up with the data coming in from the front-end, including but not limited to: DMA transfers from L1 (a few kiB of local memory running at the clock rate of the processor cores), L2 (several hundred kiB of shared memory between cores running at half the rate of L1) and L3 (128 MiB of SDRAM that runs at $\frac{1}{5}$ the rate of the processor cores), using pipelined 16 bit fixed-point math that takes advantage of the Blackfin digital signal processing capabilities.

V. TRIGGER ELECTRONICS

A. Final System

B. Beam Test System

VI. SUPPORT ELECTRONICS: TIMING DISTRIBUTION, JTAG PROGRAMMING

A. Final System

B. Beam Test System

VII. BEAM TEST DATA FORMAT

A preliminary data format has been defined in preparation for the fall 2011 beam test. This format will almost certainly be different than that used in the final system. Data is organized into different types of packets. All packet types are the same length, for ease of firmware development. A packet consists of 140 4-byte words. A number of fields in each packet are identical regardless of packet type. These are listed in Table I. The list of packet types and some of their details are found in Table II. Specific formats for the various packet types are given in Tables III through VII.

VIII. STATUS, SCHEDULE AND MILESTONES

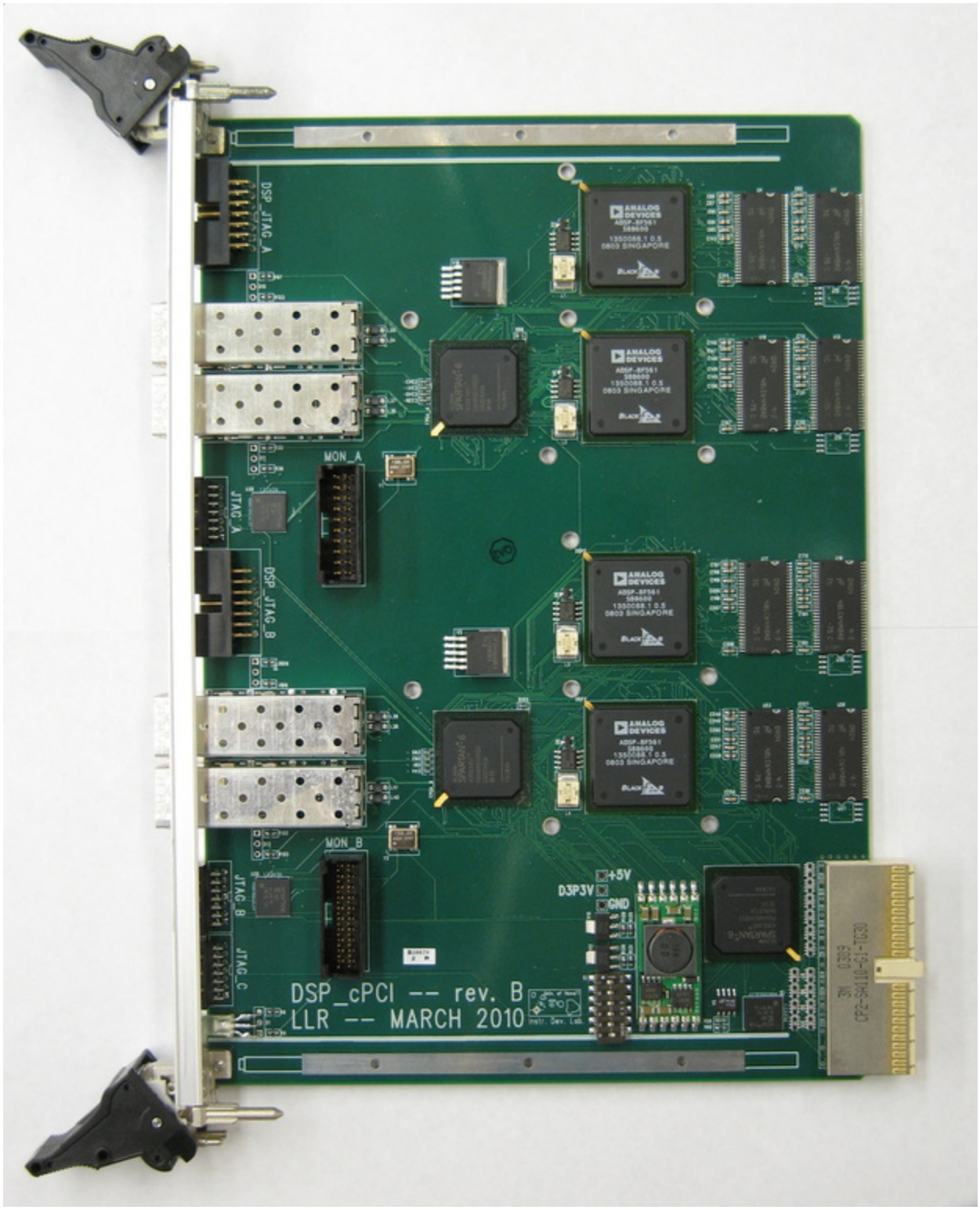

FIG. 6: DSP_cPCI revB assembled, showing 4 dual-core Blackfin DSPs, 4 fiber transceivers and three FPGAs for control

Word	Type	Upper 16 bits	Lower 16 bits	Notes
0	Header	0x00BE11E2		
1	Packet size	0x0000008C		N words (4N bytes), incl. header, footer
2	Packet type	(e.g., 0x00C0FFEE)		See Table II
3	Protocol freeze date	(e.g., 0x20110603)		YYYYMMDD in hex
4	Checksum	(e.g., 0x83E061A3)		32-bit checksum, incl. header, footer, but not itself
...	...	...		...
139	Footer	0x62504944		"bPID" in ASCII

TABLE I: Common 32-bit word fields for all packet types.

Packet	Designator	From	To	Description
Waveform	0x00C0FFEE	Front-end	Back-end	A single 256 sample waveform
Housekeeping	0x000AB0DE	Front-end	Back-end	Scalers, feedback levels, temperatures for one front-end
Trigger DACs	0x1EBE1DEF	Front-end	Back-end	DAC trigger levels for one front-end
Trigger stream	0xCE11B10C	Front-end	Back-end	Trigger bit stream for one front-end
Command	0xB01DFACE	Back-end	Front-end	Command packet to front-end(s)

TABLE II: Packet types, their hexadecimal codes, directionality, and description.

Word	Type	Upper 16 bits	Lower 16 bits	Notes
5	Event number	(e.g., 0x0000001)		Since front-end power-up
6	Channel ID	SCROD ID(31:16)	ASIC#(15:8) & Chan(7:0)	
7	Orbit number	Orbit(31:0)		
9	Reserved			
10	Reserved			
11	Waveform address		row(2:0) & col(5:0)	In ASIC storage array
12	Waveform	waveform_ADC(1)(11:0)	waveform_ADC(0)(11:0)	
13	Waveform	waveform_ADC(3)(11:0)	waveform_ADC(2)(11:0)	
...	...	...		...
138	Waveform	waveform_ADC(255)(11:0)	waveform_ADC(254)(11:0)	

TABLE III: Word field definitions unique to the waveform data packet.

Word	Type	Upper 16 bits	Lower 16 bits	Notes
5	Event number	(e.g., 0x0000001)		Since front-end power-up
6	Scaler rate	scaler(1)(15:0)	scaler(0)(15:0)	One per channel
7	Scaler rate	scaler(3)(15:0)	scaler(2)(15:0)	
...	...	...		...
69	Scaler rate	scaler(127)(15:0)	scaler(126)(15:0)	
70	Wilkinson DAC	DAC setting(1)(11:0)	DAC setting(0)(11:0)	One per ASIC
71	Wilkinson DAC	DAC setting(3)(11:0)	DAC setting(2)(11:0)	
72	Wilkinson DAC	DAC setting(5)(11:0)	DAC setting(4)(11:0)	
73	Wilkinson DAC	DAC setting(7)(11:0)	DAC setting(6)(11:0)	
74	Sampling rate DAC	DAC setting(1)(11:0)	DAC setting(0)(11:0)	One per ASIC
75	Sampling rate DAC	DAC setting(3)(11:0)	DAC setting(2)(11:0)	
76	Sampling rate DAC	DAC setting(5)(11:0)	DAC setting(4)(11:0)	
77	Sampling rate DAC	DAC setting(7)(11:0)	DAC setting(6)(11:0)	
78	Trigger width DAC	DAC setting(1)(11:0)	DAC setting(0)(11:0)	One per ASIC
79	Trigger width DAC	DAC setting(3)(11:0)	DAC setting(2)(11:0)	
80	Trigger width DAC	DAC setting(5)(11:0)	DAC setting(4)(11:0)	
81	Trigger width DAC	DAC setting(7)(11:0)	DAC setting(6)(11:0)	
82	Temperature	Interconnect temp(15:0)	HV temp(15:0)	
83	Reserved			
84	Reserved			
...	...	...		...
138	Reserved			

TABLE IV: Word field definitions unique to the housekeeping data packet.

Word	Type	Upper 16 bits	Lower 16 bits	Notes
5	Trigger threshold DAC	thresdhold(1)(15:0)	threshold(0)(15:0)	One per channel
6	Trigger threshold DAC	threshold(3)(15:0)	threshold(2)(15:0)	
...	...	...		...
68	Trigger threshold DAC	threshold(127)(15:0)	threshold(126)(15:0)	
69	Reserved			
70	Reserved			
...	...	...		...
138	Reserved			

TABLE V: Word field definitions unique to the trigger threshold data packet.

Word	Type	Upper 16 bits	Lower 16 bits	Notes
5	Trigger bits	stream(1)(15:0)	stream(0)(15:0)	One per channel, each bit 4 ns, bit 0 most recent
6	Trigger bits	stream(3)(15:0)	stream(0)(15:0)	
...	...	...		...
68	Trigger bits	stream(127)(15:0)	stream(126)(15:0)	
69	Reserved			
70	Reserved			
...	...	...		...
138	Reserved			

TABLE VI: Word field definitions unique to the trigger stream packet.

Word	Type	Upper 16 bits	Lower 16 bits	Notes

TABLE VII: Word field definitions unique to the command packet.

[1] T. Abe *et al.* (Belle II Collaboration), arXiv:1011.0352.

[2] B. N. Ratcliff, Nucl. Instrum. Meth. **A502**, 211 (2003), 10.1016/S0168-9002(03)00276-6.

[3] K. Inami, Nucl. Instrum. Meth. **A595**, 96 (2008), 10.1016/j.nima.2008.07.045.

[4] K. Nishimura, Nucl. Instrum. Meth **A639**, 177 (2011), 10.1016/j.nima.2010.09.164.

[5] K. Inami *et al.*, Nucl. Instrum. Meth. **A592**, 247 (2008), 10.1016/j.nima.2008.04.014.

[6] L. L. Ruckman, G. S. Varner, and A. Wong, Nucl. Instrum. Meth. **A591**, 534 (2008), 10.1016/j.nima.2008.03.095.