## ***Verilog Lab Level 1.2***

Q1. 8x1 Multiplexer using 2*1 Multiplexer

Q2. 1x8 demultiplexer using 1*2 Demultiplexer.

Q3. 4x16 Decoder using 2x4.

Q4. 16x4 Encoder using 4x2.

Q5. n-to-$2^n$ decoder (Hint: using for loop)

Q6. Design a 8-to-3 Priority Encoder:

(a) using Casex

(b) using for loop

Q7. 4 - bit Ripple Carry Adder

Q8. N-bit Ripple Carry Adder (Generic ripple Carry Adder)

(a) using for loop

(b) using instantiation of 1-bit full adder (Hint: use generate construct)

(c) using arithmetic assignment statement

Q9. Adder- Subtractor circuit

Q10. Design a one-digit BCD adder.

Q11. Design following Code converters using verilog:

(a) Binary to Gray Converter

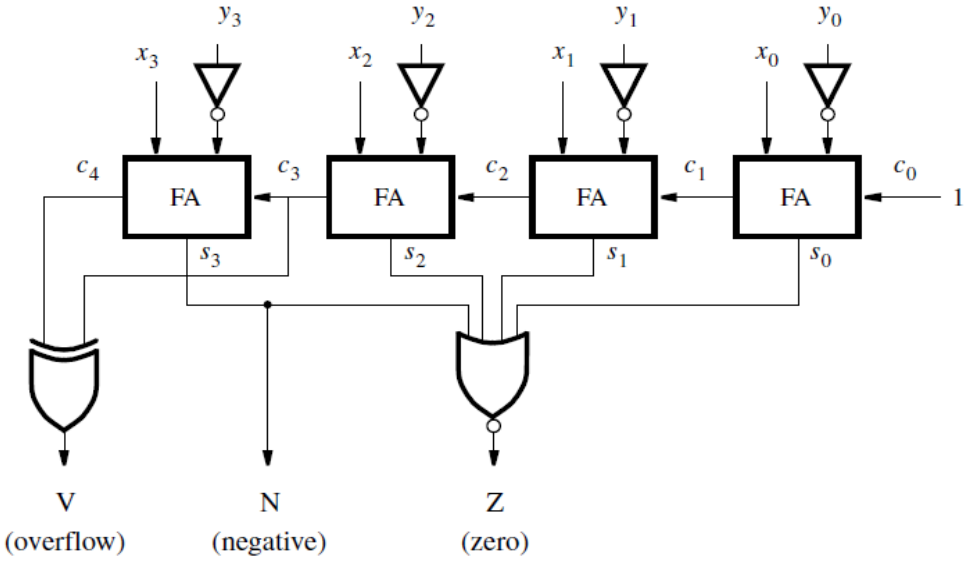
(b) Gray to Binary Converter

(c) BCD to seven segment converter

Q12. Parity Generator and Parity Checker

Q13. design a 4-bit comparator using relational operators.

Q14. Write verilog code to specify the 4-bit comparator circuit shown in following figure:




Q15. Design an 4-bit ALU which performs the following functions:

(a) Add (b) Subtract (c) XOR (D) OR (E) Invert (F)AND
(G) Multiplication (h) Division

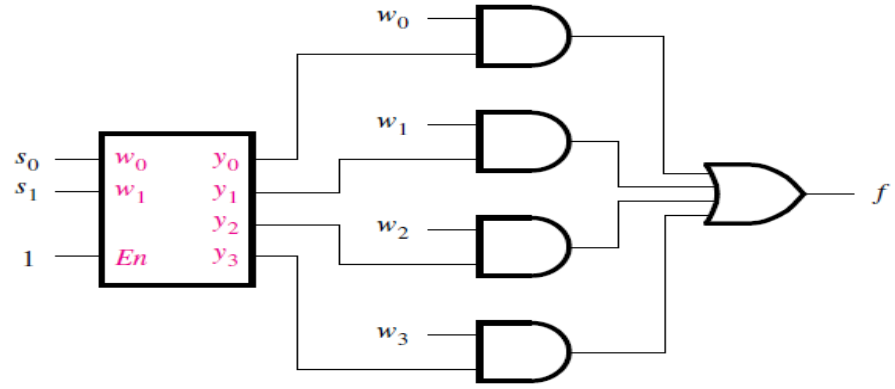
Q16. Design a 16*1 multiplexer using 4*1 with the following styles:

(a) using module instantiation

(b) using tasks

(c) using functions

Q17. Write verilog code that represents the following circuit. [Hint: use 2*4 decoder module as a subcircuit in your code]




Q18. Write Verilog code that represents the following shifter circuit: