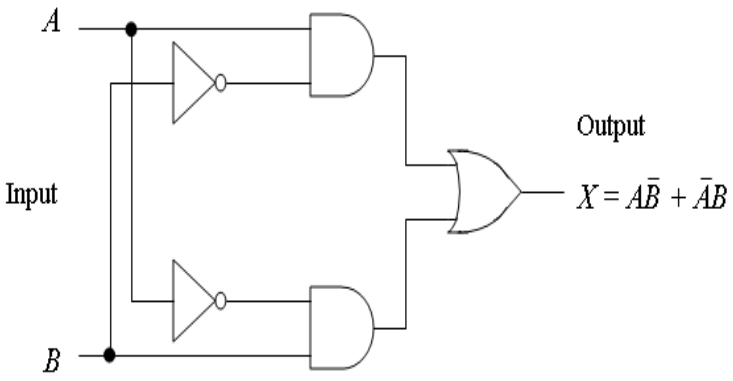
Verilog Lab Level 1.1

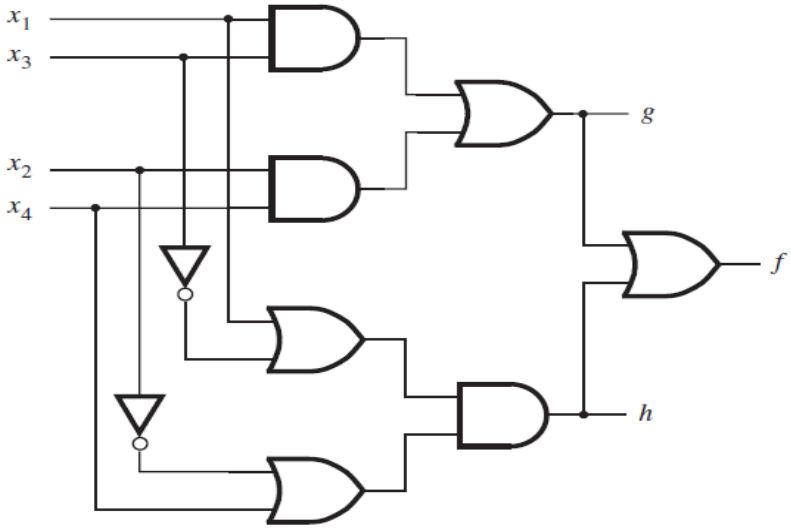
Design the following combinational circuits.

Q1. Write Verilog code for given circuits.

(a)



(b)



Q2. (a) Write Verilog code for given Equation F = x1x3' + x2x3' + x3'x4' + x1x2 + x1x4'

(b) Write Verilog code for given Equation F = (x1+x3').(x1+x2+x4').(x2+x3'+x4')

(c) Write verilog code to implement the function f(x1, x2, x3, x4) = ∑ m (0,1,2,4,5,7,8,9,11,12,14,15). Ensure that the resulting circuit is as simple as possible.

(d) Write verilog code to implement the function f(x1, x2, x3, x4) = ∑ m (1,4,7,14,15) + D(0,5,9). Ensure that the resulting circuit is as simple as possible.

(e) Write verilog code to implement the function f(x1, x2, x3, x4) = π M(6,8,9,12,13). Ensure that the resulting circuit is as simple as possible.

(f) Write verilog code to implement the function f(x1, x2, x3, x4) = π M (3, 11, 14) + D(0,2,10,12). Ensure that the resulting circuit is as simple as possible.

Q3. 4x1 Multiplexer

Q4. 1x4 Demultiplexer.

Q5. 3x8 Decoder.

Q6. 8x3 Encoder.

Q7. Design a 4*1 Multiplexer using conditional operator.

Q8. Half Adder.

Q9. Full Adder.

Q10. Half Subtractor.

Q11. Full Subtractor

Q12. Consider the following program:

```
module adder sign (X, Y, S, S2s);
        input [3:0] X, Y;
        output [7:0] S, S2s;
        assign S = X + Y,
                S2s = {{4{X[3]}}, X} + {{4{Y[3]}}, Y};
endmodule
```

(a) if X = 0011 and Y = 1101, What will be the value of S and S2s?

(b) What operation is assigned for S2s in the given program.