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DEVELOPMENT OF AN FPGA BASED LOW POWER MESSAGE DISPLAYING SYSTEM USING SCANNING TECHNIQUE

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ABSTRACT

Power efficient solution is essential for the portable electronic system. This paper presents an FPFA based embedded system for low power message display. Scanning technique is used to minimize the power. Experiment is conducted on 30 seven segments where an FPGA based intelligent controller scans all the display elements continuously at a certain speed to ensure only one display unit is on and other are off at a given time but human eye cannot detect it. Test result shows the significant reduction of power consumption over static display system.

Keywords— FPGA, Scanning, Message, Display, Low Power.

1. INTRODUCTION

Electronic display-we see it everywhere, in computers, watches, DVD players and many other electronic devices to display numeric and some alphabetic characters [1-3] [10-20]. It is also used for showing messages in digital calendars, billboards, shopping malls, airports, stadiums and many other places. It is a commonly used and efficient way of displaying information. Although electronic display is widely used, power consumption is still an important issue [4] [21-24]. In an electronic circuit, the major part of the total power is consumed by the display elements. If a large amount of display units are used in a system then the power requirement to run the system will also increase proportionately. In that case extra cooling arrangements may be required to keep the system workable. So the demands of low power consumption for FPGA systems are motivating new approaches to manage power dissipations issues. Researchers have proposed plasma screen or organic light-emitting devices (OLED) to reduce power consumption for display element [5- 6]. A microcontroller (μC) based system using scanning technique is proposed for low power message display [7]. A μC based system is usually burdened with the problem of limited number of pins, limited physical security and slow processing speed. Seven segment display with integrated controller and other circuitry are proposed to reduce the burden from main controller [8-9]. But in this case cost will be increased and power will be consumed by display control circuitry. Next section of this paper describes the scanning technique, algorithm, architecture and operation of the system and simulation result of the system.

2. SCANNING TECHNIQUE

This paper concentrates on the power dissipation issues for display devices. A scanning technique has been introduced in the proposed to minimize the power consumption for display elements. The objective is to connect all the display elements in parallel with each other and turning only one unit on at a time for a very short period and move to the next unit. If each unit can be illuminated periodically in a very short span of time the human eye will see the entire message as if all the units are turned on whereas only one unit is on at any given time.

Here seven segment displays are used as display units and as a test case a Muslim Calendar (displays Date, Time and Prayer times of Five Salah) is developed with 30 units of seven segment display. ULN is used to select the corresponding display unit. ULN is a very fast device to turn on and turn off of display units. As the algorithm for illuminating display units follow the scanning technique only one unit of seven segment display is turned on at any given time. So, theoretically the total power consumption for illuminating display units is reduced by 30 times. Hence 30 units of seven segment displays can be illuminated by only the power required by one unit.

3. ARCHITECTURE OF THE SYSTEM

The basic units of the proposed system can be divided into 7 parts: FPGA, Display elements, Display Decoder (CD4511BE), Real Time Clock (RTC), ULN (2803), Power Unit and Switches.

The outputs of the ULN are connected to the common cathodes of 30 seven segment displays. The output pins of the 7 segment decoder are connected in parallel to all seven segment displays. The FPGA sends appropriate input for

the decoder when corresponding seven segment display has logic 0 (through ULN) at its common cathode.

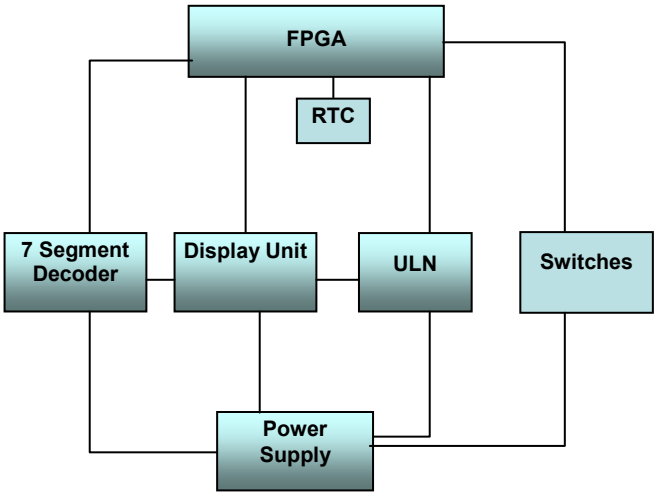

Fig 1 Block diagram of the system

A real time clock is used to keep the date and time. The FPGA reads time from the RTC each minute and changes the display clock and date accordingly. The prayer time table is loaded in the program memory of the FPGA as an array of structure. The prayer times change with the change of day and month field of the date. There is a battery connected to the RTC so that it can keep the time and date when the main power is not available. Three switches are used to set time and date. One switch is used to select which field of the time and date is to be changed. Other two switches are used to count up and count down the selected field. All these operation is controlled by the FPGA.

The main part of the system is the FLEX EPF10K70RC240-4 FPGA. All other components are connected to it and controlled by it. The four input pins of the seven segment decoder (CD4511BE) are connected to the first four pins of the FPGA. The input pins of the ULN are connected to the pins of FPGA. All output pins of ULN are connected to the common cathode pin of the 7 segment display sequentially. A 25.175MHz crystal oscillator is connected to the pin 91 of FLEX 10K FPGA.

4. OPERATION OF THE SYSTEM:

In the proposed system a controller scans all the display units continuously to ensure that only one unit is on at any given time. In this way power consumption will be much lower than that of existing static display system. Here a 'Muslim Calendar' containing date, time and prayer times for five salah has been developed as a test case. Seven segment displays are used as display units.

Here the FPGA controls the input of the ULN and Decoder. The FPGA initializes all the output pins of the ULN at level 1 (sends logic 1 thirty times in the input of the ULN), making all the seven segment displays to be turned off. At this point the FPGA sends logic 0 once and logic1 29 times so that each display receives the signal 0 sequentially while other displays receive signal 1. In this process, only one display is turned at a time and shifted sequentially.

5. SIMULATION:

The system is simulated using the Quartus II 7.0 simulator. The overall simulation is done using to the EPF10K70RC240-4 FPGA. It can be seen from the simulation that when one ULN passes signal low to the common cathode of a particular seven segment display at that time all other ULN passes the high signal to the common cathode of the others 7 segment display. When a seven segment display gets low signal in Common Cathode then it show the corresponding data passes by 7 segment decoder. Seven Segment decoder gets input from FPGA controller and passes to 7 segment display. Seven segment display is selected by ULN.

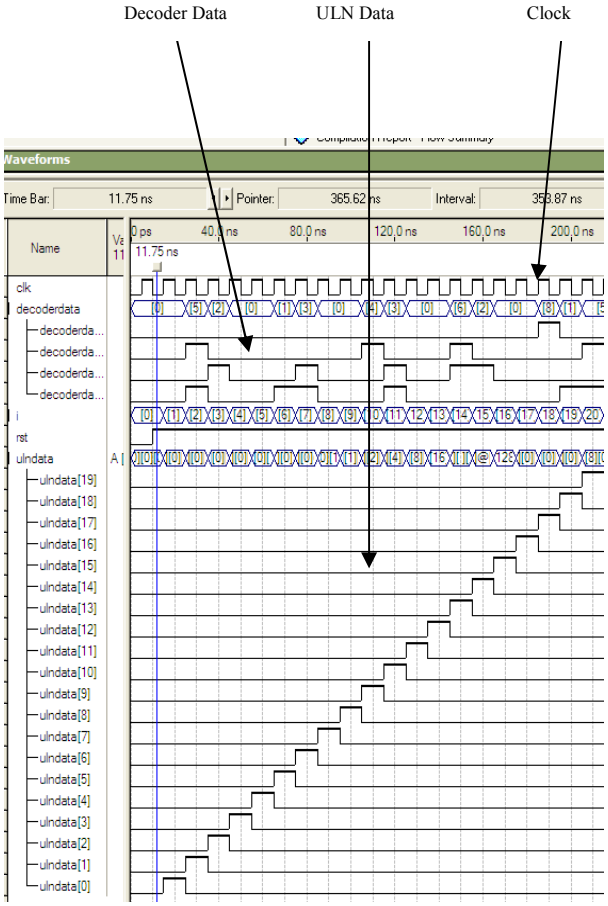

Fig 2 Simulation Result

Partial Test case result is shown below:

Fig 3 Test case result

In the above figure 3 there is a sample /partial test case result where 5 prayer time of Muslim calendar are displayed. It is possible to add more display unit on the board and can be controlled by using only one seven segment decoder and FPGA using scanning technique.

6. RESULT

Scanning technique is a power aware solution for message display. Here we have used 30 seven segment displays. But as scanning technique is applied, at any given time only one seven segment display is on. So, theoritically the system should consume $^{1}/_{30}$ times less power than it would take to make all the seven segment displays on at a time. But following table shows the practical senario.

Current and Power Consumption by the Display Elements are as follows. Agilent Technologies 0.56" (14.2 mm) seven segment display are used in the practical experiment.

Table 1

Current and power consumption

Current and Power Consumptin for 30 Units of Seven Segment Displays		
	With Scanning Technique	Without Scanning Technique
Current Consumption	18mA	75mA
Power Comsumption	0.09 watt	0.375 watt

So, in practical the power consumption is not as less as 30 times of the total power needed. But still it minimizes the power consumption to a considerable amount that is 76% less power is required to run the display units of the system when the scanning technique is applied.

The seven segment displays used as display units consume less power when scanning technique is used. Since the algorithm allows only one display unit to be illuminated at any given time rather than all the units receiving power, it consumes significant less power. The scanning technique in the corresponding circuit requires only one Display Decoder for all the display units.

7. CONCLUSION AND FUTURE WORKS

FPGA based embedded system implementing scanning technique can be used to design efficient low power message displaying system. It eliminates limitations of pins, offers higher processing speed and physical security over microcontroller based system. Simulation result shows the proper functionality of the system. The test result proves the significant improvement in power reduction. In future the modified scanning technique (clustering approach) can be incorporated in other FPGA systems with large number of display units. Future works can be done using those FPGAs.

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