

WM8731/L Audio CODEC Supported Sampling Rates

INTRODUCTION

To generate the required DAC and ADC sampling rates, the WM8731/L provides for two modes of operation Normal and USB Modes. These two modes are programmed under software control in the Sampling Control Register R8, according to Table 1.

In Normal mode, the user controls the sample rate by using an appropriate MCLK or crystal oscillator frequency and the sample rate control register setting. The WM8731/L can support sample rates from 8kHz up to 96kHz.

In USB mode, the user must use a fixed MCLK or crystal oscillator frequency of 12MHz to generate sample rates from 8kHz up to 96kHz. It is called USB mode since the common USB (Universal Serial Bus) clock runs at 12MHz and the WM8731/L Codec can be used directly in USB linked systems. The WM8731/L can generate the normal audio sample rates from this one 12MHz Master clock frequency, removing the need for different master clocks or PLL circuits.

Uniquely, the WM8731/L offers the user the ability to sample the ADC and DAC at different rates. Selecting these rates is by software control in both Normal and USB modes and reduces the burden on any controlling DSP. However, the signal processing in the ADC and DAC over-sampling filters are tightly coupled in order to minimize power consumption. To this end, only the combinations of sample rates listed in the following sections are supported. The rates supported are anticipated to be the likely combinations used in typical audio systems.

Note: The WM8731/L is not limited to the listed sample rates but using any other sample rate will negate the possibility of using mixed ADC and DAC sample rate combinations.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	
R8 (0001000) Sampling Control	0	USB/ NORMAL	0	Mode Select 1 = USB mode (250/272fs) 0 = Normal mode (256/384fs)	
	1	BOSR	0	Base Over-Sampling Rate	
				USB Mode 0 = 250fs 1 = 272fs	Normal Mode 96/88.2kHz 0 = 256fs 0 = 128fs 1 = 384fs 1 = 192fs
	5:2	SR[3:0]	0000	ADC and DAC sample rate control; See USB Mode and Normal Mode Sample Rate sections for operation	
	6	CLKIDIV2	0	Core Clock divider select 1 = Core Clock is MCLK divided by 2 0 = Core Clock is MCLK	

Table 1 Sample Rate Control Register

NORMAL MODE SAMPLE RATES

The Normal Mode sample rates are those usually expected when using standard 256fs and 384fs MCLK rates. However, the WM8731/L is also capable of being clocked from a 128fs or 192fs source but with limitations on the sample rates available. The device is also capable of being clocked by a 512fs or 768fs source, which requires an extra software setting on bit 6 of Register 8.

In Normal Mode, MCLK or the crystal oscillator is set up according to the desired sample rates of the ADC and DAC.

In Normal mode for ADC or DAC sampling rates of 8, 32, 48 or 96kHz, MCLK frequencies of either 12.288MHz (256fs/128fs) or 18.432MHz (384fs/192fs) can be used, Table 2.

In Normal mode for ADC or DAC sampling rates of 8, 44.1 or 88.2kHz, MCLK frequencies of either 11.2896MHz (256fs/128fs) or 16.9344MHz (384fs/192fs) can be used, Table 2.

Table 2 below should be used to set up the device to operate correctly with the various sample rate combinations. In normal mode, for ADC and DAC sample rates of 48kHz and 48kHz respectively, a 12.288MHz MCLK should be used and the device programmed with BOSR = 0, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0. For an 18.432MHz MCLK the device should be programmed with BOSR = 1, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0.

Dependent upon sample rate chosen, the ADC and DAC will operate with a Digital Filter of either, type 1 or type 2. Explanation of the digital filters available can be found Digital Filter Characteristics section in the datasheet.

SAMPLING RATE		MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS					DIGITAL FILTER TYPE
ADC	DAC		BOSR	SR3	SR2	SR1	SR0	
kHz	kHz	MHz						
48	48	12.288	0 (256fs)	0	0	0	0	1
		18.432	1 (384fs)	0	0	0	0	
48	8	12.288	0 (256fs)	0	0	0	1	1
		18.432	1 (384fs)	0	0	0	1	
8	48	12.288	0 (256fs)	0	0	1	0	1
		18.432	1 (384fs)	0	0	1	0	
8	8	12.288	0 (256fs)	0	0	1	1	1
		18.432	1 (384fs)	0	0	1	1	
32	32	12.288	0 (256fs)	0	1	1	0	1
		18.432	1 (384fs)	0	1	1	0	
96	96	12.288	0 (128fs)	0	1	1	1	2
		18.432	1 (192fs)	0	1	1	1	
44.1	44.1	11.2896	0 (256fs)	1	0	0	0	1
		16.9344	1 (384fs)	1	0	0	0	
44.1	8 (Note 1)	11.2896	0 (256fs)	1	0	0	1	1
		16.9344	1 (384fs)	1	0	0	1	
8 (Note 1)	44.1	11.2896	0 (256fs)	1	0	1	0	1
		16.9344	1 (384fs)	1	0	1	0	
8 (Note 1)	8	11.2896	0 (256fs)	1	0	1	1	1
		16.9344	1 (384fs)	1	0	1	1	
88.2	88.2	11.2896	0 (128fs)	1	1	1	1	2
		16.9344	1 (192fs)	1	1	1	1	

Table 2 Normal Mode Sample Rate Look-up Table

Notes:

- 8k not exact, actual = 8.018kHz
- All other combinations of BOSR and SR[3:0] that are not in the truth table are invalid

The BOSR bit represents the base over-sampling rate. The WM8731/L digital signal processing is carried out at this rate. In Normal mode, with BOSR = 0, the base over-sampling rate is at 256fs or 128fs, with BOSR = 1, the base over-sampling rate is at 384fs or 192fs. This can be used to determine the actual audio data rate produced by the ADC and required by the DAC.

128/192FS NORMAL MODE

For MCLK rates of 128fs or 192fs, only sampling rates of 44.1kHz and 48kHz can be generated, Table 3. These lower MCLK rates are the same as the 256fs or 384fs Normal mode settings for 96kHz and 88.2kHz, but run at half speed.

SAMPLING RATE		MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS					DIGITAL FILTER TYPE
ADC	DAC		BOSR	SR3	SR2	SR1	SR0	
kHz	kHz	MHz						
48	48	6.144	0	0	1	1	1	2
		9.216	1	0	1	1	1	
44.1	44.1	5.6448	0	1	1	1	1	2
		8.4672	1	1	1	1	1	

Table 3 Normal Mode 128fs/192fs Sample Rate Look-up Table

512/768FS NORMAL MODE

MCLK rates of 512fs and 768fs can also be accommodated by using the CLKIDIV2 bit (Register 8, bit 6). The core clock to the DSP will be divided by 2 so external 512fs or 768fs MCLK will scale to 256fs or 384fs internally. The device otherwise operates as in Table 2 but with MCLK at twice the specified rate. See Table 1 for software control.

NORMAL MODE SETTINGS EXAMPLES

Example scenarios are:

1. With a requirement that the ADC data rate is 8kHz and DAC data rate is 48kHz and choosing MCLK = 12.288MHz, the device is programmed with BOSR = 0 (256fs), SR3 = 0, SR2 = 0, SR1 = 1, SR0 = 0. The ADC output data rate will then be exactly 8kHz (derived from 12.288MHz/256 x 1/6) and the DAC expects data at exactly 48kHz (derived from 12.288MHz/256)
2. With a requirement that ADC data rate is 8kHz and DAC data rate is 44.1kHz, and choosing MCLK = 16.9344MHz, the device is programmed with BOSR = 1 (384fs), SR3 = 1, SR2 = 0, SR1 = 1, SR0 = 0. The ADC will not output data at exactly 8.000kHz, instead it will be 8.018kHz (derived from 16.9344MHz/384 x 2/11), the DAC is still at exactly 44.1kHz (derived from 16.9344MHz/384). A slight (sub 0.5%) pitch shift will therefore result in the 8kHz audio data. The user **must** therefore ensure that the data across the digital interface is correctly synchronized at the 8.018kHz rate.

SAMPLE RATE VARIATIONS

As demonstrated in the scenarios above, the exact sample rates desired cannot always be achieved. Comparison of the target sample rates and those actually produced are defined in Table 4 below.

TARGET SAMPLING RATE	ACTUAL SAMPLING RATE			
	BOSR=0 (256fs)		BOSR=1 (384fs)	
	MCLK=12.288	MCLK=11.2896	MCLK=18.432	MCLK=16.9344
kHz	kHz	kHz	kHz	kHz
8	8 $(12.288\text{MHz}/256) \times 1/6$	8.018 $(11.2896\text{MHz}/256) \times 2/11$	8 $(18.432\text{MHz}/384) \times 1/6$	8.018 $(16.9344\text{MHz}/384) \times 2/11$
32	32 $(12.288\text{MHz}/256) \times 2/3$	not available	32 $(18.432\text{MHz}/384) \times 2/3$	not available
44.1	not available	44.1 $11.2896\text{MHz}/256$	not available	44.1 $16.9344\text{MHz}/384$
48	48 $12.288\text{MHz}/256$	not available	48 $18.432\text{MHz}/384$	not available
88.2	not available	88.2 $(11.2896\text{MHz}/256) \times 2$	not available	88.2 $(16.9344\text{MHz}/384) \times 2$
96	96 $(12.288\text{MHz}/256) \times 2$	not available	96 $(18.432\text{MHz}/384) \times 2$	not available

Table 4 Normal Mode Actual Sample Rates

USB MODE SAMPLE RATES

In USB mode, the MCLK/crystal oscillator input is 12MHz only.

SAMPLING RATE		MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS					DIGITAL FILTER TYPE
ADC	DAC		BOSR	SR3	SR2	SR1	SR0	
kHz	kHz	MHz						
48	48	12.000	0	0	0	0	0	0
44.1 (Note 2)	44.1 (Note 2)	12.000	1	1	0	0	0	1
48	8	12.000	0	0	0	0	1	0
44.1 (Note 2)	8 (Note 1)	12.000	1	1	0	0	1	1
8	48	12.000	0	0	0	1	0	0
8 (Note 1)	44.1 (Note 2)	12.000	1	1	0	1	0	1
8	8	12.000	0	0	0	1	1	0
8 (Note 1)	8 (Note 1)	12.000	1	1	0	1	1	1
32	32	12.000	0	0	1	1	0	0
96	96	12.000	0	0	1	1	1	3
88.2 (Note 3)	88.2 (Note 3)	12.000	1	1	1	1	1	2

Table 5 USB Mode Sample Rate Look-up Table

Notes:

1. 8k not exact, actual = 8.021kHz
2. 44.1k not exact, actual = 44.118kHz
3. 88.2k not exact, actual = 88.235kHz
4. All other combinations of BOSR and SR[3:0] that are not in the truth table are invalid

Table 5 above can be used to set up the device to work with various sample rate combinations. For example, in USB mode with the ADC and DAC sample rates at 48kHz and 48kHz respectively, then the device should be programmed with BOSR = 0, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0.

Dependent upon sample rate chosen, the ADC and DAC will operate with a digital filter of types 0-3. Explanation of the digital filters available can be found in Digital Filter Characteristics section in the datasheet.

The BOSR bit represents the base over-sampling rate. The WM8731/L digital signal processing is carried out at this rate and the sampling rate will always be a sub-multiple of this at this rate. In USB mode, with BOSR = 0, the base over-sampling rate is defined at 250fs, with BOSR = 1, the base over-sampling rate is defined at 272fs. This can be used to determine the actual audio sampling rate produced by the ADC and required by the DAC.

USB MODE SETTINGS EXAMPLES

Example scenarios are:

1. With a requirement that the ADC data sampling rate is 8kHz and DAC data sampling rate is 48kHz the device is programmed with BOSR = 0 (250fs), SR3 = 0, SR2 = 0, SR1 = 1, SR0 = 0. The ADC will then be exactly 8kHz (derived from 12MHz/250 x 1/6) and the DAC expects data at exactly 48kHz (derived from 12MHz/250).
2. With a requirement that ADC data rate is 8kHz and DAC data rate is 44.1kHz the device is programmed with BOSR = 1 (272fs), SR3 = 1, SR2 = 0, SR1 = 1, SR0 = 0. The ADC will not output data at exactly 8kHz, instead it will be 8.021kHz (derived from 12MHz/272 x 2/11) and the DAC at 44.118kHz (derived from 12MHz/272). A slight (sub 0.5%) pitch shift will therefore result in the 8kHz and 44.1kHz audio data. The user **must** ensure that the data across the digital interface is correctly synchronized at the 8.021kHz and 44.118kHz rates.

SAMPLE RATE VARIATIONS

As demonstrated in the scenarios above, the exact sample rates desired cannot always be achieved. Comparison of the target sample rates and those actually produced are defined in Table 6 below.

TARGET SAMPLING RATE	ACTUAL SAMPLING RATE	
	BOSR=0 (250fs)	BOSR=1 (272fs)
kHz	kHz	kHz
8	8	8.021
	12MHz/(250 x 48/8)	12MHz/(272 x 11/2)
32	32	<i>not available</i>
	12MHz/(250 x 48/32)	
44.1	<i>not available</i>	44.118
		12MHz/272
48	48	<i>not available</i>
	12MHz/250	
88.2	<i>not available</i>	88.235
		12MHz/136
96	96	<i>not available</i>
	12MHz/125	

Table 6 USB Mode Actual Sample Rates

ADVANCED SAMPLE RATE SELECTION

It is also possible to support other sample rate selections using the WM8731 that have not been previously described above. This flexibility is possible by some inventive application of MCLK frequencies, the CLKDIV2 bit and the BOSR bits.

CLKDIV2

This bit allows the halving of the MCLK frequency internally by setting Bit 6 in Register 8, examples 1 and 3 below.

EXTERNAL MCLK DIVISION

It is also permissible to divide the external MCLK source by an integer multiple to scale the digital interface clocking rates. By dividing down the external MCLK it is possible to reduce the BCLK and LRCLK by the same multiple, example 2 below.

EXAMPLES

The selection of more unusual sampling frequencies is best demonstrated by example. Examples 1 and 2 describe how to select 22.050kHz by two different methods. Examples 3 and 4 describe how to select 11.025kHz by two different methods

1. 22.050kHz - Using table 2 it can be seen that halving the MCLK rate will half the sample frequency when set to the 44.1kHz settings. Use an 11.2896MHz MCLK and set the CLKDIV2 bit (R8; B6) to '1'. The BOSR bit (R8; B1) should be set to '0' and the SR[3:0] bits (R8; B5-2) should be set to 1000 (44.1kHz settings in Table 2).

SAMPLING RATE	MCLK	BOSR	SR	CLKDIV2
kHz	MHz	Bit	Bit	Bit
22.050	11.2896	0	1000	1

Table 7 Advanced Settings Example 1

2. 22.050kHz - Using an MCLK of 22.5792MHz divide this externally by 4 and set the BOSR; SR[3:0] bits to 01000 (44.1kHz settings in Table 2).

SAMPLING RATE	MCLK	BOSR	SR	CLKDIV2
kHz	MHz	Bit	Bit	Bit
22.050	22.5792 / 4	0	1000	0

Table 8 Advanced Settings Example 2

3. 11.025kHz - Using table 2 it can be seen that dividing the MCLK rate by 4 will divide the sample frequency by 4 when set to the 44.1kHz settings. Using a 5.6448MHz MCLK set the CLKDIV2 bit (R8; B6) to '1'. The BOSR bit (R8; B1) should be set to '0' and the SR[3:0] bits (R8; B5-2) should be set to 1000 (44.1kHz settings in Table 2).

SAMPLING RATE	MCLK	BOSR	SR	CLKDIV2
kHz	MHz	Bit	Bit	Bit
11.025	5.6448	0	1000	1

Table 7 Advanced Settings Example 3

4. 11.025kHz - Using an MCLK of 2.8224MHz set the CLKDIV2 bit to '0' and the BOSR; SR[3:0] bits to 01000 (44.1kHz settings in Table 2). This example of simply choosing a lower frequency oscillator as the source of the MCLK is the easiest solution to selecting alternative sample rates, but this is often not a suitable solution as it is usually preferable to employ clocks already available.

SAMPLING RATE	MCLK	BOSR	SR	CLKDIV2
kHz	MHz	Bit	Bit	Bit
11.025	2.8224	0	1000	0

Table 7 Advanced Settings Example 4

The above suggestions are based on an MCLK:Sample Rate (fs) ratio of 256. The MCLK rate will scale depending on the sample rate required and ratio used. Other sample rate solutions are also possible and can be derived with a little thought from the device user.

APPLICATION SUPPORT

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