VLSI Design (EC2.201) : End-semester exam

Monsoon 2025, CVEST, IIIT Hyderabad (Instructor: Prof. Abhishek Srivastava)

Date : 1st December, 2025, Duration : 3 Hours, Max. Marks : 30

Instructions:

- Read paper carefully and clearly write your assumptions (if any)
- Use commonly represented transistor parameter notations wherever required
- You are allowed to use 2 A-4 sheets of own hand written notes (no photocopy or printed material)
- Calculators are allowed

1. (a) Draw the schematic for write operation of a 6T SRAM cell in a row×column memory array. Hint: Circuit will have following control signals: a column select (Col), row select (WL), read/write (W), data (D), precharge (PC). Explain the write operation in your circuit with proper sequence of the control signals. Comment on the sizing of transistors within the 6T cell for reliable operation. [5]

   (b) Consider the circuit shown in Fig. 1. It is given that at $t = 0$, $v_1 = v + x$, $v_2 = v - x$ and all transistors are in saturation. Derive the expression for the rate of change of the difference voltage (x) with respect to time considering saturation mode. From the obtained expression, comment on the functionality of the circuit. [3]

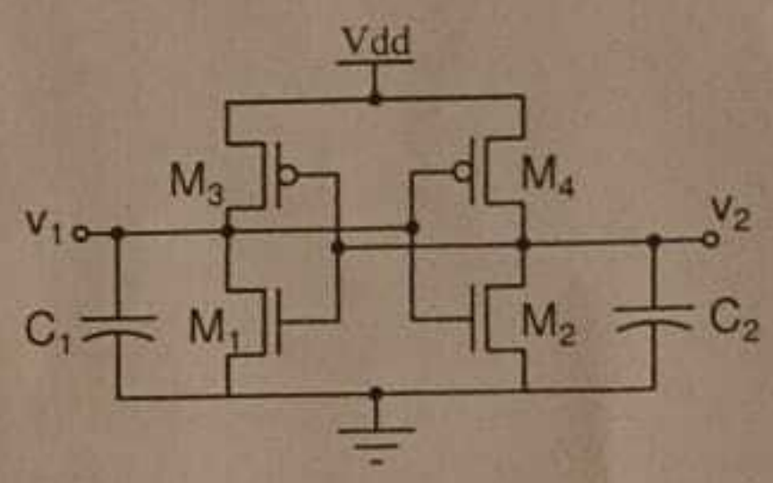

Figure 1

2. (a) Consider the circuit shown in Fig. 2(a). Re-draw the schematic in conventional style, separating all gates and with VDD on top and ground at the bottom. Describe the function and working of this circuit. For the input and clock waveforms given in Fig. 2(b), sketch the expected output showing the timing relationship with respect to the clock and the input (In). [4]

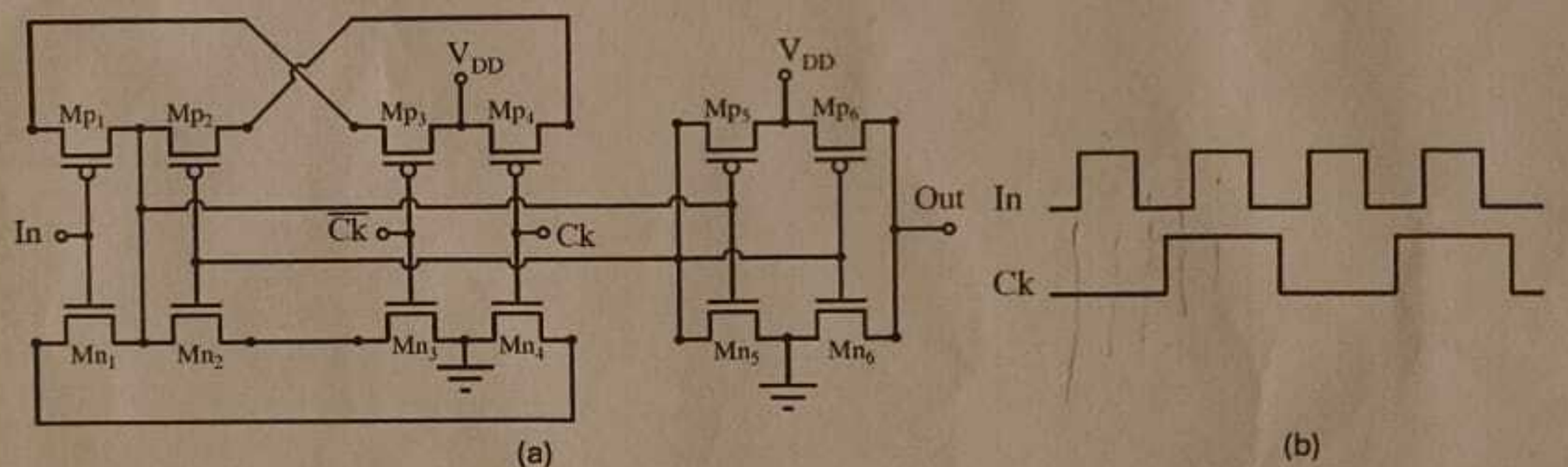

Figure 2

   (b) For a CMOS inverter, $K_p = K_n = 100\mu A/V^2$. For what input voltage is the static current drawn by the inverter maximum? What is the value of this maximum static current? Consider $V_{TN} = 0.35$V, $V_{TP} = -0.45$V and $VDD = 1.8$V. [3]

3. (a) For 1-bit full adder, the carry and sum bits can be defined as $C_{out} = A.B + Cin.(A + B)$ and $s = \overline{C_{out}}.(A + B + C_{in}) + A.B.C_{in}$, respectively. Prove that $Y = \overline{C_{out}} = \overline{A}.\overline{B} + \overline{C_{in}}.(\overline{A} + \overline{B})$. Give a static CMOS implementation of $Y = f\{A, B, C_{in}\}$. Also give static CMOS implementation of $C_{out} = f\{\overline{A}, \overline{B}, \overline{C_{in}}\}$, considering complement of the variables are also available. What is your observation from above two circuits? Discuss briefly. [3]

(b) The output carry in a Carry-Look-Ahead (CLA) adder can be quickly generated by pre-computing propagate (p_i) and generate (g_i) signals for each bit position (i), which are defined as $p_i = a_i \oplus b_i$ and $g_i = a_i.b_i$, respectively, where a_i and b_i are the input bits. The carry out ($c_{(i+1)}$) of the i^{th} bit position can be written as $c_{(i+1)} = (p_i.c_i) + g_i$ and thus, $c_{(i+1)}$ can be expressed entirely in terms of the p_i, g_i and c_0, and sum can be represented as $sum_i = p_i \oplus c_{i-1}$.

i. Since $c_{(i+1)} = (p_i.c_i) + g_i$, show that $p_i = a_i + b_i$ can be used instead of $p_i = a_i \oplus b_i$ (it will help to simplify the hardware implementation). Also give static implementation of $\overline{c_{(i+1)}} = f(a_i, b_i, c_i)$. [2]

ii. Since, $c_{(i+1)} = g_i + (p_i.c_i) = g_i + (p_i.g_{i-1} + p_i.p_{i-1}c_{i-1}) = ...$, the static implementation for the computation of carry term as a logic expression depending on all a_i, b_i and c_0 will incur significant delay and therefore it is rarely used. A faster way could be to use dynamic implementation. Consider the circuit shown in Fig.3. Find $\overline{c_{(i+1)}}$ for pre-charge phase ($clk = 0$) and evaluate phase ($clk = 1$). Can the circuit be used to implement the required logic ($c_{(i+1)} = (p_i.c_i) + g_i$) to pre-compute carry in CLA. Discuss briefly. [3]

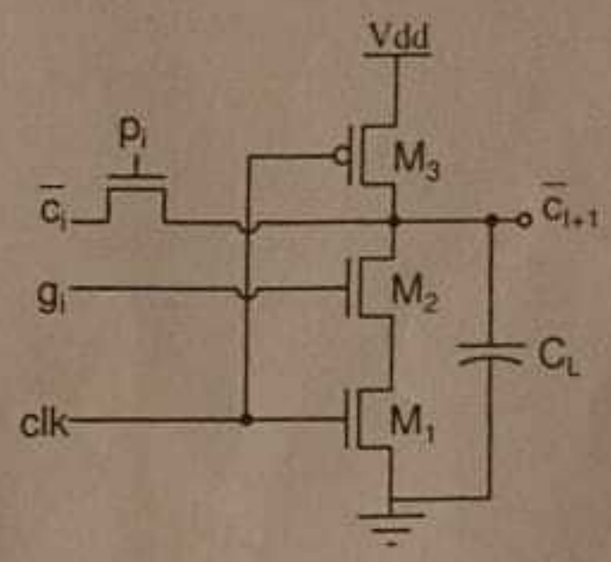

Figure 3

4. (a) Fig. 4 depicts a 4×16 decoder, where each input inverter drives 8 NAND inputs. The inverters at the input are minimum sized and each select output is loaded with capacitance equivalent to 128 minimum sized inverters. All transistors use minimum channel length. Consider a CMOS process with $\frac{\mu_n}{\mu_p} = 2.5$, The parasitic delay of gates may be taken to be proportional to the sum of the widths of transistors directly connected to the output terminal in a minimum sized gate. The parasitic delay of an inverter (ρ_{inv}) is 2τ, where τ propagation delay of a minimum sized inverter driving another minimum sized inverter without including the parasitic delay.

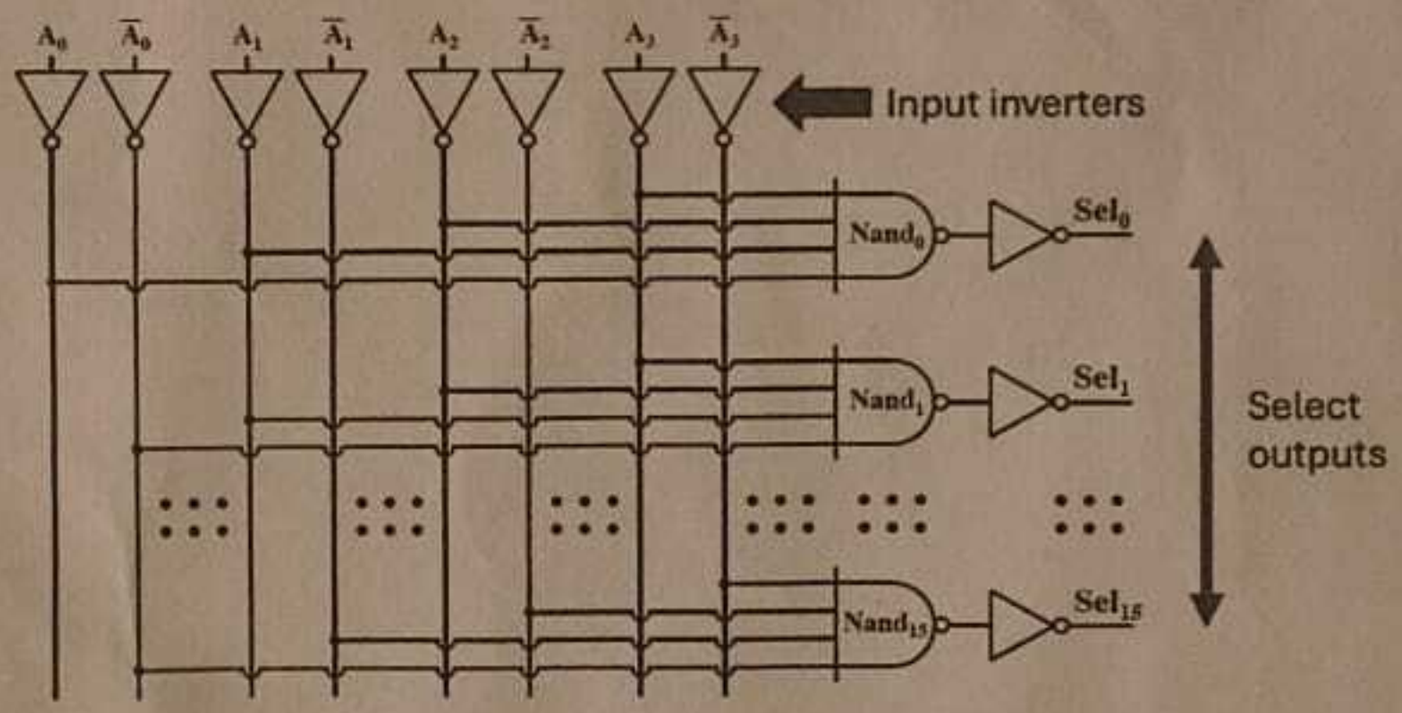

Figure 4

(b) Compute the logical effort and parasitic delay (in τ units) for all the gates in the circuit. [2]

(c) Find the widths for n and p channel transistors in all the gates of the circuit to minimize the total delay. (Give a table specifying the widths in units of the width of the n channel transistor in a minimum inverter). [4]

(d) Compute the total delay in units of τ for the circuit. [1]

Good luck !!