VLSI Design : Quiz-2

Monsoon 2025, IIIT Hyderabad (Instructor: Prof. Abhishek Srivastava)

Date : 28^{th} October, 2025, Duration : 1 Hour 15 Minutes, Max. Marks : 10

Instructions:

- Clearly write your assumptions (if any)
- You are allowed to use 1 A-4 sheets of own handwritten notes
- Calculator is allowed

1. (a) Use the 2×1 multiplexor (only) shown in Fig. 1 and implement the following logic function such that each input (x_1 to x_4) goes to gates of pass transistors. [2]

$$f = x_1x_2 + x_1x_3 + x_1x_4 + x_2x_3 + x_2x_4 + x_3x_4$$

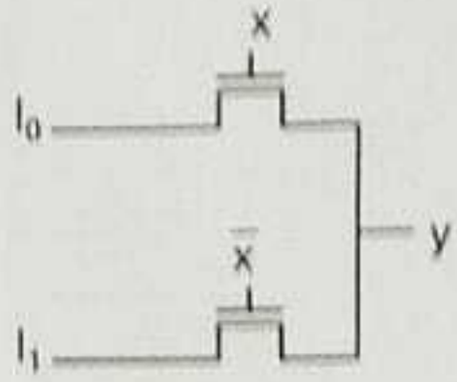

Figure 1

(b) Identify the optimal number of repeaters in the circuit to have maximum discharge chain length of 3 NMOS pass transistors. Also mention the locations of the repeaters in the circuit. [1]

2. Give an implementation of 4 input NAND and AND function using complementary pass transistor logic (CPL) based multiplexor discussed in class. Assume that complementary inputs (eg: A, $\bar{A}$) are also available. Discuss the disadvantages (if any) of your implementation. [2]

3. Consider the scenario shown in Fig. 2. Find the maximum delay (t_{pdmax}) and minimum delay (t_{pdmin}) of the combinational logic such that setup and hold time violations are avoided for the circuit. It is given that clock to propagation delay (t_{pcq}), setup time (t_{su}) and hold time (t_h) for D flip-flops are 5 ns, 4 ns and 2 ns, respectively. Clock period (T_{clk}) is 10 ns and the buffer delay (t_{skew}) is 5 ns. Clearly draw timing diagram and show your calculations. [3]

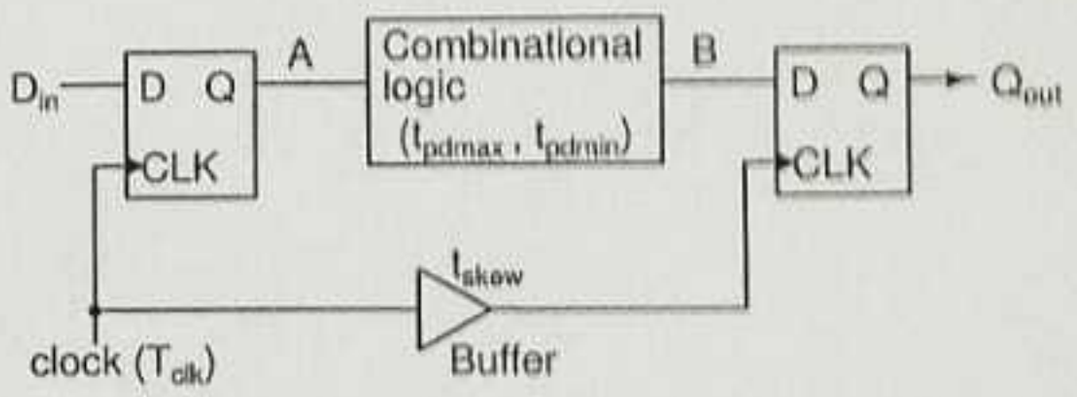

Figure 2

4. (a) Derive the functionality of the TSPC register shown in Fig. 3 *(Acknowledgement: Rabaey)*. [1]

(b) Discuss the hold and setup time for this circuit. [1]

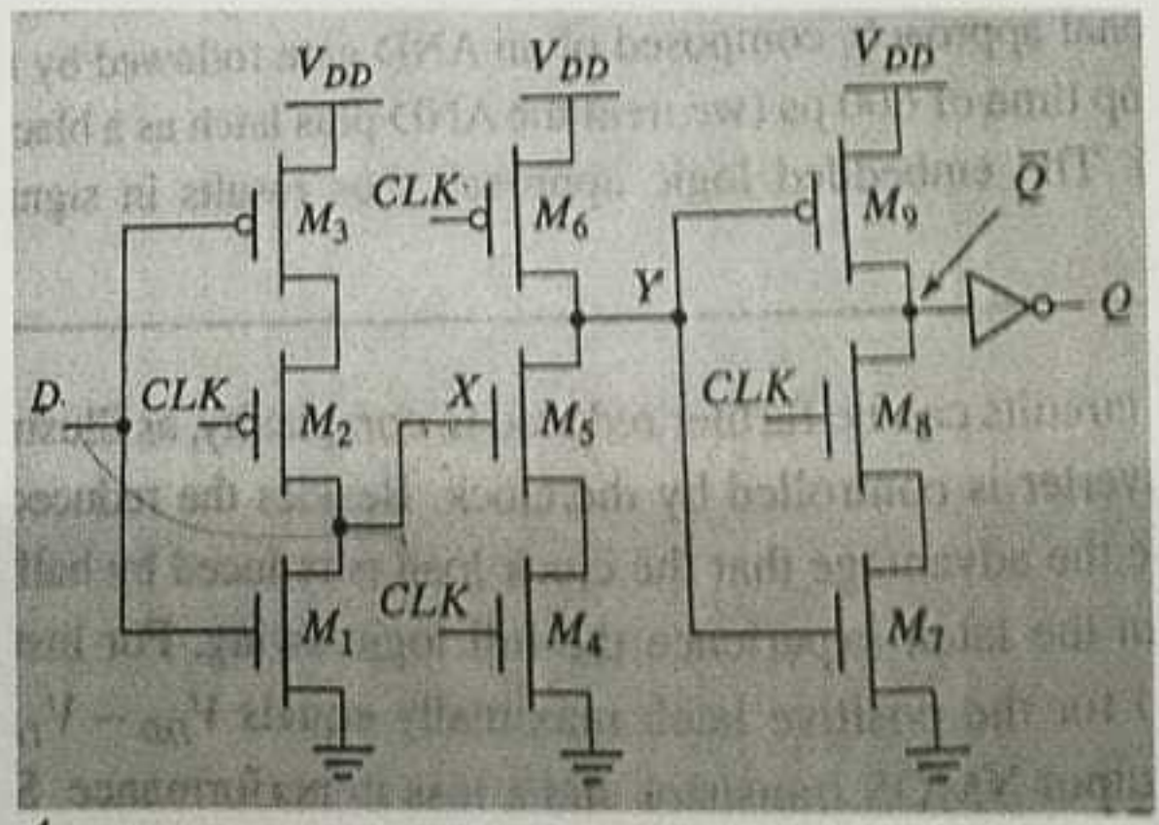

Figure 3