VLSI Design (EC2.201) : Mid-Semester Exam

Monsoon 2025, IIIT Hyderabad (Instructor: Prof. Abhishek Srivastava)

Date : 22^{nd} Sep, 2025, Duration : 1 hr 30 min, Max. Marks : 20

Instructions:

- Clearly write your assumptions (if any)
- Delay unit (τ) has the conventional meaning as discussed in lectures
- Students are allowed to use 1 A-4 sheets of own handwritten notes
- Use of calculator is allowed

1. Input capacitance (C_{in-inv}) and output parasitic capacitance C_{par}) of a CMOS inverter can be approximated by following expressions, where notations have usual meaning:

$$C_{in-inv} = C_{OX}W_NL_N + C_{GDOVN}W_N + C_{GSOVN}W_N + C_{OX}W_PL_P + C_{GDOVP}W_P + C_{GSOVP}W_P$$

$$C_{par} = C_{DBN} + C_{DBP} + 2C_{GDOVN}W_N + 2C_{GDOVP}W_P$$

It is given that $C_{G(D,S)OVN} = C_{G(D,S)OVP} = C_{OV} = 973\ aF/\mu m$, $C_{OX} = 8355\ aF/\mu m^2$, $(C_{DBN} + C_{DBP}) = 1fF$, $\mu_n/\mu_p = 2.5$ and $L_N = L_P = 0.18\mu m$. Consider that the inverter is designed to equalize the rise-fall times and noise margins. Inverter is driving a capacitive load $C_L = 50\ fF$.

   (a) Plot inverter-delay in τ units vs width of NMOS (W_N) for $W_N = \{1, 10, 100, 1000\}\mu m$. [4]

   (b) Discuss from your plot, what advantage or disadvantage you get in delay optimization by varying the width. [1]

2. You are asked to design a non-inverting buffer with optimal delay to drive an output capacitive load $C_L = 12\ pF$, while presenting input capacitance $C_{IN} \approx 12\ fF$. Assume $L_N = L_P = 0.18\ \mu m$ and $\rho_{inv} = 1$, where ρ_{inv} is the parasitic component of the inverter delay.

   (a) Write the delay expression for the entire chain in terms of stage effort (x), number of stages (N), ρ_{inv} and τ units. [1]

   (b) Find the number of stages and the final stage effort value for minimum delay and calculate corresponding delay in τ units. *(Hint:* $x_{next} = \frac{x_{initial}+\rho}{ln(x_{initial})}$*)* [2]

   (c) Find the sizes of all inverters (in μm) in the chain. Capacitance values and mobility ratio is same as given in Question 1 above. Solving that first will help. [2]

3. (a) Using static CMOS logic style, design a logic gate to implement the following function [2]

$$Y = \overline{A(B+C) + DE}$$

   (b) Considering $\frac{\mu_n}{\mu_p} = m$, size the gate to equalize its delay to that of a minimum size inverter (NMOS width is W) in the same technology node. [2]

   (c) Calculate logical effort for each input. [1]

4. Consider the circuit shown in Fig. 1.

   (a) Derive an expression for the time to charge a load capacitor C_L from 0V to an output voltage $V_{OH} >> |V_{TP}|$, when the input is LOW and the nMOS is OFF. The expression should be in terms of VDD, C_L, V_{OH} and V_{TP}. [3]

   (b) Consider $C_{OX} = 4.4 \times 10^{-7}F/cm2$, $\mu_n = 400cm^2/Vs$, $\mu_p = 190cm^2/Vs$, $V_{TP} = -0.65V$, $V_{TN} = 0.55V$ and $VDD = 3.3V$. What should be the aspect ratio of pMOS transistor (W_p/L_p) such that the circuit charges $C_L = 10fF$ from 0 to 3V in 50 ps when the input is LOW (and so the nMOS is OFF). [2]

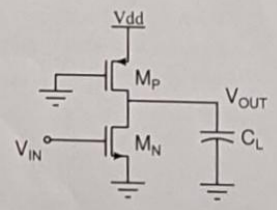

Figure 1

Good luck !!