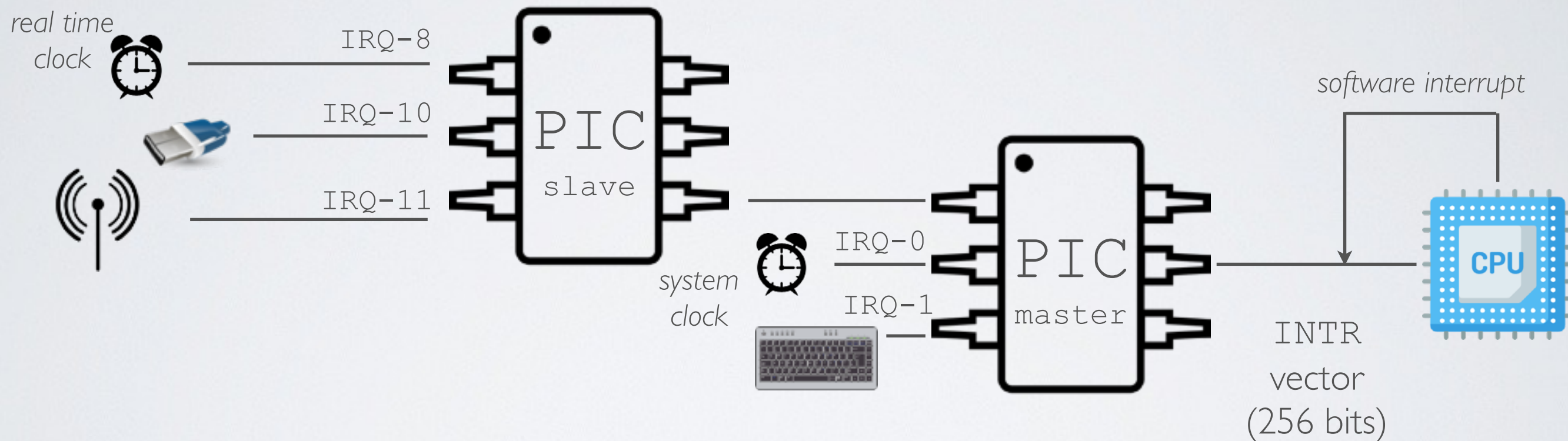


# Internal Interrupt and External Interrupt - the real implementation



➔ I/O devices have unique or shared IRQs that are managed by two **Programmable Interrupt Controllers** (PIC)

# Programmable Interrupt Controllers (PIC)

- ➔ Responsible to tell CPU when and which devices wishes to interrupt through the INTR vector
- ✓ 16 lines of interrupt (IRQ0 - IRQ15)
- ✓ Interrupts have different priority
- ✓ Interrupts can be masked