

國立中央大學八十八學年度碩士班研究生入學試題卷

所別：資訊工程研究所 不分組 科目： 計算機結構 共 / 頁 第 / 頁

- 1 (15%) Design a counter using 3 D-flip-flops that generates the following sequence: 0 → 1 → 2 → 4 → 6 → 0 ... If an unused state is given, your circuit should be able to adjust itself to enter one of the above states (i.e., 0, 1, 2, 4, 6) after some pulses.
- 2 (15%) Consider a 1Kx8 RAM chip (i.e., it has 1024 bytes).
 - a (3%) How many address lines and data lines are there in this chip?
 - b (4%) How many such chips do you need to construct a 16Kx16 memory?
 - c (4%) How many address lines and data lines are there in the 16Kx16 memory?
 - d (4%) What kind of decoder do you need to connect this 16Kx16 memory?
- 3 (25%) Answer the following questions about pipeline design.
 - a (10%) What are the three major kinds of pipeline hazards? Give one example for each of these hazards.
 - b (5%) What is the data forwarding technique? What kind of hazard can it solve?
 - c (5%) What is the branch prediction technique? What kind of hazard can it solve?
 - d (5%) Design a 2-bit branch predictor.
- 4 (15%) Consider a CPU with 5-stage pipeline (such as DLX) which runs the following assembly code:

```
LOAD R1, b  
LOAD R2, c  
ADD R3, R1, R2 /* R3 = R1 + R2; with a stall  
STORE a, R3  
LOAD R4, e  
LOAD R5, f  
ADD R6, R4, R5 /* R6 = R4 + R5; with a stall  
STORE d, R6
```

Suppose there are two stalls in the above program, each falling between an occurrence of adjacent LOAD and ADD instructions. Show how to reschedule the above code so that all stalls can be removed.

- 5 (15%) Answer the following questions about cache design:
 - a (5%) What are the 3 major categories for cache miss?
 - b (5%) Suppose we enlarge our cache block size. Which of the above cache misses can be reduced? Which of the above cache misses will increase?
 - c (5%) What is the victim cache technique?
- 6 解釋下列名詞：(每題 3 分，共 15 分)
 - a SIMD
 - b MIMD
 - c superscalar
 - d IEEE 754 for floating-point numbers
 - e memory hierarchy