1. (10%) In the hierarchical storage structure, the same data could appear in different levels of the storage system. A multiprocessor environment could even complicate the problems. Please explain the cache coherency problem in a multiprocessor environment. Should we solve it without considering any hardware issue? Explanation is needed.

2. (15%) Spin locking is a way to implement semaphores. Please use the concept of spin locking to implement the *wait* and *signal* operations of binary semaphores. You MUST ensure that no starvation and no deadlock could occur.

3. (10%) Free disk space can be kept track of using a free list or a bit map. Suppose that disk addresses require A bits.
   (a) For a disk with D blocks, F of which are free, state the condition under which the free list uses less space than the bit map.
   (b) For A having the value 32 bits, express your answer as a percentage of the disk space that must be free.

4. (15%) Consider the following page reference string:
   3, 2, 1, 4, 3, 2, 5, 3, 2, 3, 4, 1, 4, 3, 5, 3, 4, 2, 1, 2
   If FIFO replacement algorithm is used, show the states of memory at the times just after each memory references, and the number of page faults would occur for the following systems:
   (a) A system with 3 frames of memory.
   (b) A system with 4 frames of memory.
   (c) Show the working set of the system at the times just after each of the memory references, assuming the window size of the working set is 3.

5. (15%) A pipelined CPU executes instructions in either 3 or 4 clock cycles. In the first cycle of instruction execution, the CPU fetches the instruction. In the second cycle, the CPU decodes the instruction and reads the input operands from the registers. The execution of a simple instruction is completed in the third cycle, while the execution of a complicated instruction is completed in the fourth cycle. Discuss what types of data hazards could cause problems in instruction executions. Assume that internal forwarding (bypassing) hardware is incorporated to feedback the output of the ALU to its inputs.

6. (10%) A CPU implements a 2-level page table in its virtual memory system. Each of the first-level page tables contains 512 entries and each of the second-level page tables contains 1024 entries. Assume that the virtual address generated by the CPU contains 32 bits and one byte is the minimum unit of memory space addressable by the CPU. What is the size of a page in the virtual memory system?

7. (13%) 請說明 RAID 5 (redundant array of inexpensive disks) 的架構及其 read 、write 之方法。

8. (12%) 請討論 Snoopy Cache Coherence Protocol 及 Directory based Protocol 在 fat-tree 多重處理機架構中之優劣。