# DIGITAL ELECTRONICS LAB

# EXPERMINET – 4

*PULKIT PANDEY*

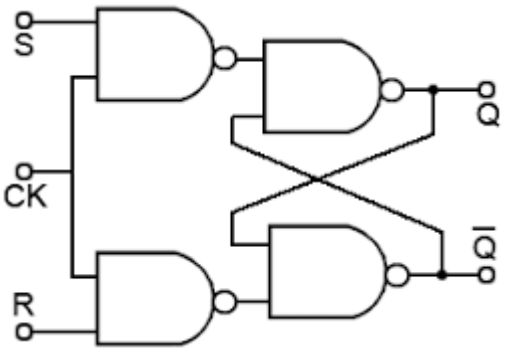
*2K19/EP/076*

**AIM:** To verify the truth tables for S-R, D and J-K Flip-Flops.

**THEORY:**

**S-R FLIP FLOP**

It is required to set or reset the memory cell in synchronism with a train of pulses known as a clock signal (CLK). Such a circuit is referred to as a clocked set reset (S-R) FLIP FLOP. The circuit responds to the input signal only if the clock signal is present. If Sn=Rn=0 and CLK is applied, the output at the end of the clock pulse is the same as output before the clock pulse i.e. Qn+1=Qn.

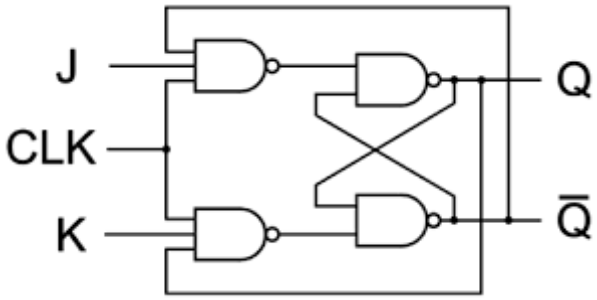



| S | R | CLK | Outputs $Q_{n+1}$ |
|---|---|---|---|
| 0 | 0 | ↑ | $Q_n$(No Change) |
| 0 | 1 | ↑ | 0 |
| 1 | 0 | ↑ | 1 |
| 1 | 1 | ↑ | ⋆(Race) |


K Map

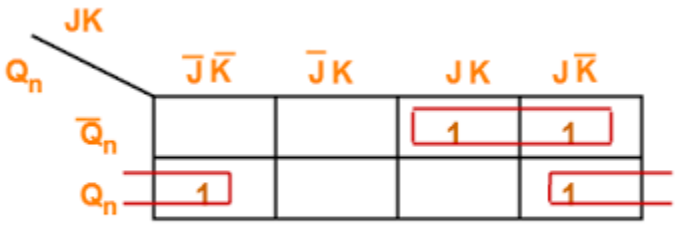
**J-K FLIP FLOP**

The uncertainty in the state of an S-R flip flop when Sn=Rn=1 can be eliminated by converting it into a J-K flip flop.




Truth Table

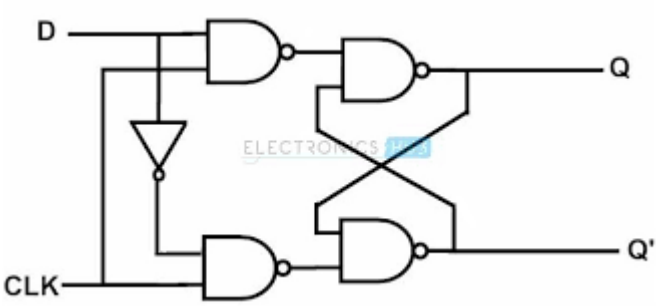
| J | K | CLK | Q |
|---|---|---|---|
| 0 | 0 | ↑ | $Q_0$ (no change) |
| 1 | 0 | ↑ | 1 |
| 0 | 1 | ↑ | 0 |
| 1 | 1 | ↑ | $\overline{Q}_0$ (toggles) |



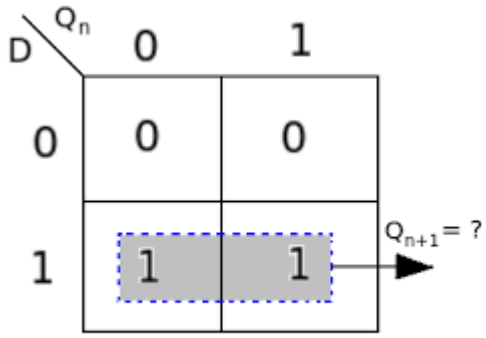

K Map

## D TYPE FLIP FLOP

The circuit diagram of D-type flip flop shows that it has only one input reference i.e. D-input or data input. Its truth table shows that the ouput Qn+1 at the end of the clock pulse equals the input Dn before the clock pulse.

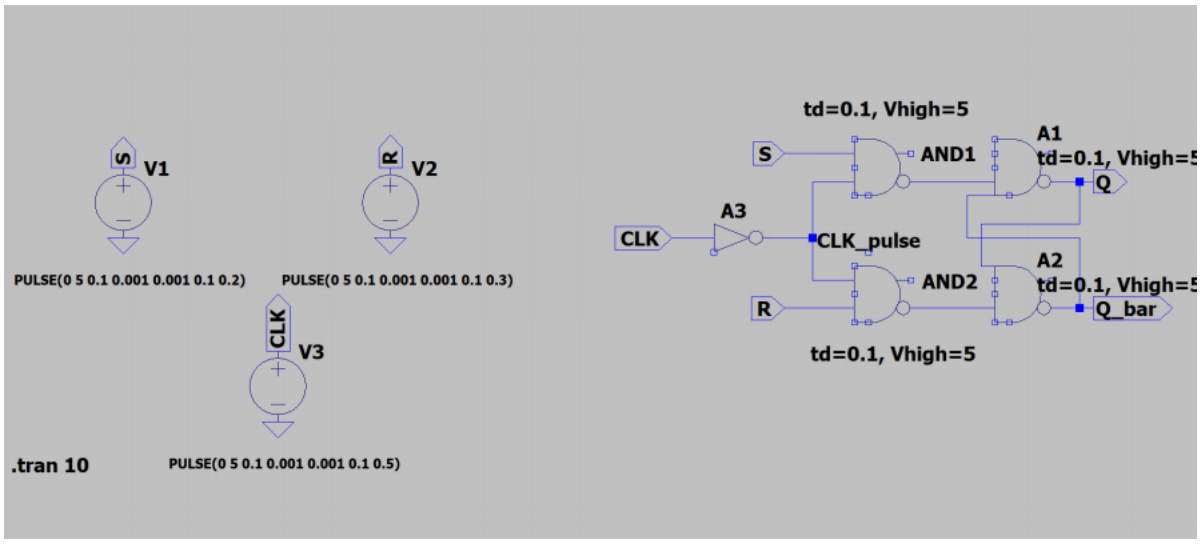


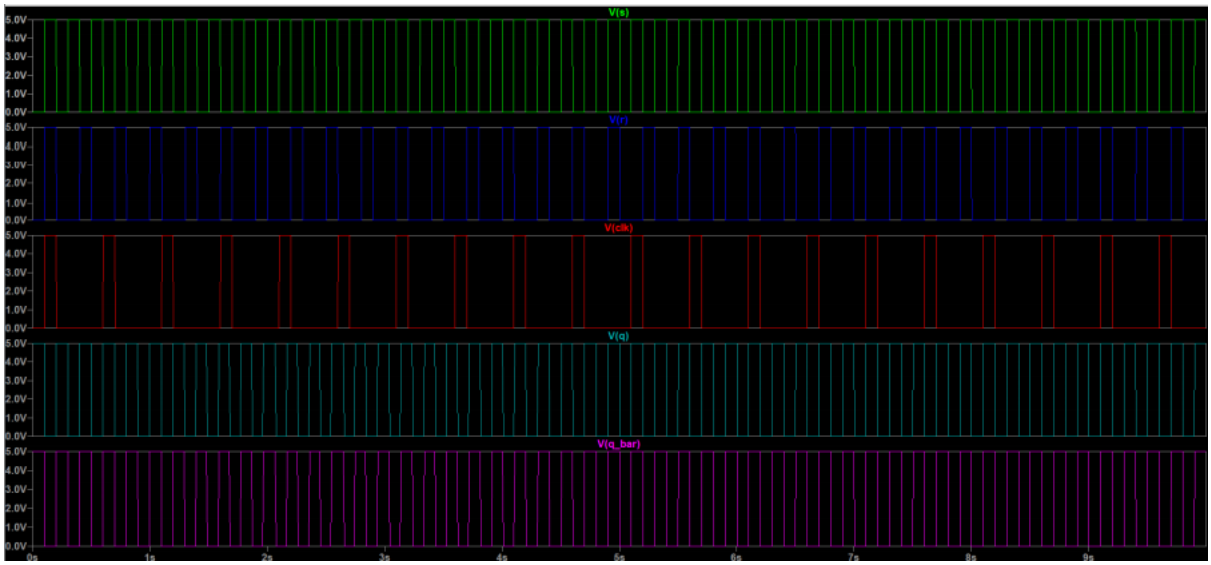

| Input $D_n$ | Output $Q_{n+1}$ |
|---|---|
| 0 | 0 |
| 1 | 1 |



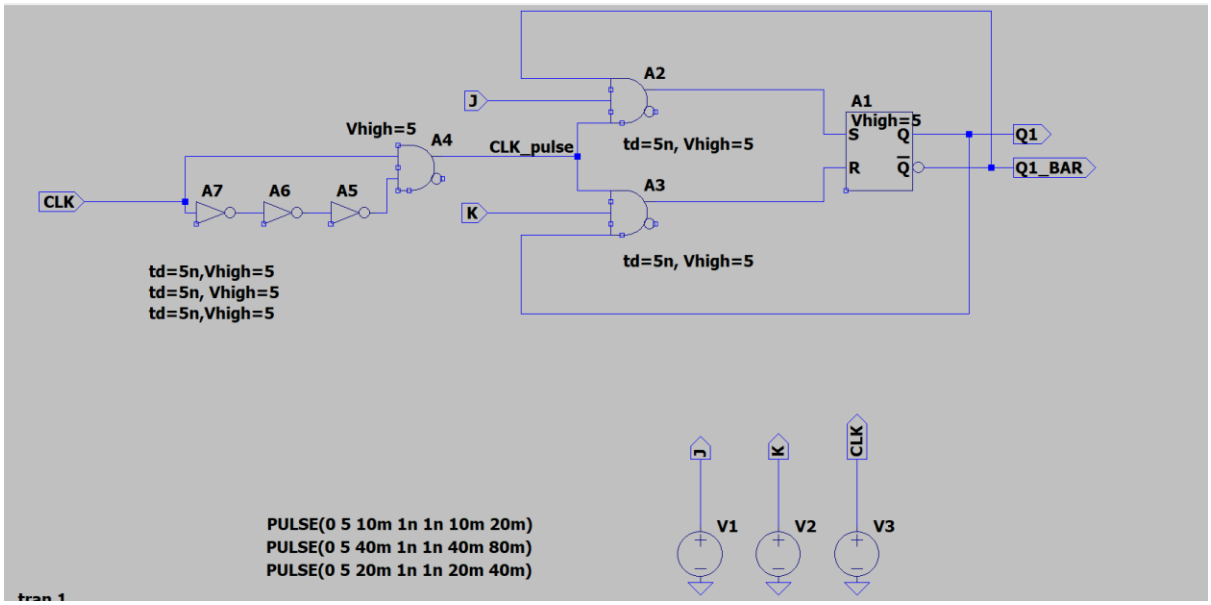

## SOFTWARE SIMULATIONS

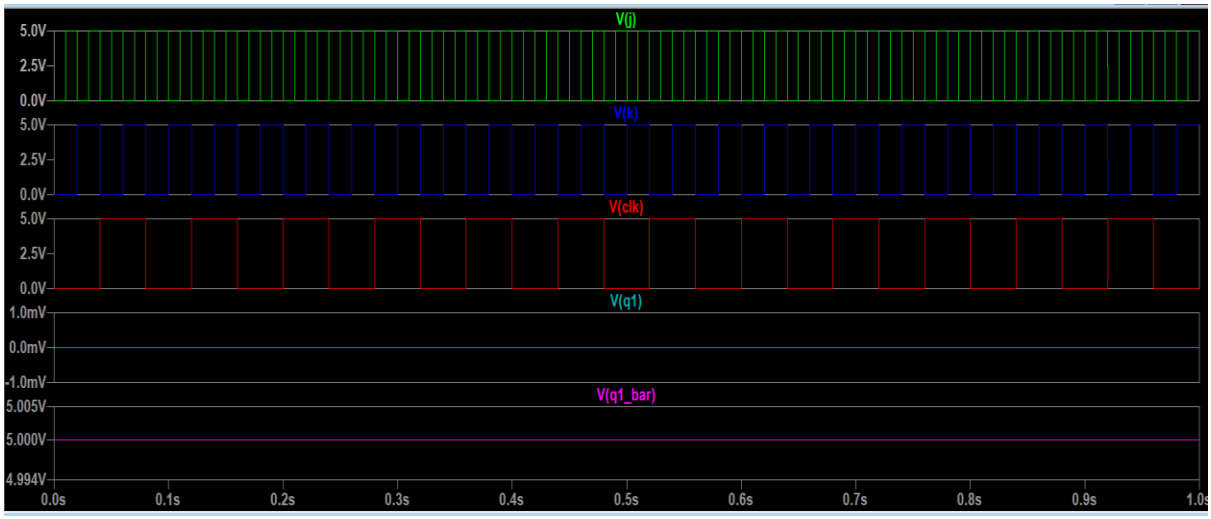
### S-R FLIP FLOP




V(s)
V(r)
V(clk)
V(q)
V(q_bar)

## J-K FLIP FLOP


J
K
CLK
A1
A2
A3
A4
A5
A6
A7
Vhigh=5
CLK_pulse
td=5n, Vhigh=5
td=5n, Vhigh=5
td=5n,Vhigh=5
td=5n, Vhigh=5
td=5n,Vhigh=5
S
R
Q
Q1
Q1_BAR
PULSE(0 5 10m 1n 1n 10m 20m)
PULSE(0 5 40m 1n 1n 40m 80m)
PULSE(0 5 20m 1n 1n 20m 40m)
V1
V2
V3
tran 1


V(j)
V(k)
V(clk)
V(q1)
V(q1_bar)
5.0V
2.5V
0.0V
1.0mV
0.0mV
-1.0mV
5.005V
5.000V
4.994V
0.0s
0.1s
0.2s
0.3s
0.4s
0.5s
0.6s
0.7s
0.8s
0.9s
1.0s

# D TYPE FLIP FLOP