

DIGITAL ELECTRONICS LAB

EXPERIMENT – 2

PULKIT PANDEY

2K19/EP/076

AIM: To verify the truth table of half adder and full adder.

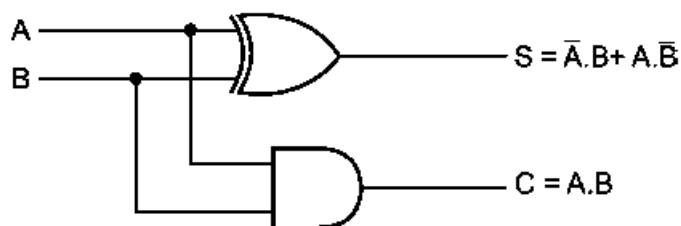
THEORY:

HALF ADDER: A half adder is an MSI circuit that adds two binary digits, giving a SUM bit and a CARRY bit as in the logic truth table. If A and B are the two input bits then SUM is the XOR of A & B:

$$\text{Sum} = AB' + A'B$$

Similarly CARRY is the AND of A & B:

$$\text{Carry} = A.B$$



Circuit Diagram: Half Adder

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth Table: Half Adder

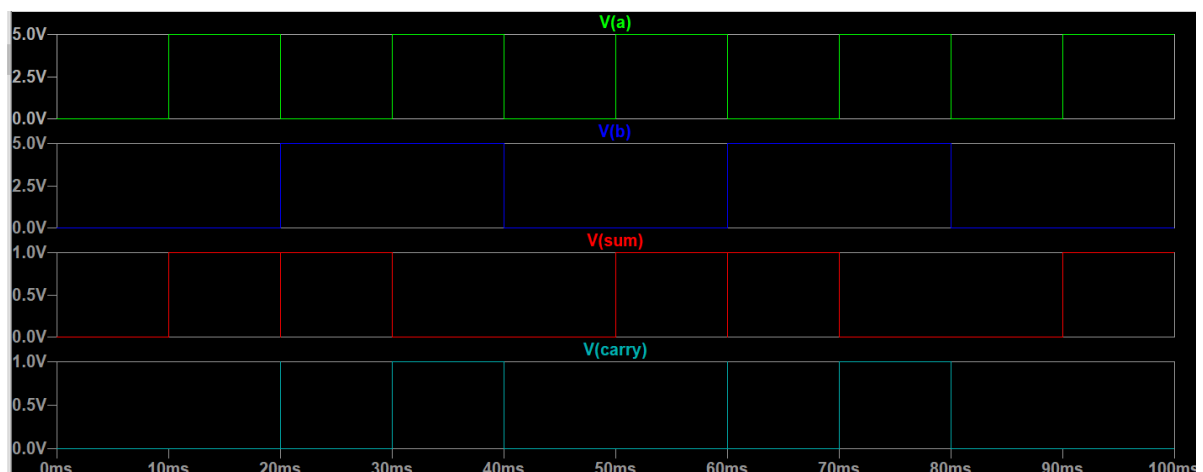
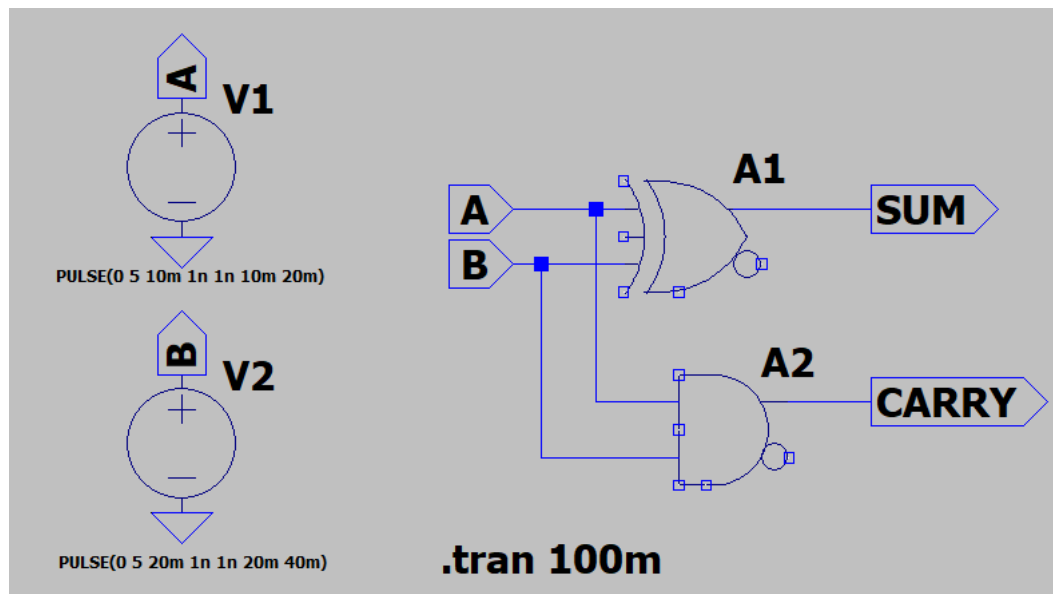
A \ B	0	1
0	0	1
1	2	1

K-map for Carry

A \ B	0	1
0	0	1
1	1	2

K-map for Sum

K-MAPS for half adder.



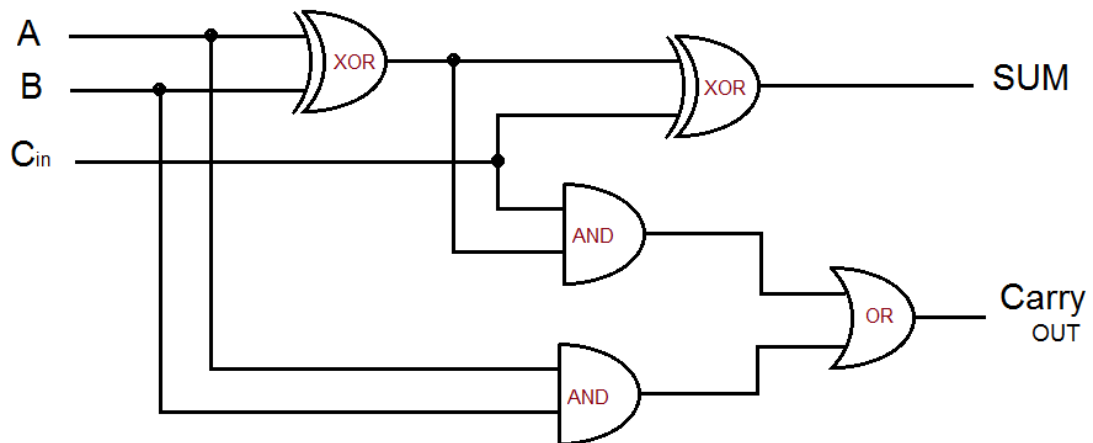
SIMULATION

FULL ADDER: A full adder is an MSI circuit that adds two input bits and carry from the previous stage and outputs a SUM bit and a CARRY OUT bit. A and B are the main bits, C is the carry from the previous stage. Sum produced is:

$$\text{Sum} = A'B'C + A'BC' + AB'C' + ABC$$

CARRY is the output carry bit and is:

$$\text{Carry} = AB + BC + AC$$



Circuit Diagram: Full Adder

INPUTS			OUTPUTS	
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table: Full Adder

A \ BC	BC			
	00	01	11	10
0	0	1	3	2
1	1	4	5	6

K-map for Sum (S)

A \ BC	BC			
	00	01	11	10
0	0	1	1	3
1	4	1	5	6

K-map for Carry (C_{out})

K-MAPS for full adder.

