DIGITAL ELECTRONICS

EXPERIMENT – 5

PULKIT PANDEY

2K19/EP/076

AIM: To verify the operation of Shift Registers: SISO, SIPO, PISO and PIPO

THEORY:

Flip flops can be used to store a single bit of binary data (1 or 0). However, in order to store multiple bits of data, we need multiple flip flops. A Register is a device which is used to store such information. It is a group of flip flops connected in series used to store multiple bits of data. The information stored within these registers can be transferred with the help of shift registers. Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses. The registers which will shift the bits to left are called “Shift left registers”. The registers which will shift the bits to right are called “Shift right registers”.

Shift registers are basically of 4 types:

1) Serial in Serial Out shift register

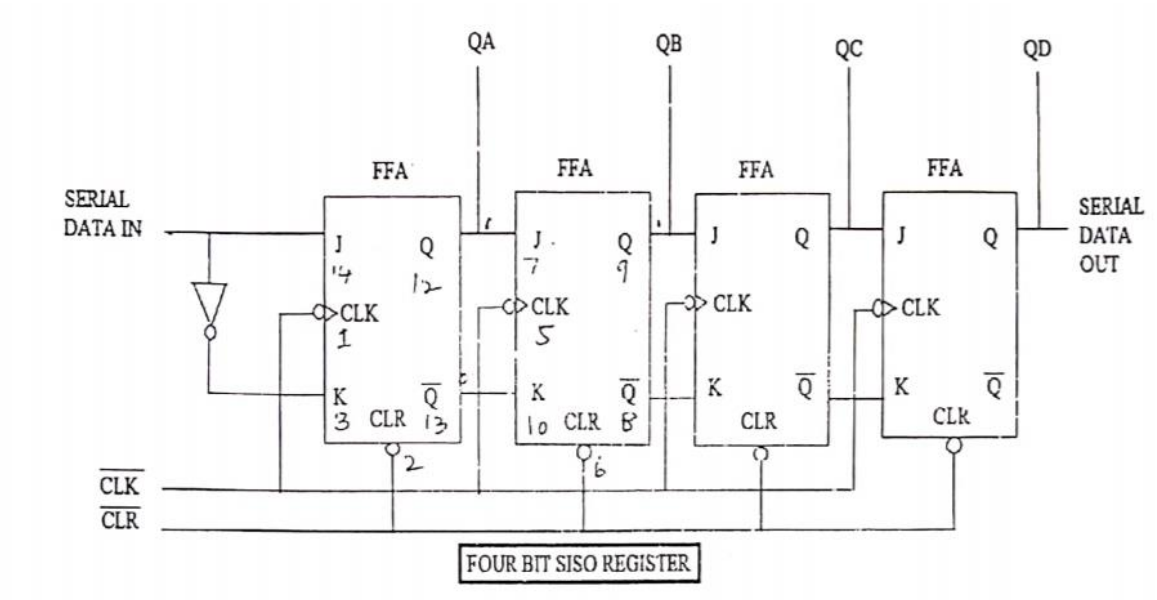
2) Serial in parallel Out shift register

3) Parallel in Serial Out shift register

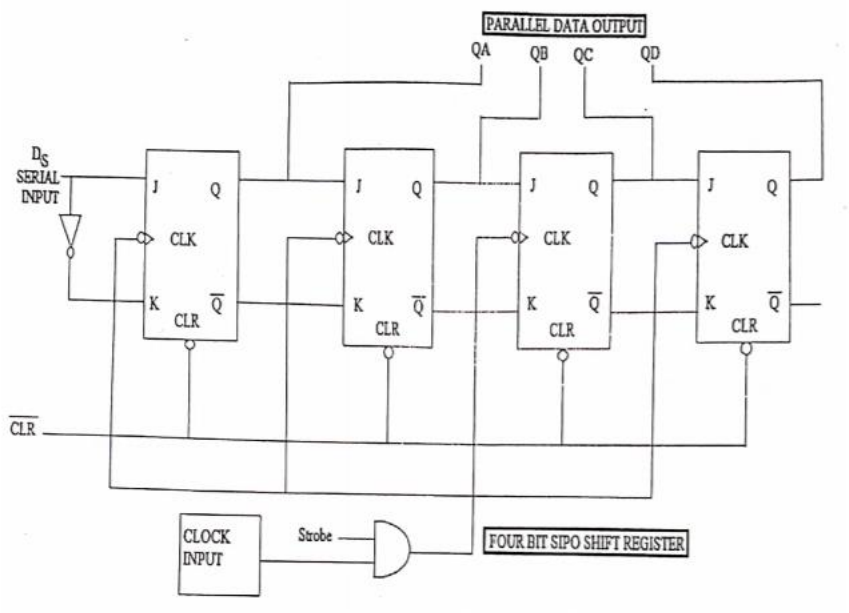
4) Parallel in parallel Out shift register

CIRCUIT DIAGRAM:

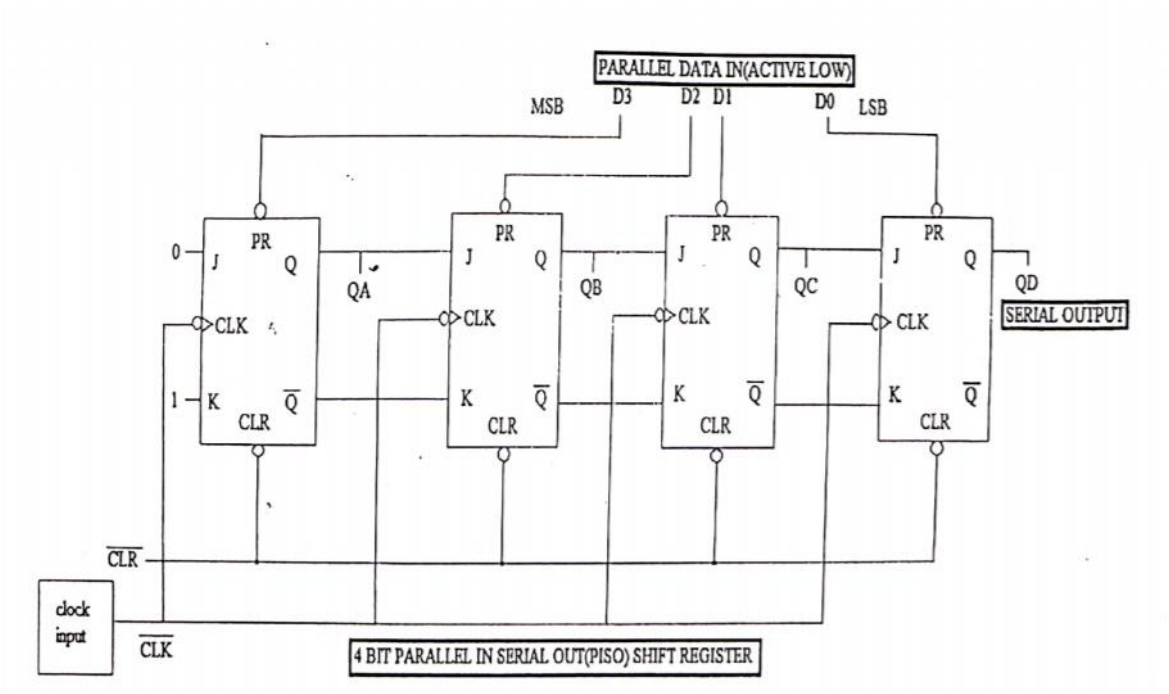
4 – BIT SISO REGISTER



4 BIT SIPO REGISTER



4 BIT PISO REGISTER



4 BIT PIPO REGISTER

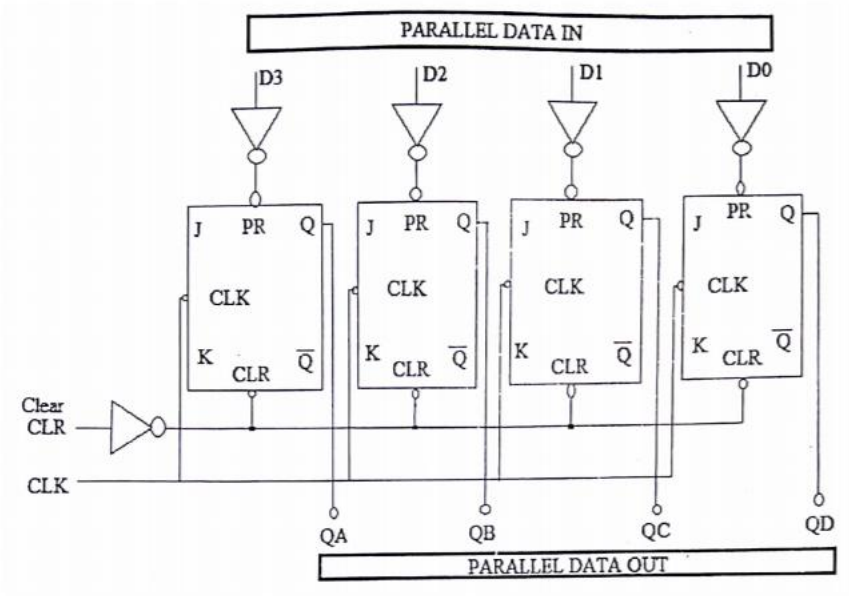
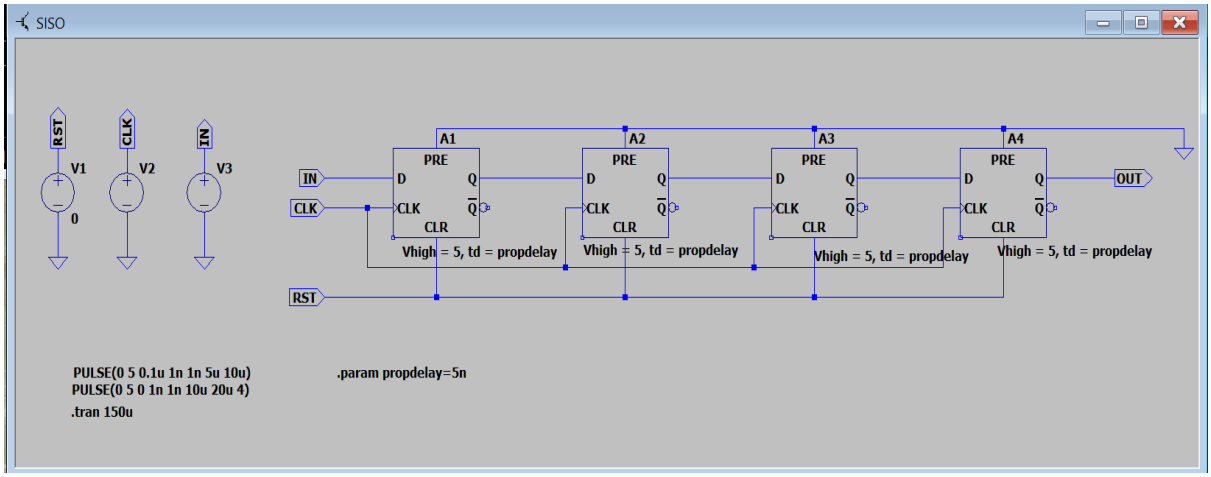
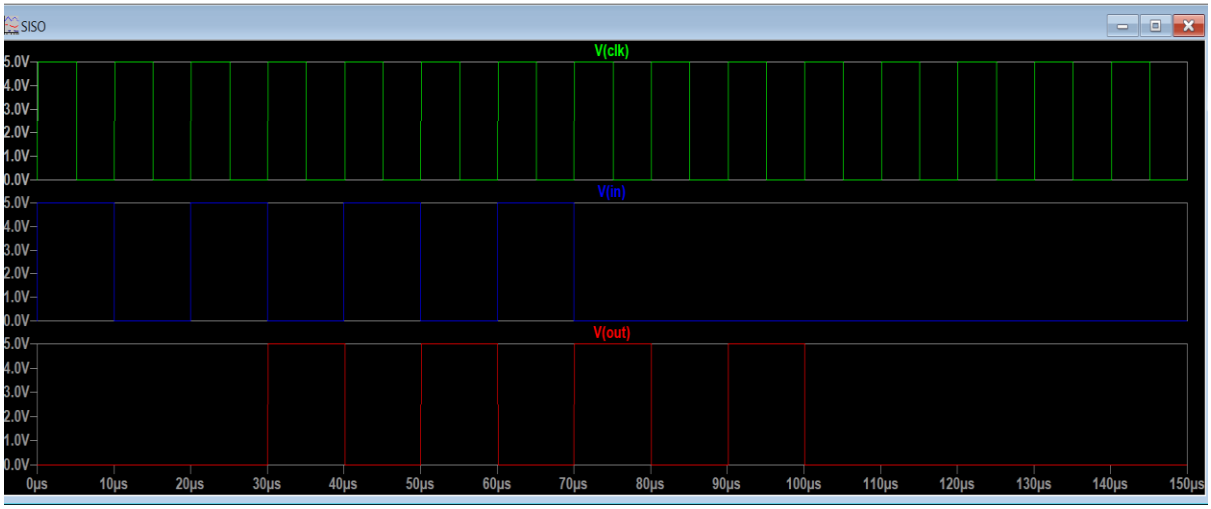


Figure 4: 4 BIT PIPO REGISTER CIRCUIT DIAGRAM

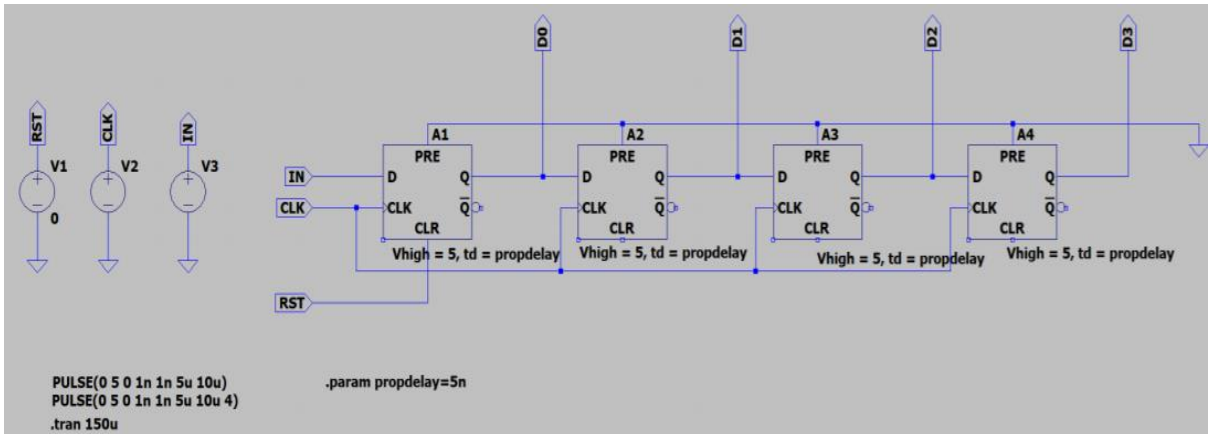
SOFTWARE SIMULATIONS

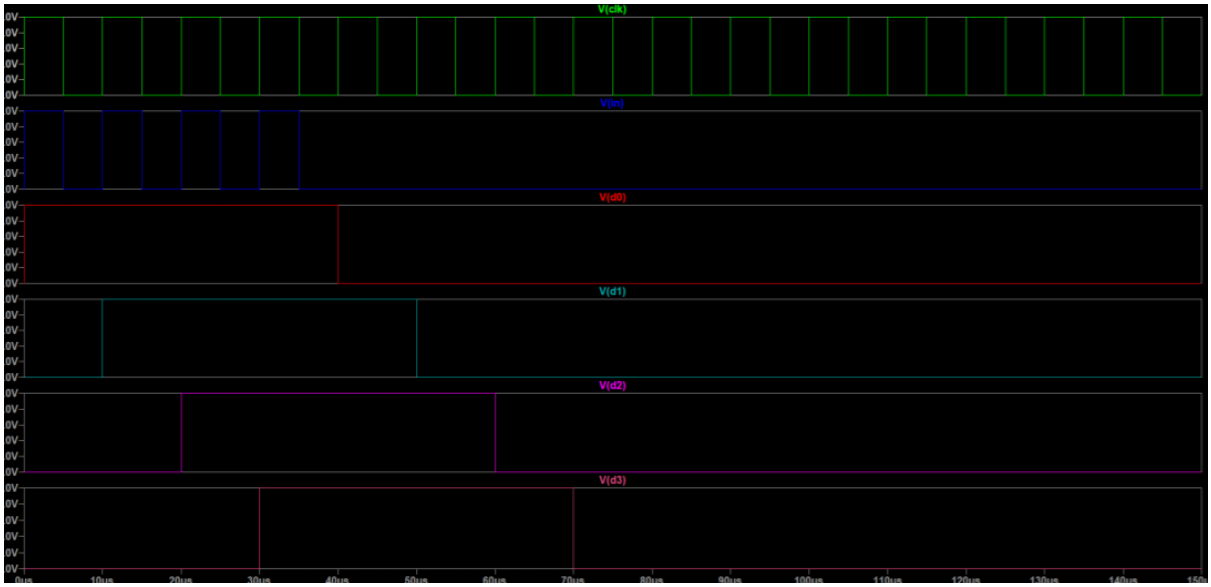
SISO



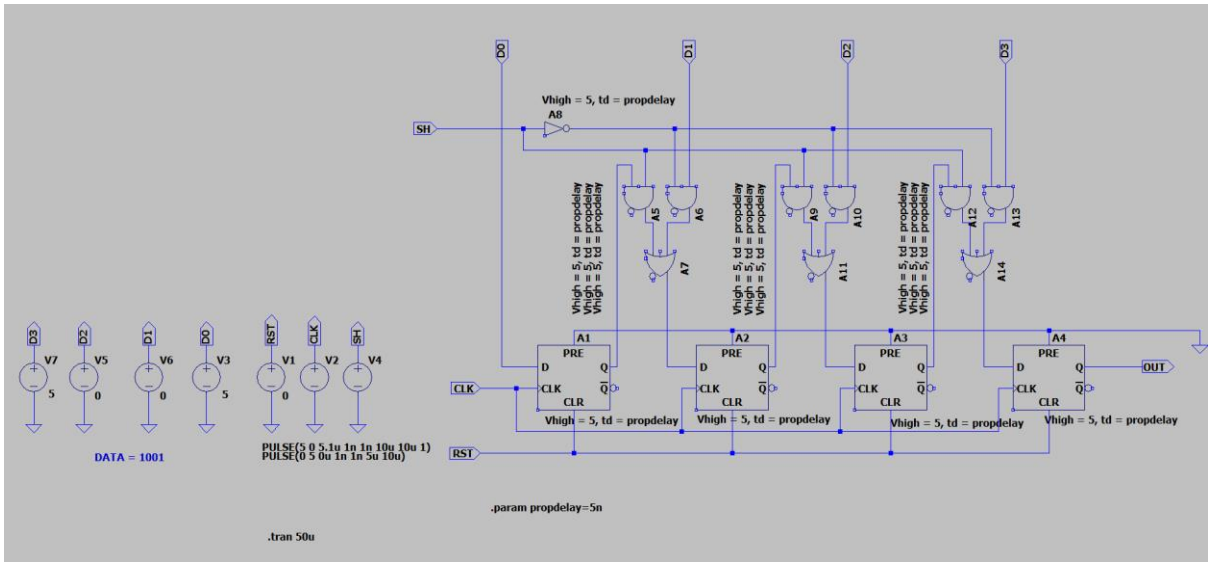


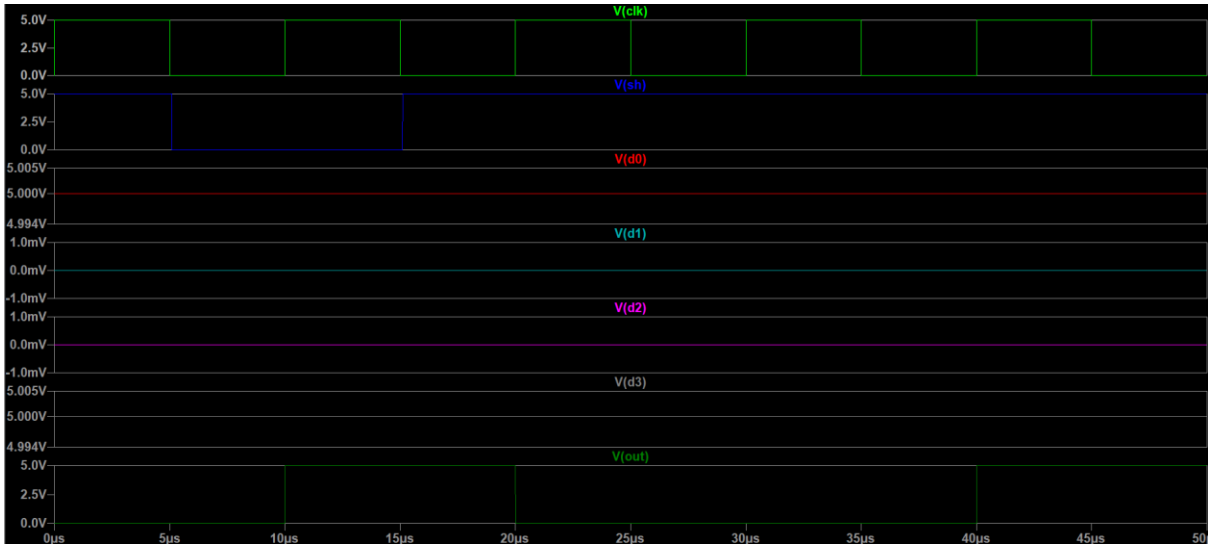
SIPO



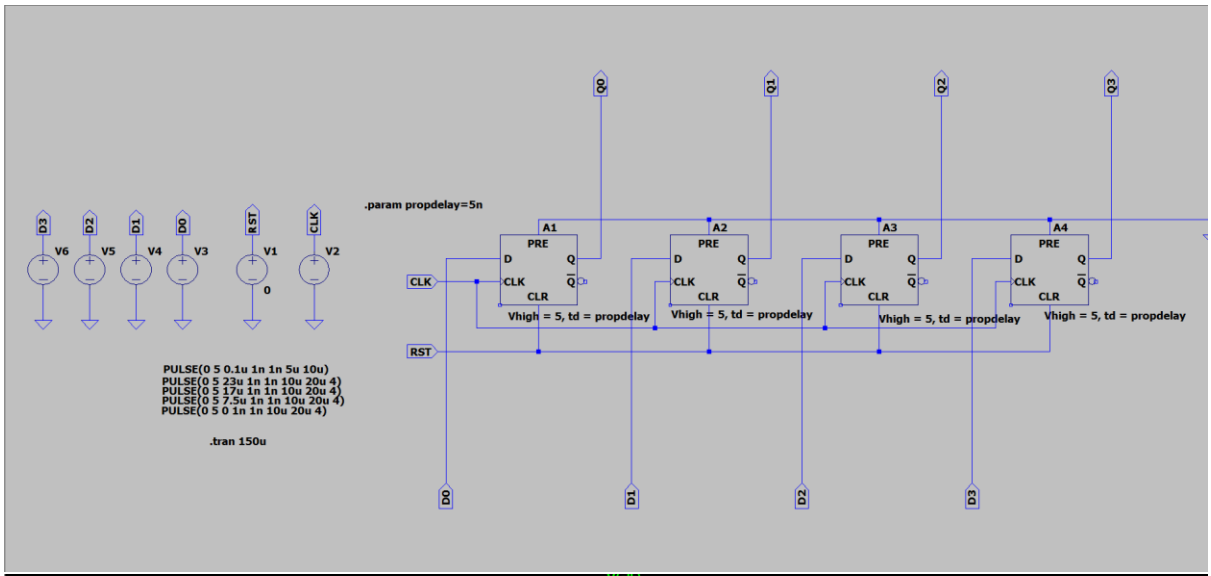

V(clk)
V(in)
V(d0)
V(d1)
V(d2)
V(d3)
0V
0us
10us
20us
30us
40us
50us
60us
70us
80us
90us
100us
110us
120us
130us
140us
150u

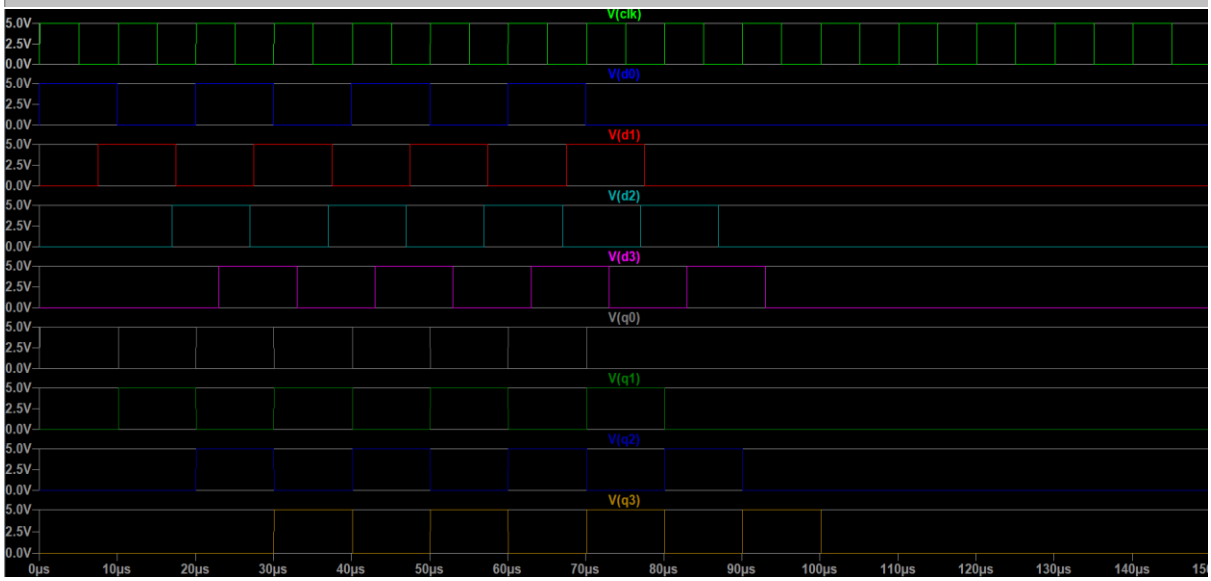
PISO


D0
D1
D2
D3
SH
Vhigh = 5, td = propdelay
A8
A5
A6
A7
A9
A10
A11
A12
A13
A14
A1
A2
A3
A4
PRE
D
CLK
CLR
Q
OUT
CLK
RST
V7
V5
V6
V3
V1
V2
V4
5
0
0
5
0
DATA = 1001
PULSE(5 0 5.1u 1n 1n 10u 10u 1)
PULSE(0 5 0u 1n 1n 5u 10u)
.param propdelay=5n
.tran 50u


V(clk)
5.0V
2.5V
0.0V
V(sh)
5.0V
2.5V
0.0V
V(d0)
5.005V
5.000V
4.994V
V(d1)
1.0mV
0.0mV
-1.0mV
V(d2)
1.0mV
0.0mV
-1.0mV
V(d3)
5.005V
5.000V
4.994V
V(out)
5.0V
2.5V
0.0V
0µs
5µs
10µs
15µs
20µs
25µs
30µs
35µs
40µs
45µs

PIPO


D3
D2
D1
D0
RST
CLK
V6
V5
V4
V3
V1
V2
0
PULSE(0 5 0.1u 1n 1n 5u 10u)
PULSE(0 5 23u 1n 1n 10u 20u 4)
PULSE(0 5 17u 1n 1n 10u 20u 4)
PULSE(0 5 7.5u 1n 1n 10u 20u 4)
PULSE(0 5 0 1n 1n 10u 20u 4)
.tran 150u
.param propdelay=5n
Q0
Q1
Q2
Q3
A1
A2
A3
A4
PRE
D
Q
CLK
CLR
Vhigh = 5, td = propdelay
D0
D1
D2
D3


V(clk)
V(d0)
V(d1)
V(d2)
V(d3)
V(q0)
V(q1)
V(q2)
V(q3)
5.0V
2.5V
0.0V
0µs
10µs
20µs
30µs
40µs
50µs
60µs
70µs
80µs
90µs
100µs
110µs
120µs
130µs
140µs