DIGITAL ELECTRONICS

EXPERIMENT – 6

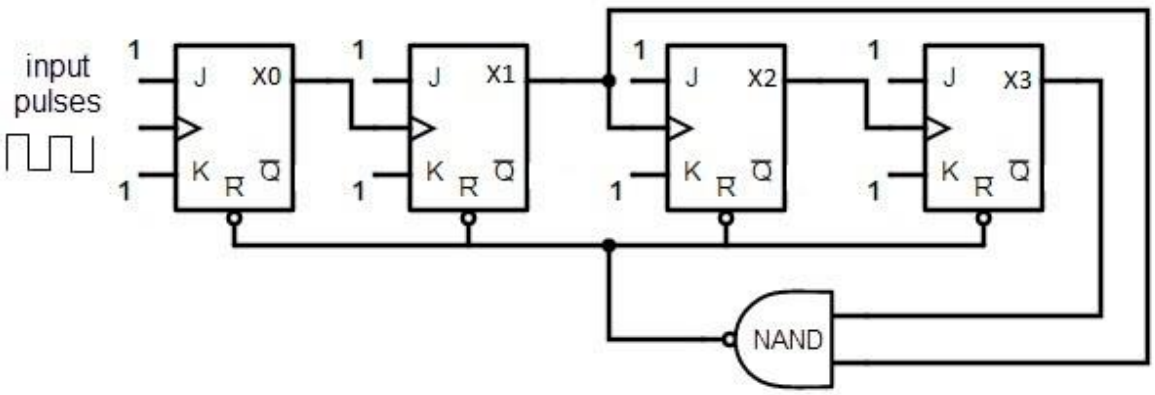
PULKIT PANDEY

2K19/EP/076

AIM: To verify the operation of a decade counter (5490 AJ).

THEORY: A decade counter is a serial digital counter that counts 10 digits. With each clock pulse the outputs advance to the next higher value, resetting to 0000 when the output is 1001 and a subsequent clock pulse is received. Decade counters are used in clock circuits, frequency dividers, state machines, and sequencers, just to name a few applications. In a decade counter constructed with D flip flops, the clock input of every flip flop is connected to the output of the last flip flop except for the first flip flop. The Q output of each flip flop is connected to its D-input. The Q-outputs of the 2nd and 4th flip flop are connected to an AND gate which goes high when they are both high. The AND gate is further connected to the clear line giving CLR input to all the flip flops. Thus, the counter counts from 0000 to 1001, at which point the counter is reset by the output of the AND gate and a new clock pulse is delivered to the flip flops.

CIRCUIT DIAGRAM:



4 BIT ASYNCHRONOUS DECADE COUNTER

SOFTWARE SIMULATIONS: