DIGITAL ELECTRONICS

EXPERIMENT-10

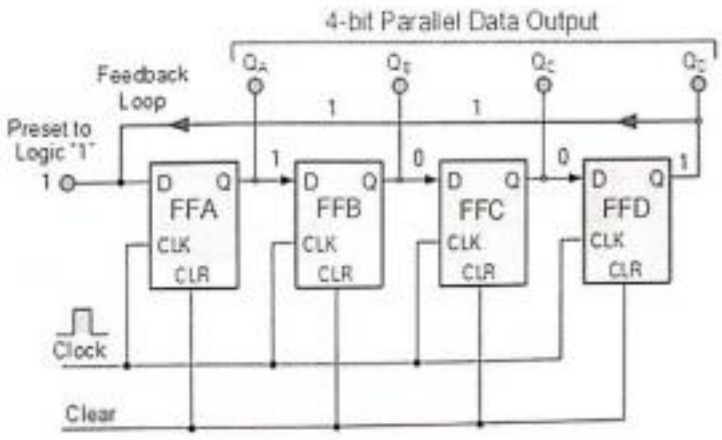
PULKIT PANDEY

2K19/EP/076

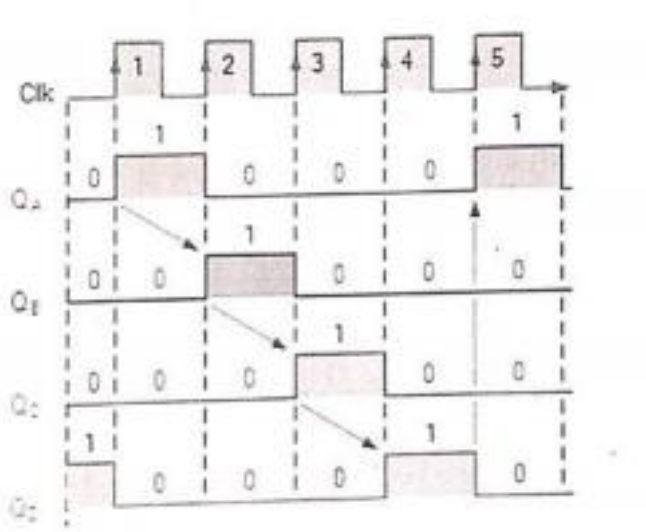
AIM: To design and implement the operation of Ring counter and Johnson Counter using D-flip flops.

THEORY: A ring counter is a special type of application of the Serial IN Serial OUT Shift register. The only difference between the shift register and the ring counter is that the last flip flop outcome is taken as the output in the shift register. But in the ring counter, this outcome is passed to the first flip flop as an input. All of the remaining things in the ring counter are the same as the shift register. The synchronous Ring counter, is preset so that exactly one data bit in the register is set to logic “1” with all the flip-flops together in order to “RESET” their outputs to a logic “0” level and then a “PRESET” pulse is applied to the input of the first flip before the clock pulses are applied. This then places a single logic”1” value into the circuit to the ring counter.

CIRCUIT DIAGRAMS:



Ring Counter Circuit



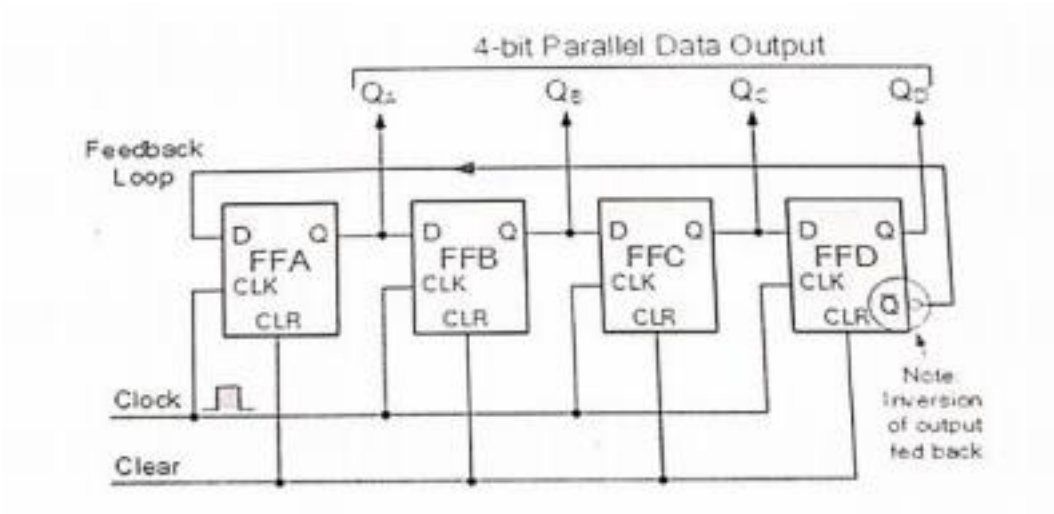
Timing Diagram

Clock Cycle	Q_1	Q_2	Q_3	Q_4
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0
6	0	1	0	0
.	.	.	.	.
.	.	.	.	.

Bit-pattern repeats for every 4 clock cycles

Truth Table

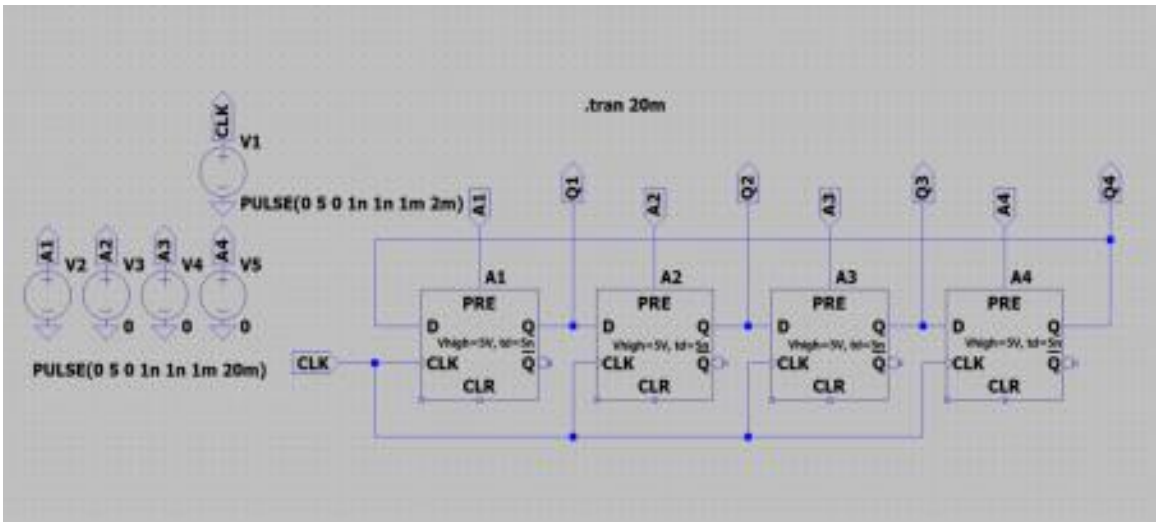
Johnson Counter: The Johnson Ring Counter or Twisted Ring Counters, is another shift register with feedback exactly the same as the standard Ring-Counter above, except that this time the inverted output Q of the last flip- flop is now connected back to the input D of the first flip-flop as shown below.

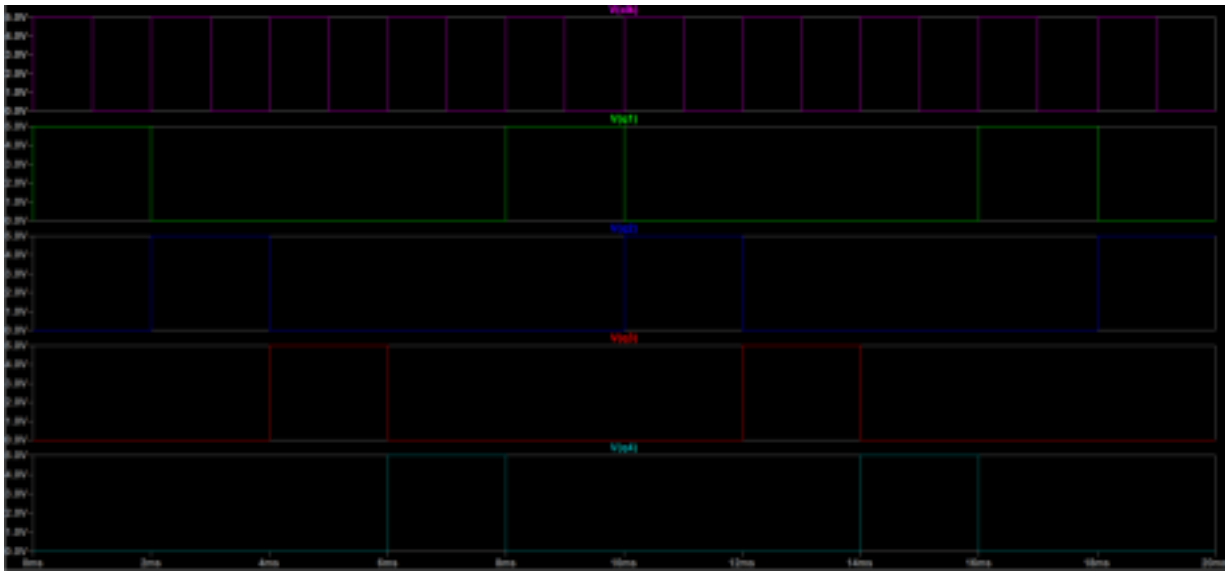


Johnson Counter

SOFTWARE SIMULATIONS:

Ring Counter:





Johnson Counter: